

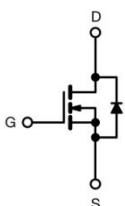


## N-channel Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.	550	
$R_{DS(on)}$ max. at 25°C ( $\Omega$ )	$V_{GS}=10V$	1.5
$Q_g$ max. (nC)	42	
$Q_{gs}$ (nC)	12	
$Q_{gd}$ (nC)	6.5	
Configuration	single	



TO-252



Schematic diagram

## Features

- $I_D=5A$  ( $V_{GS}=10V$ )
- Ultra Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested
- RoHS compliant

## Applications

- Switching Mode Power Supplies (SMPS)
- PWM Motor Controls
- DC to DC Converters
- LED Lighting
- Bridge Circuits

## ORDERING INFORMATION

Device	SPD5N50G
Device Package	TO-252
Marking	5N50G

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ C$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain to Source Voltage	$V_{DSS}$	500 <sup>(1)</sup>	V
Continuous Drain Current (@ $T_C=25^\circ C$ )	$I_D$	5 <sup>(1)</sup>	A
Continuous Drain Current (@ $T_C=100^\circ C$ )		3.1	A
Drain current pulsed <sup>(2)</sup>	$I_{DM}$	20	A
Gate to Source Voltage	$V_{GS}$	30	V
Single pulsed Avalanche Energy <sup>(3)</sup>	$E_{AS}$	285	mJ
Peak diode Recovery dv/dt <sup>(4)</sup>	dv/dt	6	V/ns
Total power dissipation (@ $T_C=25^\circ C$ )	$P_D$	112	W
Derating Factor above 25°C		0.88	W/°C
Operating Junction Temperature & Storage Temperature	$T_{STG}, T_J$	-55 to + 150	°C
Maximum lead temperature for soldering purpose	$T_L$	260	°C

## Notes

1. Drain current is limited by maximum junction temperature.
2. Repetitive rating : pulse width limited by junction temperature.
3.  $L = 15mH$ ,  $I_{AS} = 5A$ ,  $V_{DD} = 50V$ ,  $R_G=25\Omega$ , Starting at  $T_J = 25^\circ C$
4.  $I_{SD} \leq 5A$ ,  $di/dt = 100A/us$ ,  $V_{DD} \leq BV_{DSS}$ , Starting at  $T_J = 25^\circ C$



THERMAL CHARACTERISTICS			
Parameter	Symbol	Value	Unit
Thermal resistance, Junction to case	$R_{thjc}$	0.75	$^{\circ}C/W$
Thermal resistance, Junction to ambient	$R_{thja}$	62.5	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}C$ unless otherwise specified )						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain to source breakdown voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	500	--	--	V
Breakdown voltage temperature coefficient	$\Delta BV_{DSS} / \Delta T_J$	$I_D=250\mu A$ , referenced to $25^{\circ}C$	--	0.5	--	$V/^{\circ}C$
Drain to source leakage current	$I_{DSS}$	$V_{DS}=500V, V_{GS}=0V$	--	--	1	$\mu A$
		$V_{DS}=400V, T_C=125^{\circ}C$	--	--	50	$\mu A$
Gate to source leakage current, forward	$I_{GSS}$	$V_{GS}=30V, V_{DS}=0V$	--	--	100	nA
Gate to source leakage current, reverse		$V_{GS}=-30V, V_{DS}=0V$	--	--	-100	nA
<b>On Characteristics</b>						
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	--	4	V
Drain to source on state resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=2.5A$	--	1.35	1.5	$\Omega$
Forward Transconductance	$G_{fs}$	$V_{DS}=30V, I_D=2.5A$	--	3.7	--	S
<b>Dynamic Characteristics</b>						
Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V, f=1MHz$	--	1271	--	pF
Output capacitance	$C_{oss}$		--	143	--	
Reverse transfer capacitance	$C_{rss}$		--	1	--	
Turn on delay time	$t_{d(on)}$	$V_{DS}=250V, I_D=5A, R_G=25\Omega$	--	27.5	--	ns
Rising time	$t_r$		--	25	--	
Turn off delay time	$t_{d(off)}$		--	127	--	
Fall time	$t_f$		--	35	--	
Total gate charge	$Q_g$	$V_{DS}=400V, V_{GS}=10V, I_D=5A$	--	31.5	--	nC
Gate-source charge	$Q_{gs}$		--	12	--	
Gate-drain charge	$Q_{gd}$		--	6.5	--	

SOURCE TO DRAIN DIODE RATINGS CHARACTERISTICS						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous source current	$I_S$	Integral reverse p-n Junction diode in the MOSFET	--	--	5	A
Pulsed source current	$I_{SM}$		--	--	20	A
Diode forward voltage drop.	$V_{SD}$	$I_S=5A, V_{GS}=0V$	--	--	1.2	V
Reverse recovery time	$T_{rr}$	$I_S=5A, V_{GS}=0V,$	--	567	--	ns
Reverse recovery Charge	$Q_{rr}$	$di/dt=100A/\mu s$	--	4	--	$\mu C$



Fig1. Output characteristics

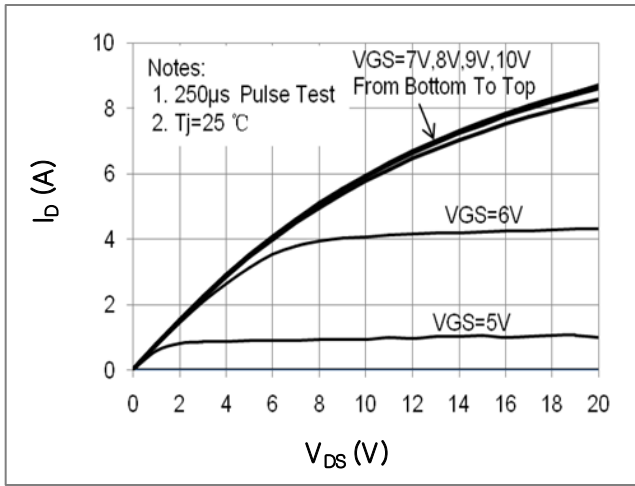


Fig2. Drain-source on-state resistance

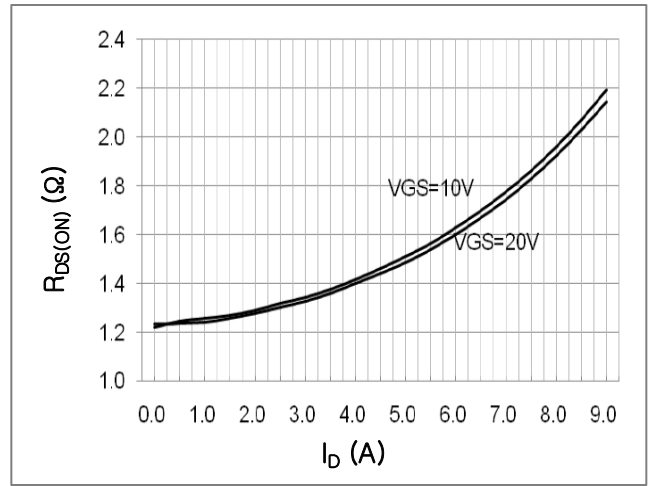


Fig3. Gate charge characteristics

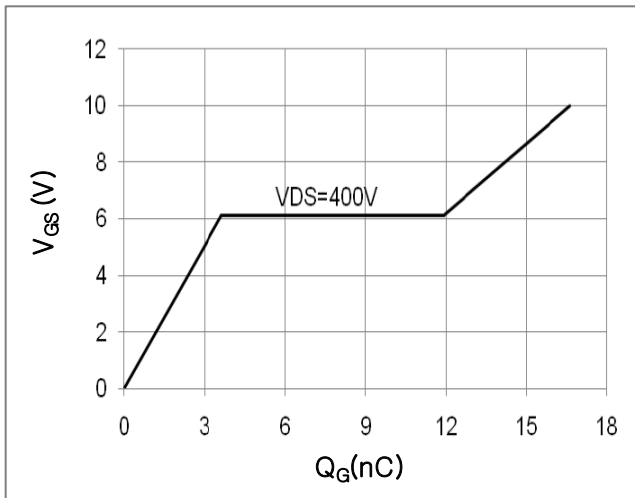


Fig 4. Capacitance Characteristics

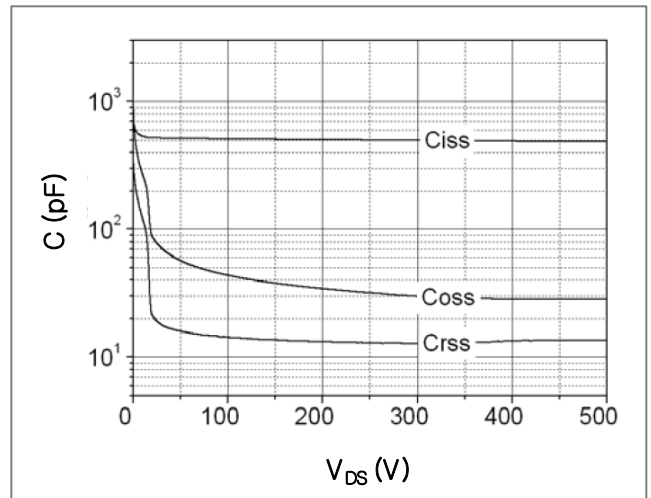


Fig 5. RDS(ON) vs junction temperature

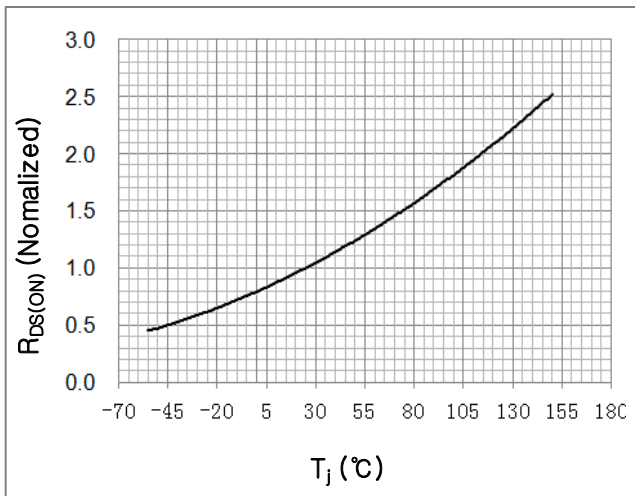


Fig 6. BVDS vs junction temperature

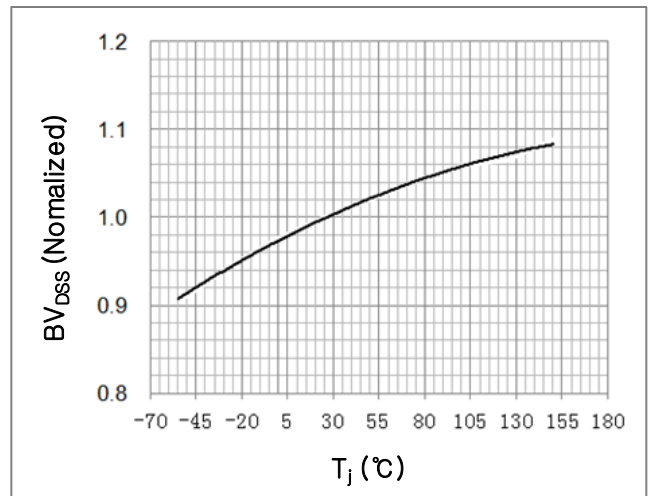




Fig 7 . Safe operating area

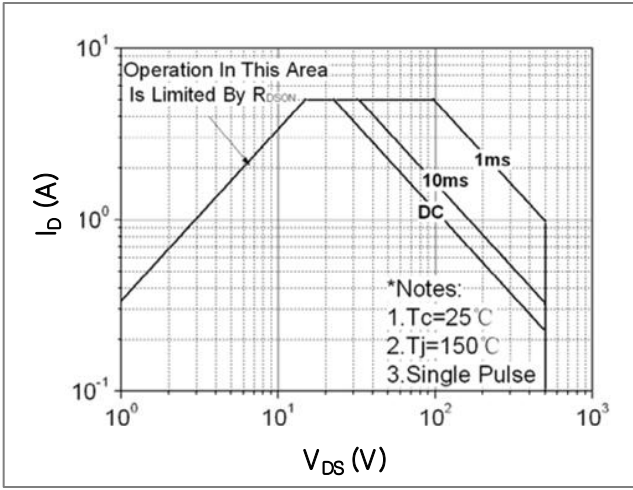


Fig 8 . Transient thermal impedance

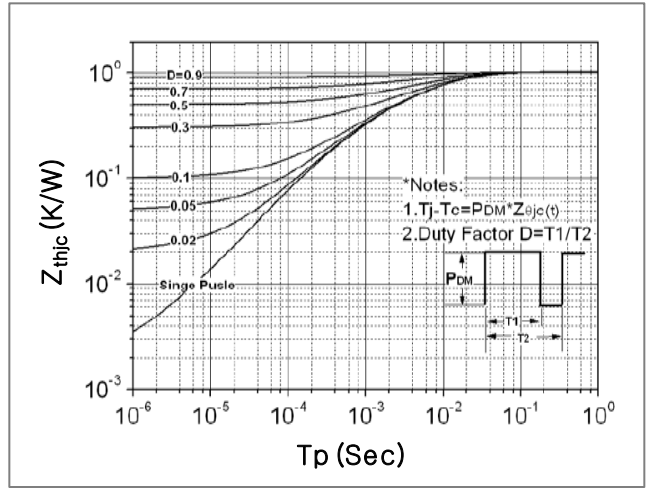


Fig 9. Forward characteristics of reverse diode

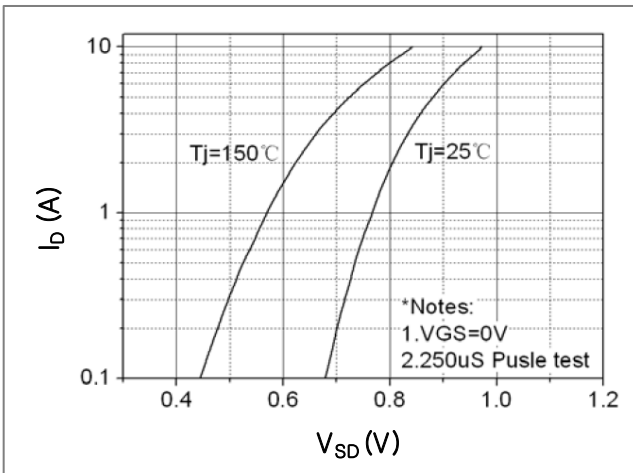


Fig 10. Gate charge test circuit & waveform

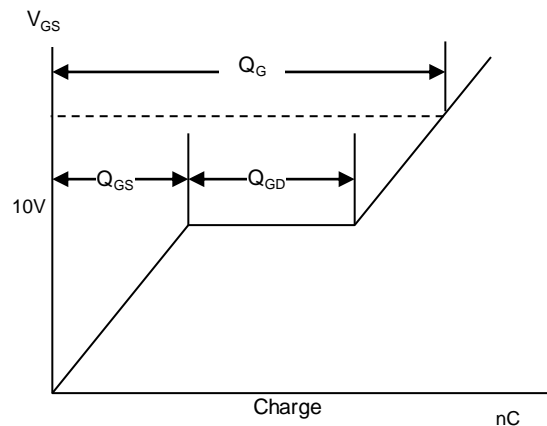
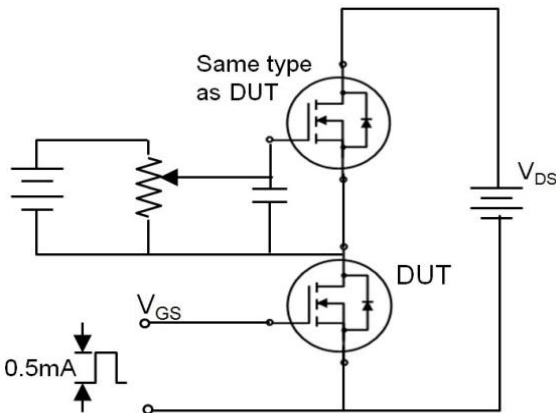


Fig 11. Switching time test circuit & waveform

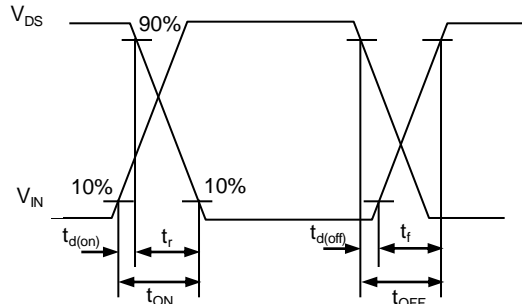
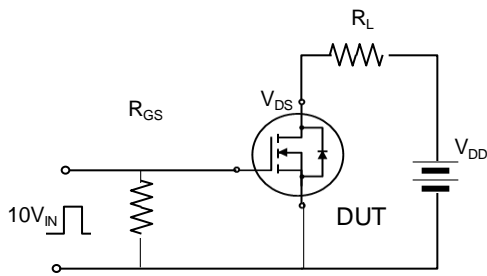


Fig 12. Unclamped Inductive switching test circuit & waveform

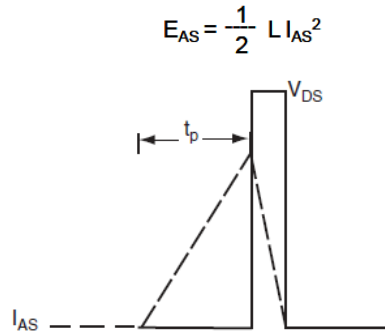
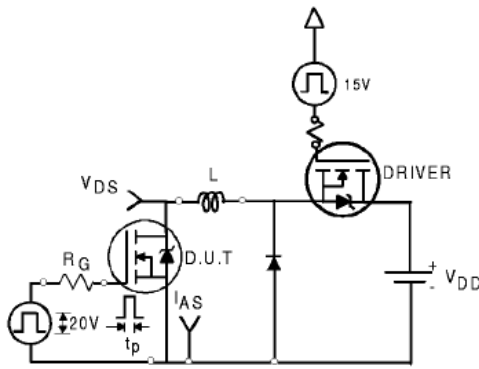
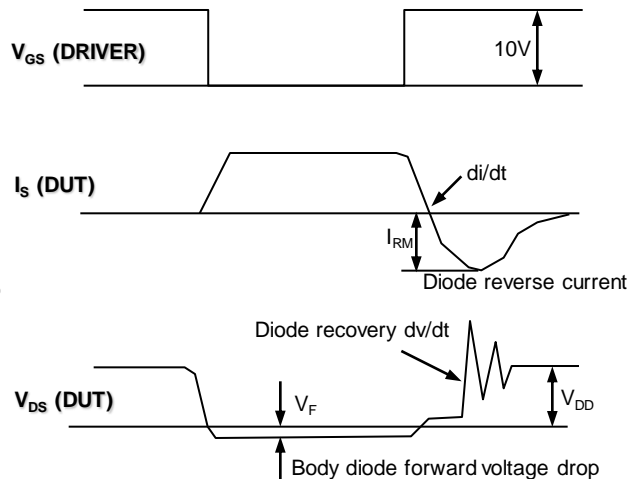
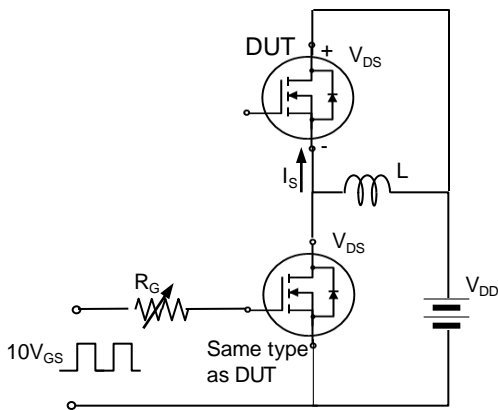


Fig 13. Peak diode recovery dv/dt test circuit & waveform



\*. dv/dt controlled by R<sub>G</sub>  
 \*. I<sub>S</sub> controlled by pulse period



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