2.7V-20V VIN, 15A Switch Current, Fully Integrated Synchronous Boost Converter with Load Disconnection Control

FEATURES

- Wide Input Voltage Range: 2.7V-20V
- Wide Output Voltage Range:4.5V-21V
- Fully Integrated 13mΩ High Side FET and 11mΩ Low Side FET
- Up to 96% Efficiency at Vin=7.2V, Vout=15V, and Iout=2A
- Up to 15A Switch Current and Programmable Peak Current Limit
- Load Disconnection Control with an External P-Channel MOSFET
- Typical Shut-down Current: 1uA
- Programmable Switching Frequency: 200kHz-1.0MHz
- PFM Mode
- Programmable Soft Start
- Output and Feedback Overvoltage Protection
- Thermal Shutdown Protection: 150°C
- Available in DFN-20L 3.5mmx4.5mm Package

APPLICATIONS

- Bluetooth Audio
- Power Banks
- Type-C Power Delivery

DESCRIPTION

The SCT12A2 is a high efficiency synchronous boost converter with fully integrated a 13mΩ high-side MOSFET and an 11mΩ low-side MOSFET, supporting 2.7V to 20V input voltage range and up to 15-A switch current. The switch current limit can be adjustable with an external resistor.

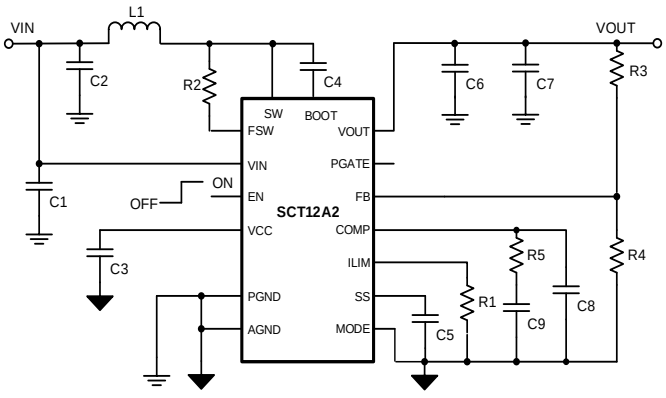
The SCT12A2 adapts constant off-time peak current control to provide fast transient. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions. Connection MODE pin to ground selects the Pulse Frequency Modulation (PFM) operation.

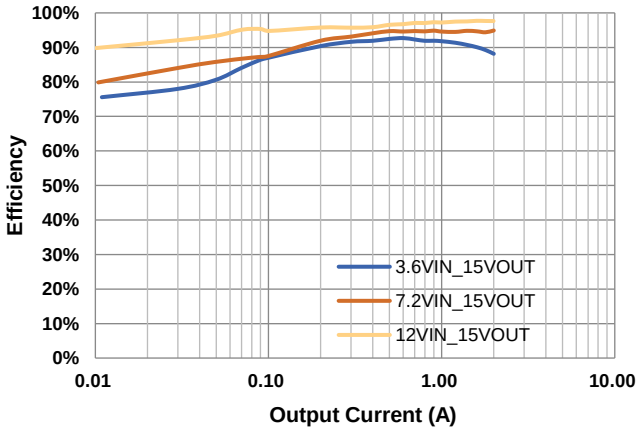
The SCT12A2 offers the gate control for an external P-channel MOSFET to disconnect load from boost converter output. This safety feature prevents the damage on load from input shooting through to output in shutdown condition.

The SCT12A2 monitors both output voltage and feedback voltage to protect over voltage condition. It features cycle-by-cycle peak current limit and thermal shutdown protection when the device over loads.

The device is available in a low-profile package DFN-20L 3.5mmx4.5mmx0.9mm with enhanced thermal power pad.

TYPICAL APPLICATION





Power Efficiency, Vout=15V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0 released to market

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT12A2DHK	12A2	20-Lead 3.5mm×4.5mm Plastic DFN

1）For Tape & Reel, Add Suffix R (e.g. SCT12A2DHKR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

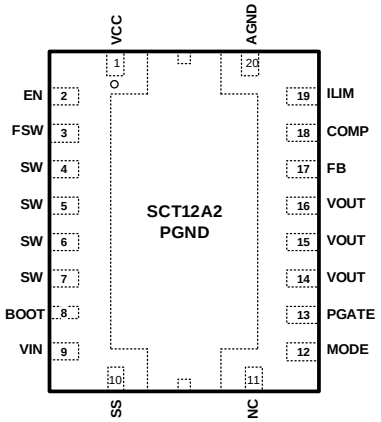
DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	28	V
VIN, SW, VOUT, FSW, PGATE	-0.3	22	V
VCC, LIM，FB， EN,SS, COMP, MODE	-0.3	5.5	V
Operating junction temperature T_J(2)	-40	125	C
Storage temperature T_{STG}	-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN CONFIGURATION

Top View: 20-Lead Plastic DFN 3.5mmx4.5mm



PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VCC	1	Internal linear regulator output. Connect a 1uF or larger ceramic capacitor to ground. VCC cannot to be externally driven. No additional components or loading is recommended on this pin.
EN	2	Enable logic input. A 800KΩ resistor connects this pin to ground inside. Floating disables the device.
FSW	3	Place a resistor from this pin to SW to set the switching frequency.
SW	4,5,6,7	Switching node of the boost converter.
BOOT	8	Power supply for the high-side FET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
SS	10	Place a ceramic cap from this pinto ground to program soft-start time. An internal 5uA current source pulls SS pin to VCC.
NC	11	Not Connected.

MODE	12	Ground connected enables PSM mode.
PGATE	13	Gate driver output for an external P-channel MOSFET to disconnect load.
VOUT	14,15,16	Boost converter output. Connect a 1uF decoupling capacitor as close to VOUT pins and power ground pad as possible to reduce the ringing voltage of SW.
FB	17	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference value of 1.2V typical.
COMP	18	Output of the error amplifier and switching converter loop compensation point.
ILIM	19	Inductor peak current limit set point input. A resistor connecting this pinto ground sets current limit through low-side power FET.
AGND	20	Analog ground. Analog ground should be used as the common ground for all small signal analog inputs and compensation components. No electrical connection to PGND inside.
PGND	21	Power ground. Must be soldered directly to ground planes using multiple vias directly under the IC for improved thermal performance and electrical contact.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	20	V
V_{OUT}	Output voltage range	4.5	21	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-20L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	38	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	39	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT12A2 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT12A2. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		20	V
V_{OUT}	Output voltage range		4.5		21	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.6 200	2.7	V mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1	3	uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching		1		uA
	Quiescent current from VOUT			420		uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.8		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB	FPWM mode	1.180	1.206	1.230	V
		PSM mode	1.196	1.220	1.244	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		20		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		20		uA
V_{COMP_H}	COMP high clamp	V_{FB}=1V， R_{ILIM}=100KΩ		1.5		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.5V, R_{ILIM}=100KΩ,PFM		0.6		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			13		mΩ
R_{DSON_L}	Low side FET on-resistance			11		mΩ
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=100kΩ		15		A
Enable and Mode						
V_{EN}	Enable high threshold Enable low threshold	V_{CC}=5V	 0.4		1.2	V V
R_{EN}	Enable pull down resistance			800		kΩ
V_{MODE}	MODE high threshold MODE low threshold	V_{CC}=5V	 1.5		4	V V
I_{SS}	Soft-start charging current			5		uA
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=301k, V_{OUT}=12V		520		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=301k, V_{OUT}=12V		160	200	ns
t_{OFF_MIN}	Minimum off-time	R_{FSW}=301k, V_{FB}=0V		480	150	ns
Load Disconnection Control						
I_{PGATE}	PGATE pull down current			250		uA
V_{PGATE_C}	Clamp voltage between PGATE and VOUT			6.1	7	V
Protection						
V_{OVP_VOUT}	Output overvoltage threshold	V_{OUT} rising		22		V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Hysteresis			400		mV
V_{OVP_VFB}	Feedback overvoltage with respect to reference voltage	V_{FB} rising V_{FB} falling		110 105		% %
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
	Hysteresis			20		°C

TYPICAL CHARACTERISTICS

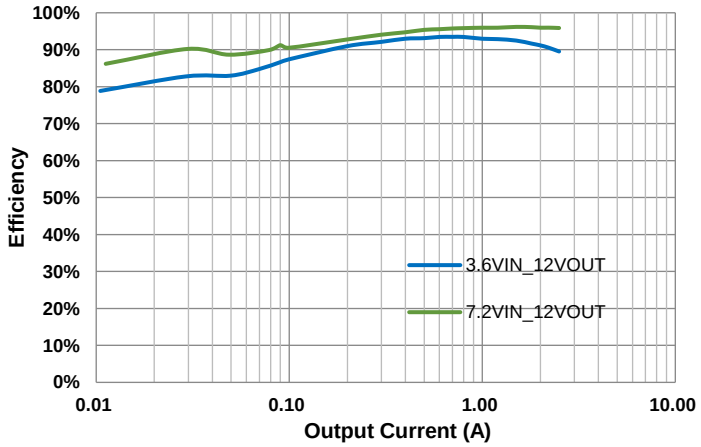


Figure 1. Efficiency, Vout=12V, fsw=400KHz, PFM

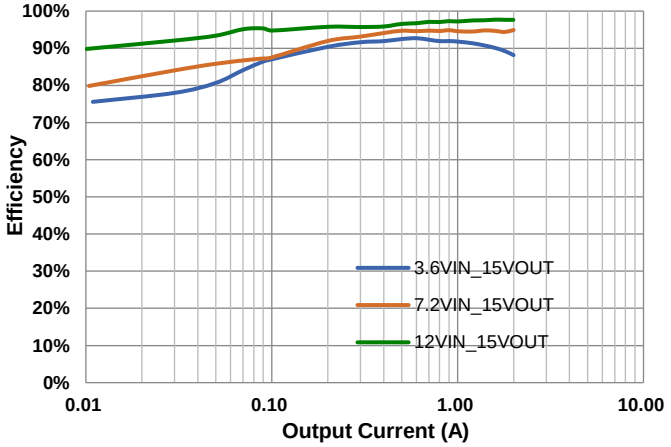


Figure 2. Efficiency, Vout=15V, fsw=400KHz, PFM

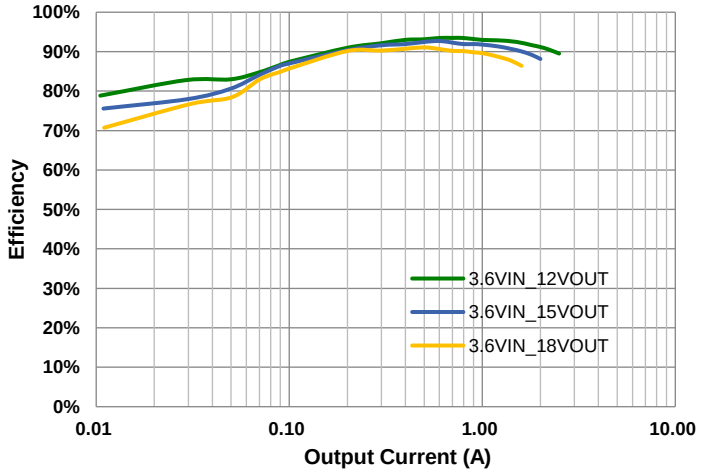


Figure 3. Efficiency, fsw=400 kHz, 1-cell Battery, PFM

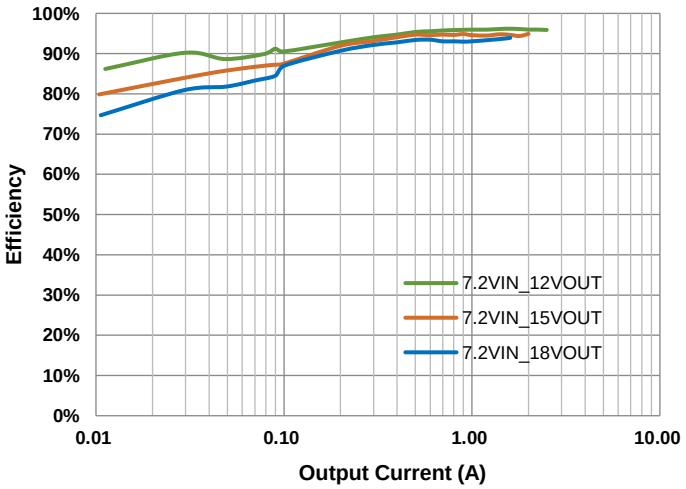


Figure 4. Efficiency, fsw=400KHz, 2-cells Battery, PFM

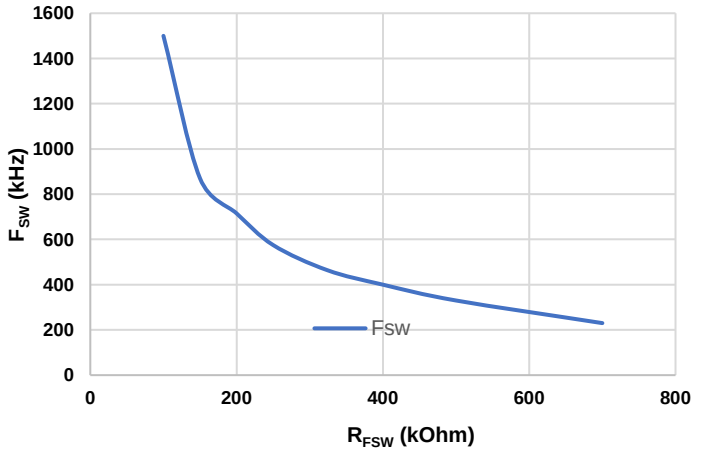


Figure 5. Switching Frequency vs FSW Resistance

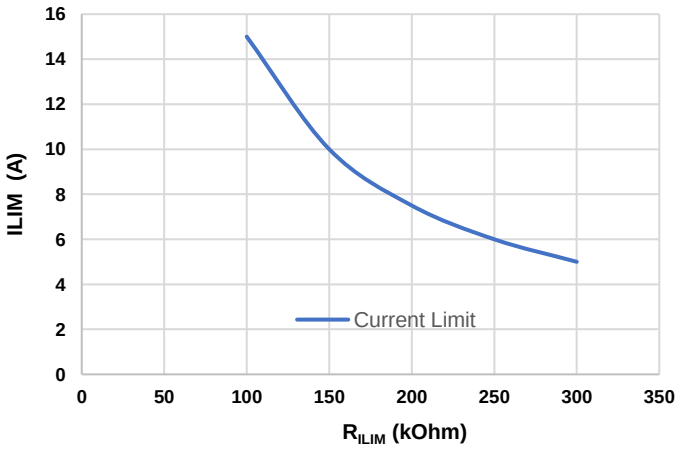


Figure 6. Inductor Peak Current Limit vs RLIM Resistance

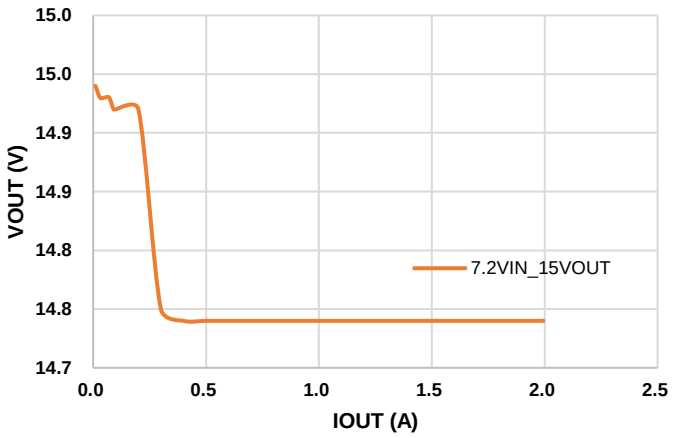


Figure 7. Load Regulation (Vin=7.2V, Vout=15V)

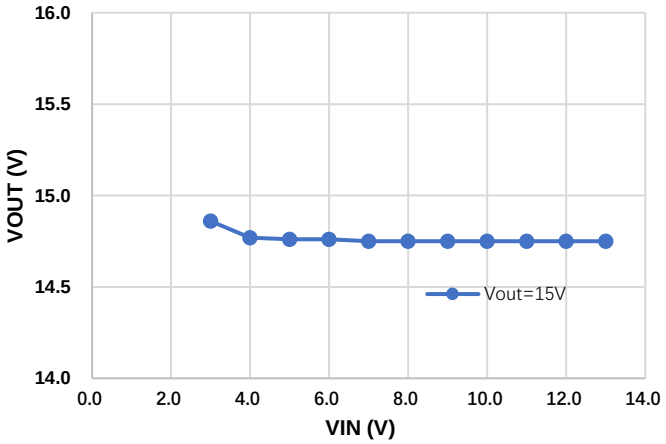


Figure 8. Line Regulation (Vout=15V)

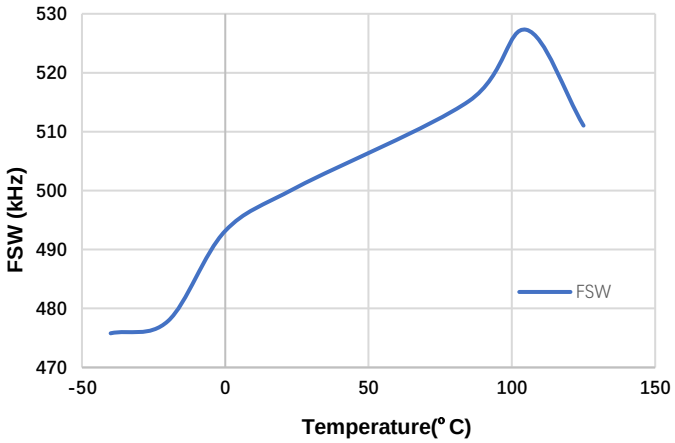


Figure 9. Frequency vs Temperature

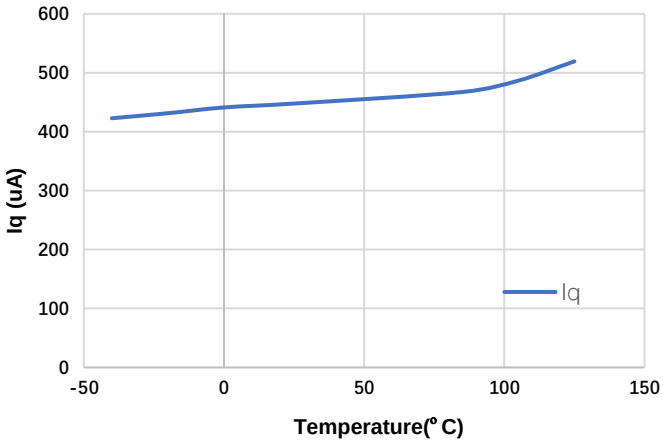


Figure 10. Quiescent Current vs Temperature

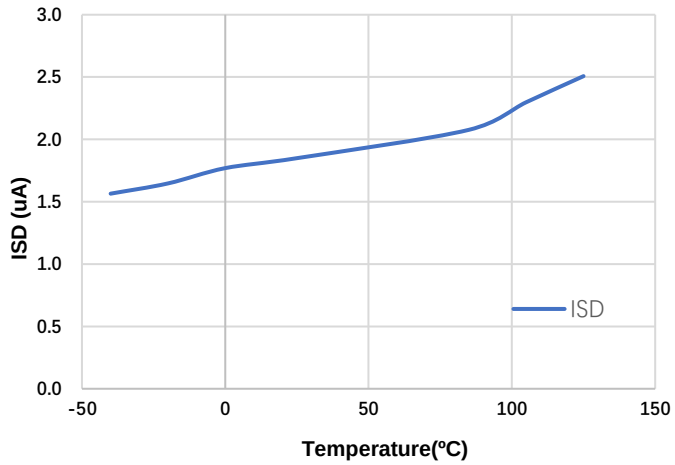


Figure 11. Shutdown Current vs Temperature

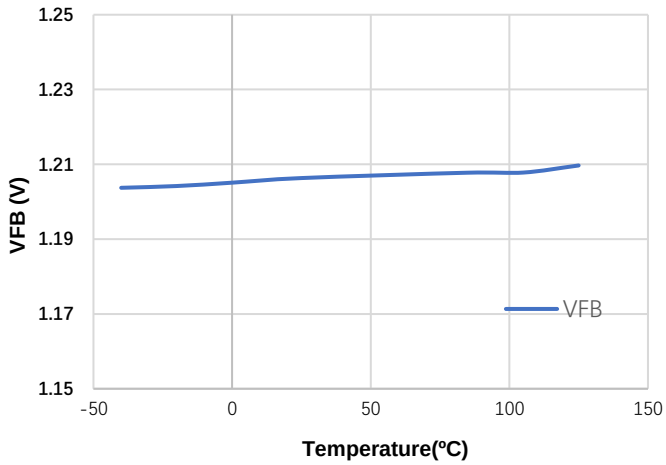
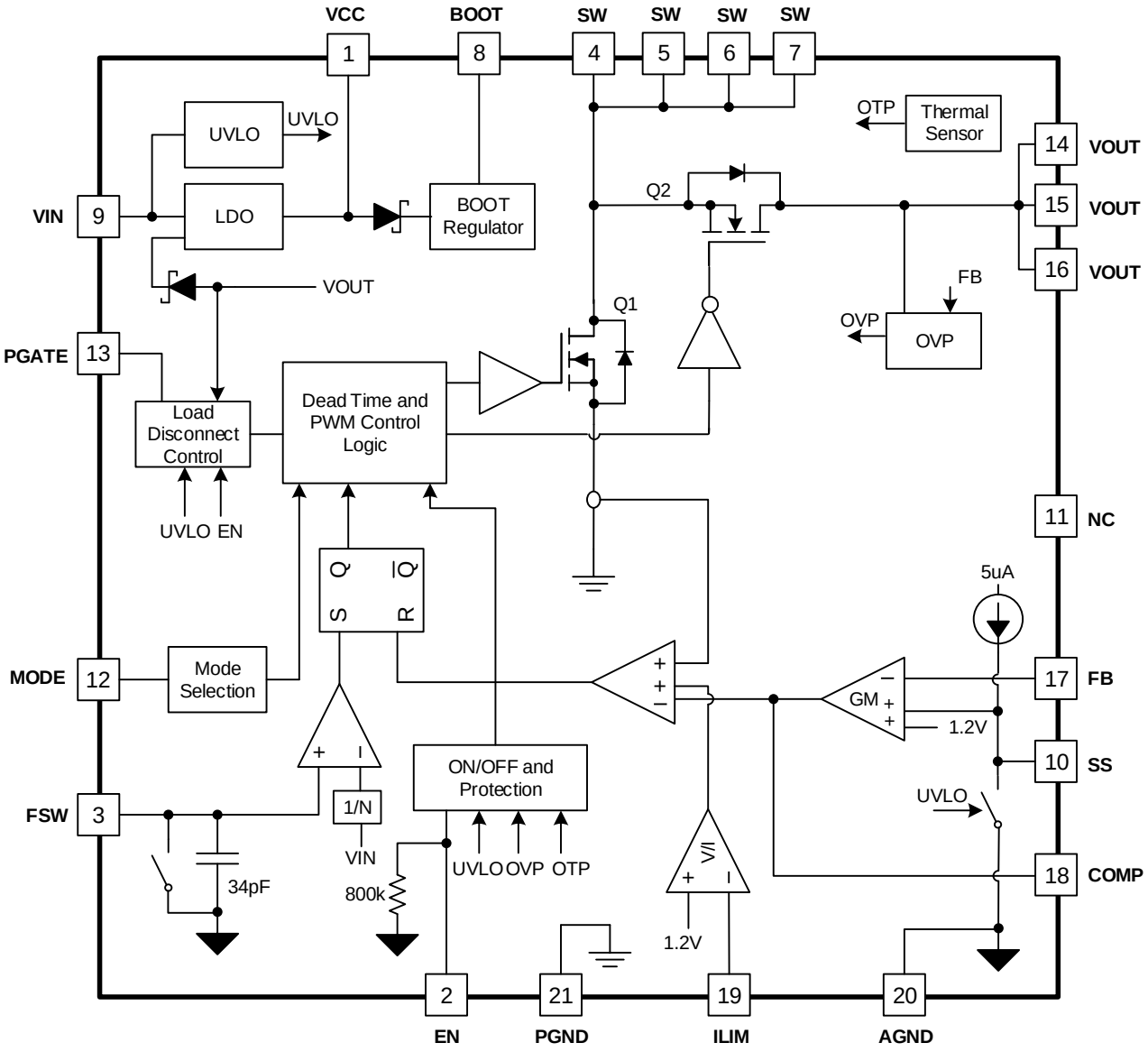


Figure 12. Feedback Reference vs Temperature

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT12A2 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage of COMP. After the inductor current reaches the peak current, the device turns off low-side MOSFET and inductor goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases. Based on Vin and Vout voltage, the device predicts required off-time and turns off high-side MOSFET Q2.This repeats on cycle-by-cycle based.

The voltage feedback loop regulates the FB voltage to a 1.2V reference with an internal trans-conductance error amplifier. The feedback loop stability and transient response are optimized through an external loop compensation network connected to the COMP pin.

When MODE pin is connected to ground, the SCT12A2 works at PFM mode to further increase the efficiency in light load condition. The quiescent current of SCT12A2 is 420uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current is 1μA.

A resistor connected between SW pin and the FSW pin sets the switching frequency. The wide switching frequency range of 200 kHz to 1.0 MHz offers optimization on efficiency or size of filter components.

The SCT12A2 provides PGATE pin to control the gate of an external load disconnection P-channel MOSFET, which completely disconnects the load from the input during output shutdown condition. During start-up, the SCT12A2 gradually turns on the load disconnection switch to limit the inrush current.

The SCT12A2 device features adjustable soft-start time, cycle-by-cycle low-side FET current limit, over-voltage protection, and over-temperature protection.

The SCT12A2 uses two separate ground pins to avoid ground bouncing due to the high switching current through the N-channel power MOSFET. AGND pin sets the reference for all control functions. The source of the power MOSFET connects to PGND pin. Both grounds must be connected to the thermal pad on the PCB at the closest point.

VIN Power

The SCT12A2 is designed to operate from an input voltage supply range between 2.7 V to 20V. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is ceramic capacitor with a value of 47μF or 2 x 22uF.

VCC Power

The internal VCC LDO provides the bias power supply for internal circuitries. A ceramic capacitor of no less than 1uF is required to bypass from VCC pin to ground. During starting up, input of VCC LDO is from VIN pin. Once the output voltage at VOUT pin exceeds VIN voltage, VCC LDO switches its input to VOUT pin. This allows higher voltage headroom of VCC at lower input voltage. The maximum current capability of VCC LDO is 130mA typical. No additional components or loading are recommended on this pin.

Under Voltage Lockout UVLO

The SCT12A2 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunctioning and the battery over discharging. The default VIN rising threshold is 2.6V typical at startup and falling threshold is 2.4V typical at shutdown. The internal VCC LDO dropout voltage is about 100mV and the device is disabled when VCC falling trips 2.1V typical threshold. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT to SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT12A2 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold (minimum 0.4V). An internal 800KΩ resistor connects EN pin to the ground. Floating EN pin automatically disables the device.

The SCT12A2 features programmable soft start to prevent inrush current during power-up. SS pin sources an internal 5μA current charging an external soft-start capacitor C_{SS} when EN pin exceeds turn-on threshold. The device uses the lower voltage between the internal voltage reference 1.2V and the SS pin voltage as the reference input voltage of error amplifier and regulates the output. The soft-start completes when SS pin voltage exceeds the internal 1.2V reference. Use equation 1 to calculate the soft-start time (10% to 90%). When EN pin is pulled low to disable the device, the SS pin will be discharged to ground.

$$t_{SS} = \frac{C_{SS} * V_{REF}}{I_{SS}} \quad (1)$$

where

- t_{SS} is the soft start time
- V_{REF} is the internal reference voltage of 1.2V
- C_{SS} is the capacitance connecting to SS pin
- I_{SS} is the source current of 5uA to SS pin

Adjustable Switching Frequency

The SCT12A2 features adjustable switching frequency from 200kHz to 1.0MHz.To set the switching frequency, an external resistor between SW pin and FSW pin is a must to guarantee the proper operation. Use Equation 2 or the curves in Figure 5 to determine the resistance for a given switching frequency. To reduce the solution size, one can typically set the switching frequency as higher as possible, but need to consider the tradeoff of the thermal dissipation and minimum on time of low-side power MOSFET.

$$R_{FREQ} = \frac{6 * (\frac{1}{f_{SW}} - T_{DELAY} * \frac{V_{OUT}}{V_{IN}})}{C_{FREQ}} \quad (2)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 90 ns
- C_{FREQ} = 34 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Adjustable Peak Current Limit

The SCT12A2 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 3 or Figure 6 to calculate the peak current limit.

$$I_{LIM} = \frac{1500}{R_{LIM}} \quad (3)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Load Disconnection Control

For both non-synchronous and synchronous boost converter, there is a non-fully controlled current path from converter input to output load through the diode or the high-side MOSFET body diode. During start up, once VIN is present, VOUT is moved to VIN level due to the direct path from input to output even when the device is shut down or the load is not ready. The presence of unwanted output voltage before system start up sequence could cause system to latch off or malfunction.

To address the above issues, the SCT12A2 provides a solution to insert an external P-channel MOSFET to disconnect the load from the converter output in application as shown in Figure 13. Choosing a lower R_{dson} of the disconnection P-channel MOSFET Q3 reduces impact on the efficiency. The source of Q3 needs connect to VOUT pin. Output capacitor is required at both VOUT pin and the source of P-channel MOSFET to maintain the loop stability.

In Figure 13, PGATE pin connecting to gate of Q3 has a constant sink current pulling down capability and a resistance pulling up capability. During SCT12A2 starting up, internal circuitry softly starts up of P-channel MOSFET. When gate-source voltage of external P-channel MOSFET is lower than the threshold voltage, the Q3 is turned on and the load is connected to VOUT pin. The source-gate voltage of external P-channel MOSFET is clamped up to 8V when the P-channel MOSFET is fully turned on.

When the Enable is disabled or the input voltage lower than the VIN UVLO threshold, the SCT12A2 shuts off the external P-channel MOSFET and disconnect the load

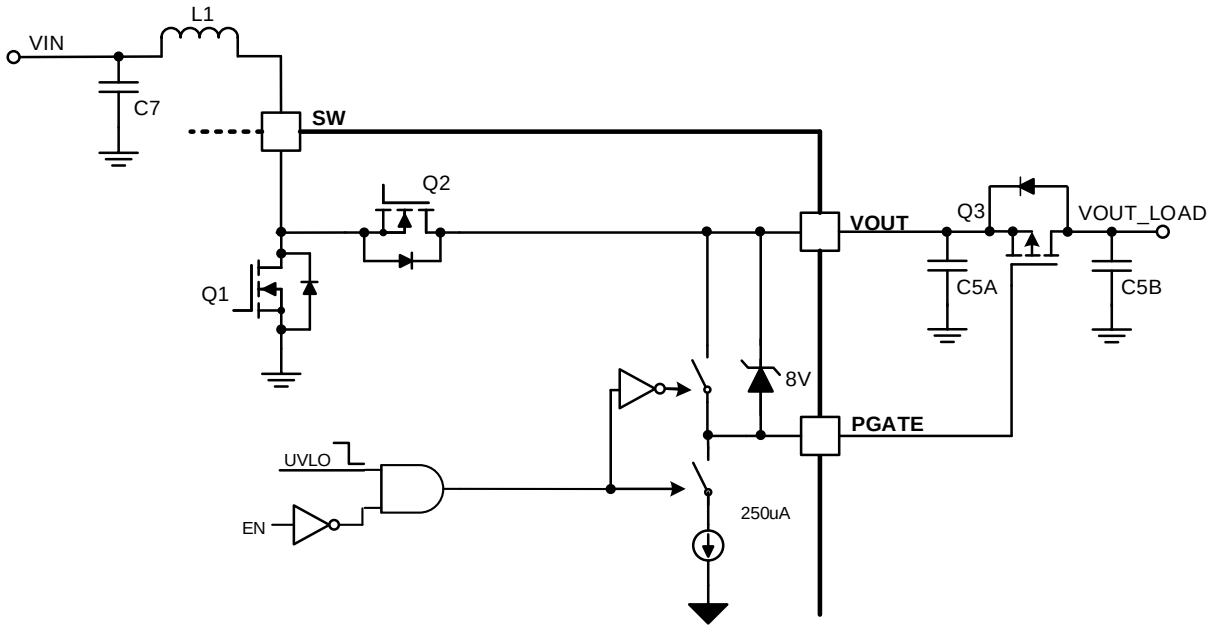


Figure 13. Load Disconnection Control

Over Voltage Protection and Minimum On-time

The SCT12A2 features both VOUT pin over voltage protection and the FB pin over voltage protection. If the VOUT pin is above 22V typical or FB pin voltage exceeds 1.32V typical, the device stops switching immediately until the VOUT pin drops below 21 V or FB pin voltage drops below 1.26V. The OVP function prevents the connected output circuitry from un-predictive overvoltage.

The low-side MOSFET has minimum on-time 160ns typical limitation. While the device is operating at minimum on time and further increasing Vin push output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

Pulse Frequency Modulation (PFM) Modes

Connecting MODE pin to ground, the SCT12A2 works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the load current decreasing, the COMP pin voltage decreases as resulting the inductor current down. With the load current further decreasing, the COMP pin voltage decreases and be clamped to a voltage corresponding to the ILIM/12. The converter extends the off time of high-side MOSFET Q2 to reduce the average delivered current to output. The switching frequency is lower and varied depending on loading condition. In PFM mode, the peak inductor current is fixed at around 1A and the output voltage is regulated 0.7% higher than the setting out put voltage. When the inductor current decreased to zero, zero-cross detection circuitry on high-side MOSFET Q2 forces the Q2 off until the beginning of the next switching cycle. The boost converter does not sink current from the load at light load.

Thermal Shutdown

Once the junction temperature in the SCT12A2 exceeds 150C, the thermal sensing circuit stops switching until the junction temperature falling below 125C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

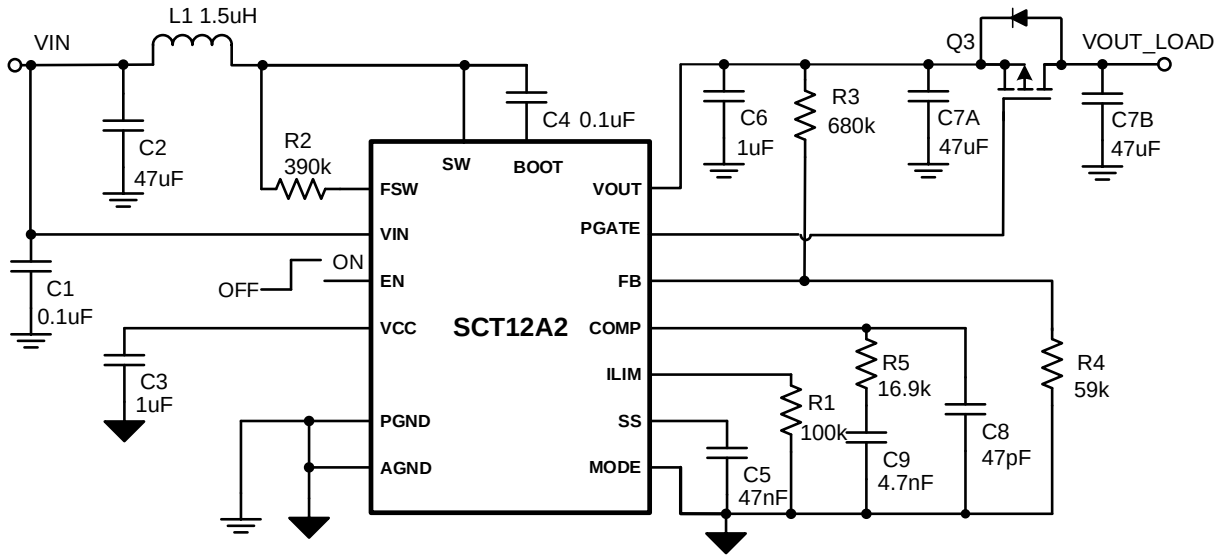


Figure 14. One Cell Battery Input, 15V Output with Load Disconnection Protection

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 14V
Output Voltage	15V
Output Current	2A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	400 kHz
Operation Mode	PFM

∗For description in the typical application section, the converter output before PMOS is specified as VOUT and the converter output after PMOS is specified as VOUT_LOAD in below.

Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

$$R_{FREQ} = \frac{6*(\frac{1}{f_{SW}} - T_{DELAY}*\frac{V_{OUT}}{V_{IN}})}{C_{FREQ}} \quad (3)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 90 ns
- C_{FREQ} = 34 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Table 1. R_{FSW} Value for Common Switching Frequencies (Vin=3.6V, Vout=15V, Room Temperature)

Fsw	R_{FSW}
230 KHz	680 KΩ
400 KHz	390 KΩ
575 KHz	270 KΩ
715 KHz	200 KΩ

Peak Current Limit

Using equation 4 the correct external resistor at ILIM pin sets the peak input current. For a typical current limit of 12A, the resistor value is 100KΩ. The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

$$I_{LIM} = \frac{1500}{R_{LIM}} \quad (4)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

Table 2. R_{LIM} Value for Inductor Peak Current (Vin=3.6V, Vout=15V, L=1.5uH, Room Temperature)

I_{LIM}	R_{LIM}
15 A	100 KΩ
10 A	150 KΩ
7.5A	200 KΩ

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 5.

$$R_3 = \frac{(V_{OUT} - V_{REF}) \times R4}{V_{REF}} \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.2V

Table 3. Feedback Resistor R_3R_4Value for Output Voltage (Room Temperature)

V_{OUT}	R_3	R_4
9 V	390 KΩ	59 KΩ
15 V	698 KΩ	59 KΩ

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance values reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as in equation 6

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 7

$$I_{LPP} = \frac{1}{L \times (\frac{1}{V_{OUT}-V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 8.

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \quad (8)$$

Set the current limit of the SCT12A2 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

The inductor's DC resistance (DCR), equivalent series resistance (ESR) at switching frequency and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. There is a tradeoff among the inductor's inductance, DCR and ESR resistance, and its footprint. Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT12A2. Verify whether the recommended inductor can support the

user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor SMD7443552150 is used on SCT12A2 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
WE-HCI SMD 7443552150	1.5	5.3	17 / 14	10.5 x 10.2 x 4.0	WurthElektronix

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT12A2. A ceramic capacitor of more than 1.0μF is required at the VCC pin to get a stable operation of the internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22μF or 47uF input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 9 and 10 to calculate the minimum required effective capacitance, C_{OUT}.

$$V_{ripple\_C} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (9)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times ESR \quad (10)$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

External P-channel MOSFET Selection

To minimize the power efficiency impact on the boost system, the external P-channel MOSFET with smaller R_{dson} is inserted between the converter output and load circuit to implement the load disconnection protection. The SCT12A2 provides the gate drive capability for the external P-channel MOSFET, the maximum V_{GS} of the P-channel MOSFET is clamped up to -7.1V typically if the VOUT is higher than 7.1V. Otherwise, the maximum V_{GS} follows the VOUT pin voltage in the application. As a result, the low R_{dson} and low threshold P-channel MOSFET is preferred. Table 5 shows the recommended P-channel MOSFET details.

Table 5. Recommended External P-channel MOSFET

Part Number	R_{dson} (mΩ)	I_D (A)	Max V_{DS} (V)	Max V_{GS} (V)	Vendor
FDMC612PZ	8.4	14	-20	±12	Fairchild
CSD25404Q3	5.5	18	-20	±12	Texas Instruments

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C8 and C9 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

$$G_{PS}(S) = \frac{R_{load} \times (1-D)}{2 \times R_{SENSE}} \times \frac{(1+\frac{S}{2\pi \times f_{ESRZ}})(1+\frac{S}{2\pi \times f_{RHPZ}})}{1+\frac{S}{2\pi \times f_P}} \quad (11)$$

where

- D is the switching duty cycle.
- R_{load} is the output load resistance.
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.08 Ω.

$$f_P = \frac{1}{2\pi \times R_{load} \times C_O} \quad (12)$$

where

- C_O is the output capacitance

$$f_{PESRZ} = \frac{1}{2\pi \times ESR \times C_O} \quad (13)$$

where

- ESR is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_{load} \times (1-D)^2}{2\pi \times L} \quad (14)$$

The COMP pin is the output of the internal trans-conductance amplifier. Equation 15 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1+\frac{S}{2\pi \times f_{COMZ}})}{(1+\frac{S}{2\pi \times f_{COMP1}})(1+\frac{S}{2\pi \times f_{COMP2}})} \quad (15)$$

where

- G_{EA} is the amplifier's trans-conductance
- R_{EA} is the amplifier's output resistance
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C . The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW} , or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R5, C8, and C9 in typical application circuit by following these equations.

$$R_5 = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times f_C \times C_O}{(1-D) \times V_{REF} \times G_{EA}} \quad (16)$$

where

- f_C is the selected crossover frequency.

$$C_8 = \frac{R_{load} \times C_O}{2 \times R_5} \quad (17)$$

$$C_9 = \frac{ESR \times C_O}{R_5} \quad (18)$$

If the calculated value of C9 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

Test Condition: VIN=7.2V, VOUT=15V, T_a=27° C.

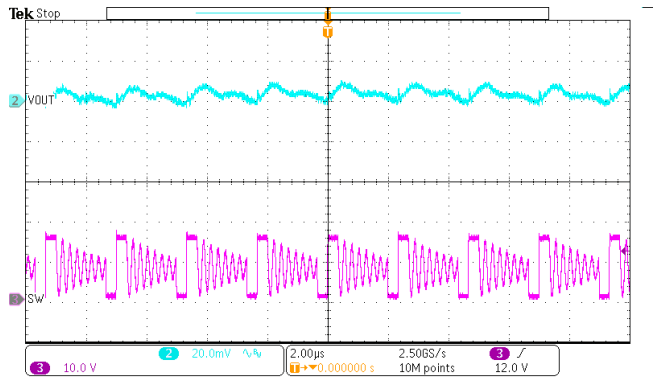


Figure 15. Switching Waveforms and Output Ripple
(Vout=15V, Iout=100mA)

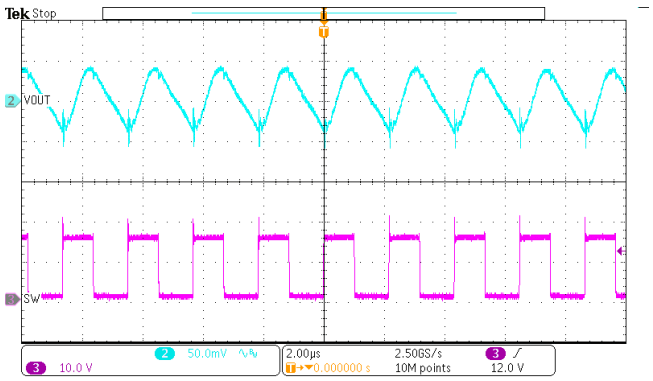


Figure 16. Switching Waveforms and Output Ripple
(Vout=15V, Iout=2A)

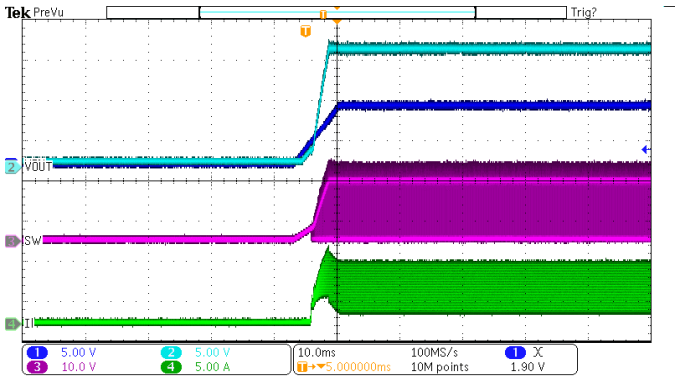


Figure 17. Power up (Vout=15V, Iout=2A)

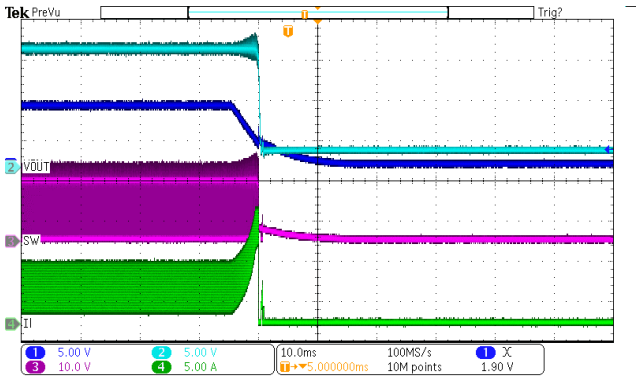


Figure 18. Power Down (Vout=15V, Iout=2A)

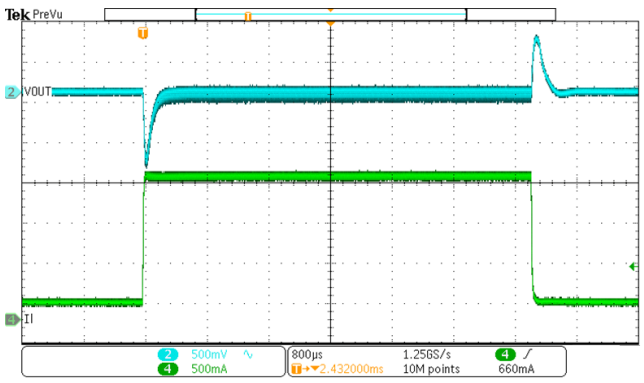


Figure 19. Load Transient
(Vout=15V, Iout=0.2A to 1.8A, SR=250mA/us)

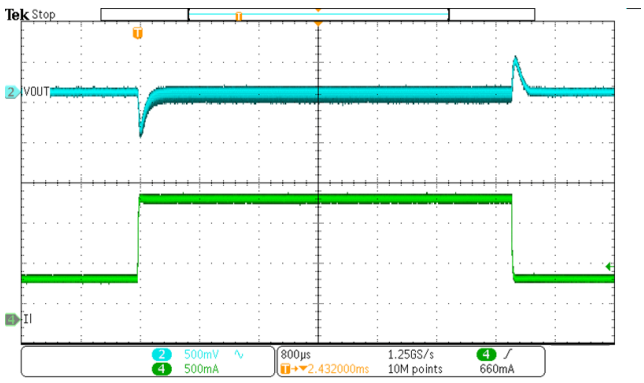


Figure 20. Load Transient
(Vout=15V, Iout=0.5A to 1.5A, SR=250mA/us)

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple. The placement and ground trace for C6 is critical for the performance of SW ringing voltage. Place capacitor C6 as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias (≤8mil) underneath the thermal pad. The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias. Since thermal pad is electrical power ground of the device, improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

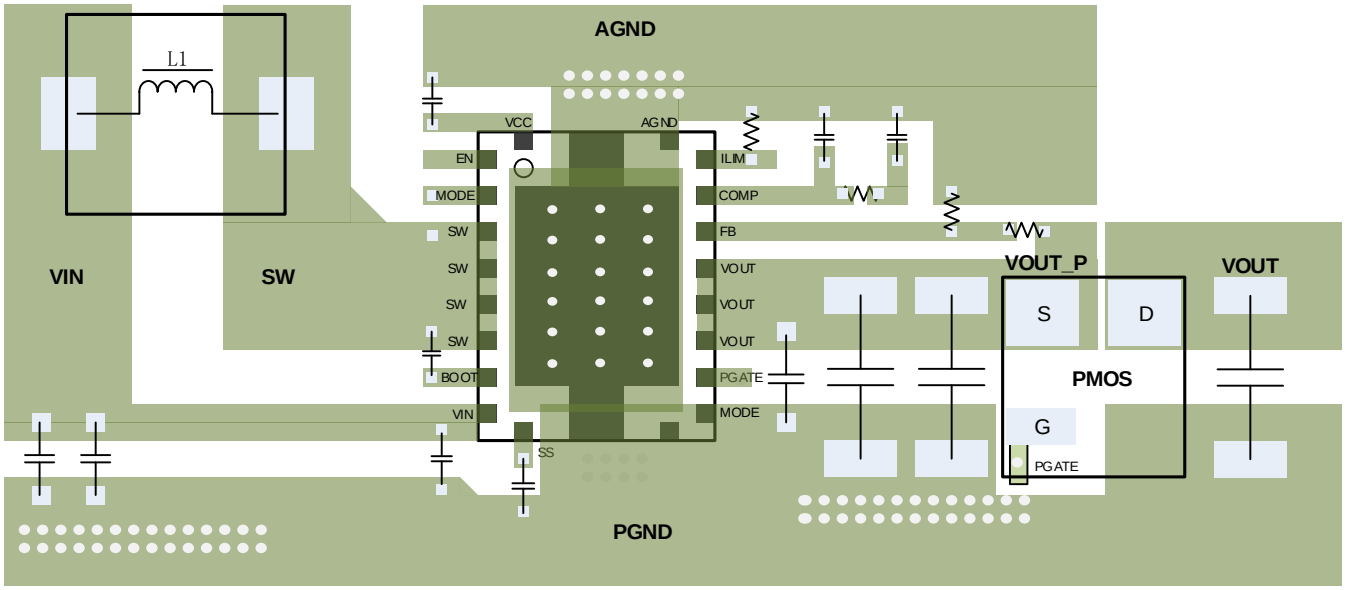


Figure 21. PCB Layout Example Top Layer

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

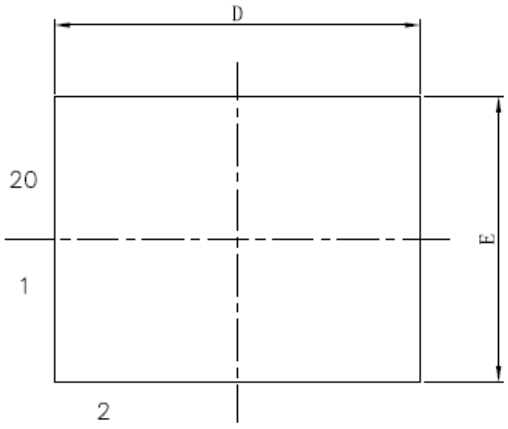
$$P_{D(MAX)} = \frac{125 - TC_A}{R_{\theta JA}} \quad (19)$$

where

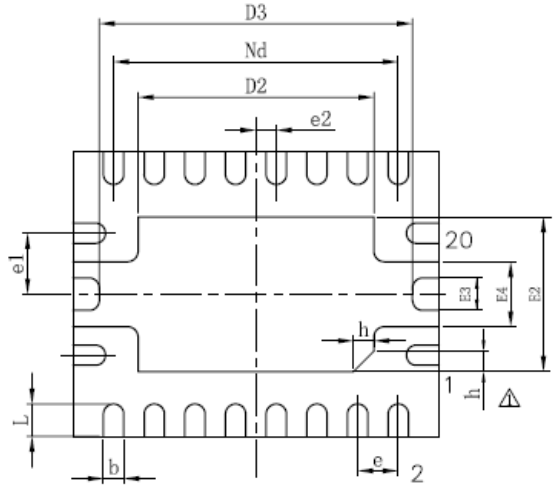
- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT12A2 DFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

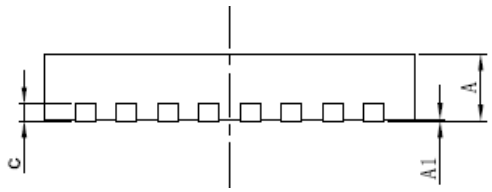
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

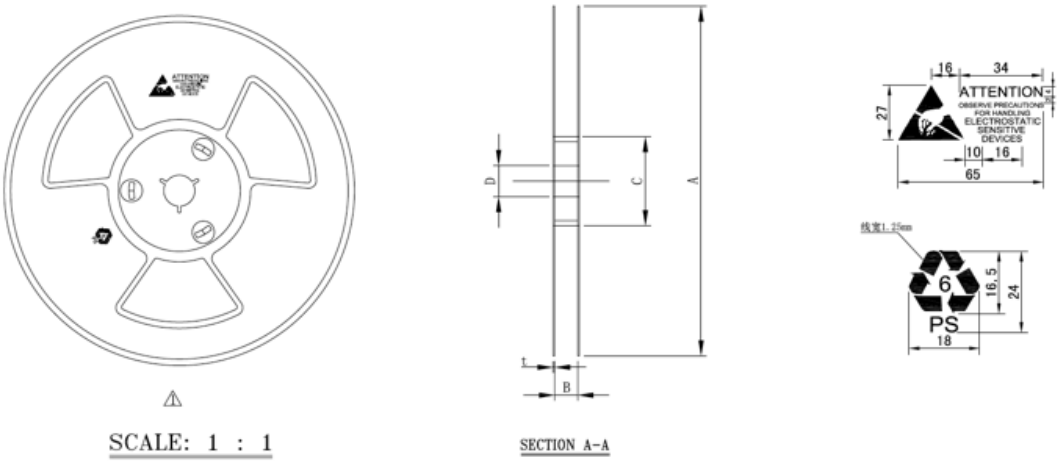
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.85	0.9	0.95
A1	——	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.40	4.50	4.60
D2	3.10	3.20	3.30
D3		3.85REF	
e		0.50BSC	
e1		0.75BSC	
e2		0.25BSC	
Nd		3.50BSC	
E	3.40	3.50	3.60
E2	2.10	2.20	2.30
E3		0.35REF	
E4		0.75REF	
L	0.35	0.40	0.45
h	0.20	0.25	0.30

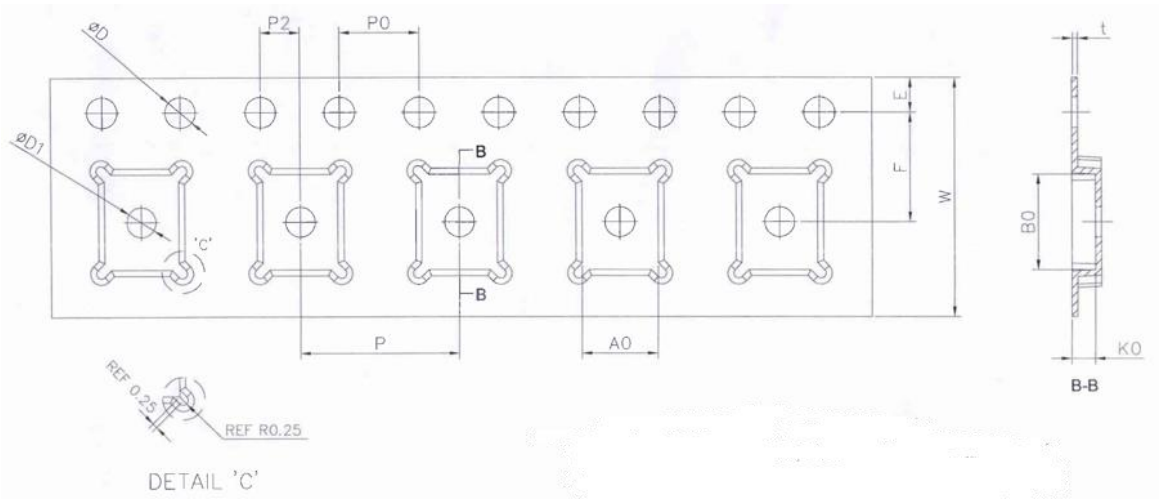
TAPE AND REEL INFORMATION

Device	Package Type	Pins	SPQ
SCT12A2DHKR	DFN	20	3000



REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TYPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
12±0.30	3.80±0.10	4.80±0.10	1.18±0.10	0.30±0.05	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.10	2.00±0.10	1.55±0.10	1.50MIN	4.00±0.10	40.0±0.20

RELATED PARTS

PART NUMBERS	DESCRIPTION	COMMENTS
SCT12A3	15-A Fully-integrated Synchronous Boost Converter	Vin=2.7V-20V, 15A switch peak current with load disconnection control and AAO
SCT12A0	12-A Fully-integrated Synchronous Boost Converter	Vin=2.7V-14V, 12A switch peak current without load disconnection control
SCT12A1	12-A Fully-integrated Synchronous Boost Converter with load disconnection	Vin=2.7V-14V, 12A switch peak current with load disconnection control

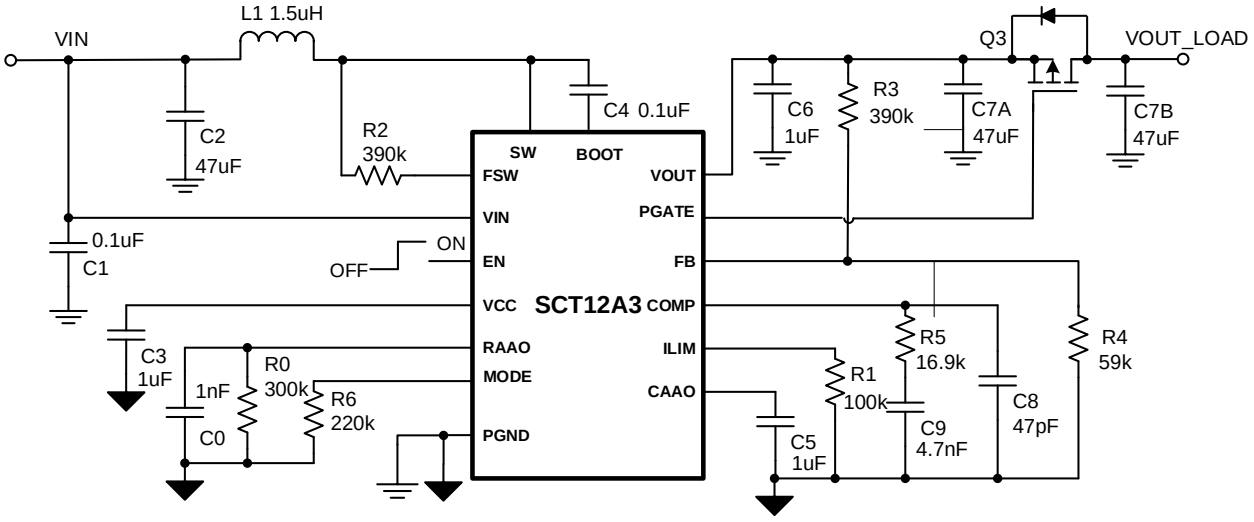


Figure 22. SCT12A3 Typical Application

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