NVD5117PL

MOSFET – Power, Single, P-Channel
-60 V, 16 mΩ, -61 A

ON Semiconductor®

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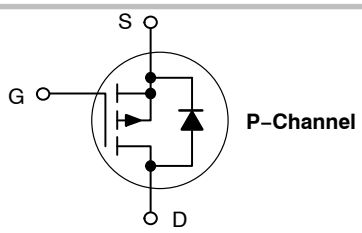
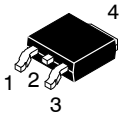
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
−60 V	16 mΩ @ −10 V	−61 A
	22 mΩ @ −4.5 V	

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC−Q101 Qualified
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant





DPAK
CASE 369C
STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	−61	A
		T_C = 100°C		−43	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	118	W
		T_C = 100°C		59	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 2)	Steady State	T_A = 25°C	I_D	−11	A
		T_A = 100°C		−8	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	4.1	W
		T_A = 100°C		2.1	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	−419	A
Current Limited by Package (Note 3)	T_A = 25°C		$I_{Dmaxpkg}$	60	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	−118	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, $I_{L(pk)}$ = 40 A, L = 0.3 mH, R_G = 25 Ω)			E_{AS}	240	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

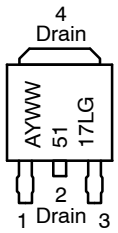
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Drain)	$R_{\theta JC}$	1.3	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	37	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5117L = Device Code
G = Pb−Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

ORDERING INFORMATION

Device	Package	Shipping†
NVD5117PLT4G	DPAK (Pb−Free)	2500 / Tape & Reel
NVD5117PLT4G−VF01	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −60 V	T_J = 25°C			−1.0	μA
			T_J = 125°C			−100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1.5		−2.5	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −29 A			12	16	mΩ
		V_{GS} = −4.5 V, I_D = −29 A			16	22	
Froward Transconductance	g_{FS}	V_{DS} = −15 V, I_D = −15 A			30		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −25 V			4800		pF
Output Capacitance	C_{oss}				480		
Reverse Transfer Capacitance	C_{rss}				320		
Total Gate Charge	$Q_{G(TOT)}$	V_{DS} = −48 V, I_D = −29 A	V_{GS} = −4.5 V		49		nC
			V_{GS} = −10 V		85		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = −4.5 V, V_{DS} = −48 V, I_D = −29 A			3		
Gate−to−Source Charge	Q_{GS}				13		
Gate−to−Drain Charge	Q_{GD}				28		
Plateau Voltage	V_{GP}				3.2		V
SWITCHING CHARACTERISTICS (Notes 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −48 V, I_D = −29 A, R_G = 2.5 Ω			22		ns
Rise Time	t_r				195		
Turn−Off Delay Time	$t_{d(off)}$				50		
Fall Time	t_f				132		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −29 A	T_J = 25°C		−0.86	−1.0	V
			T_J = 125°C		−0.74		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_s = −29 A			36		ns
Charge Time	t_a				19		
Discharge Time	t_b				17		
Reverse Recovery Charge	Q_{RR}				44		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

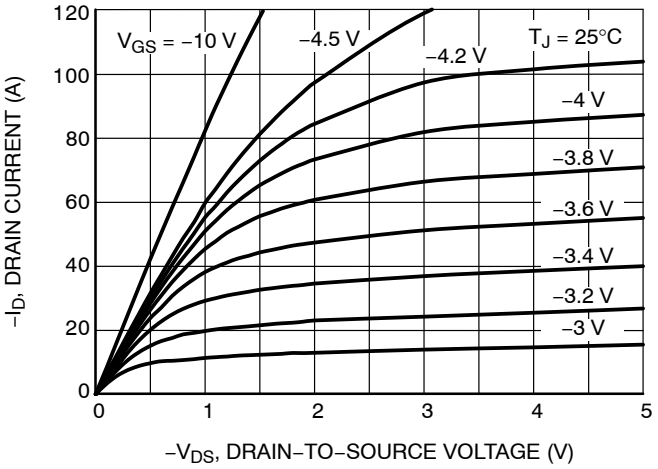


Figure 1. On−Region Characteristics

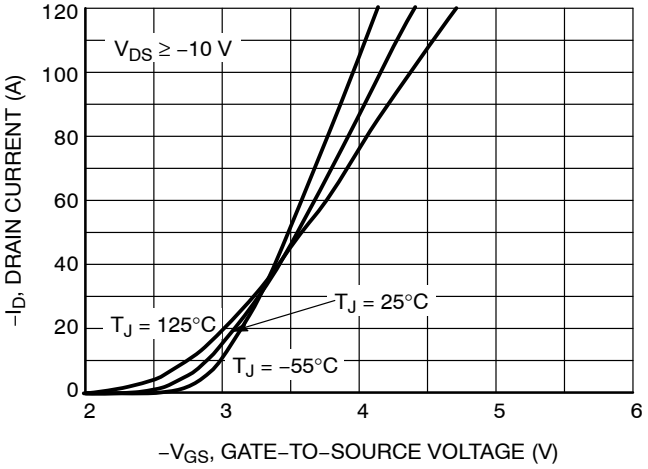


Figure 2. Transfer Characteristics

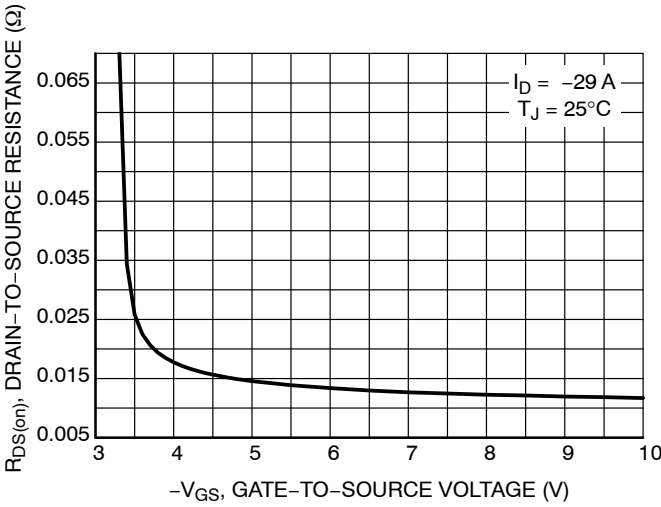


Figure 3. On−Resistance vs. Gate−to−Source Voltage

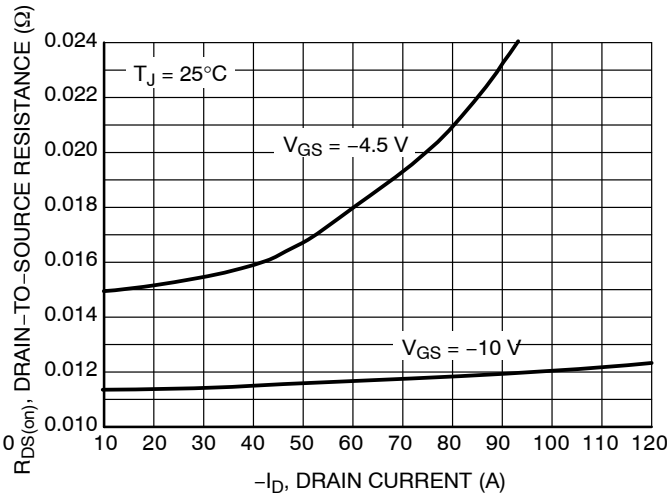


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

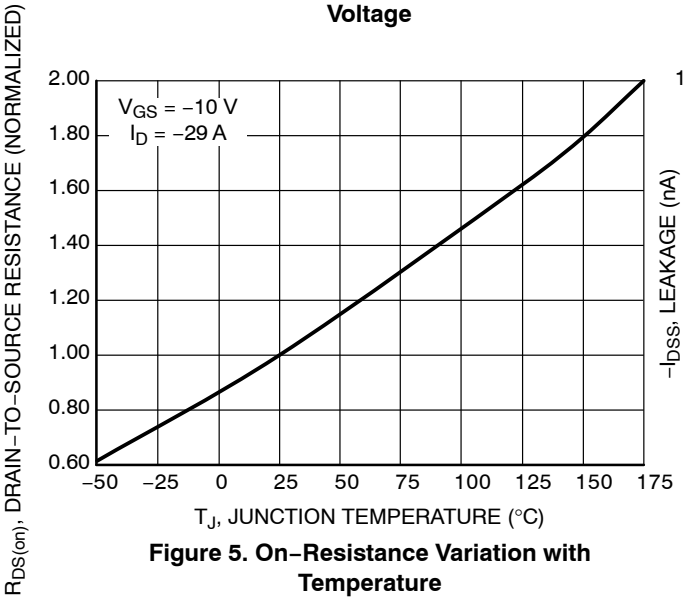


Figure 5. On−Resistance Variation with Temperature

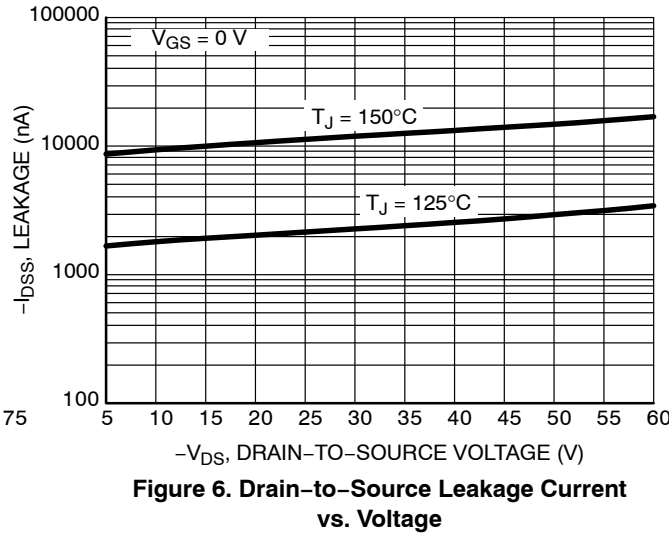


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

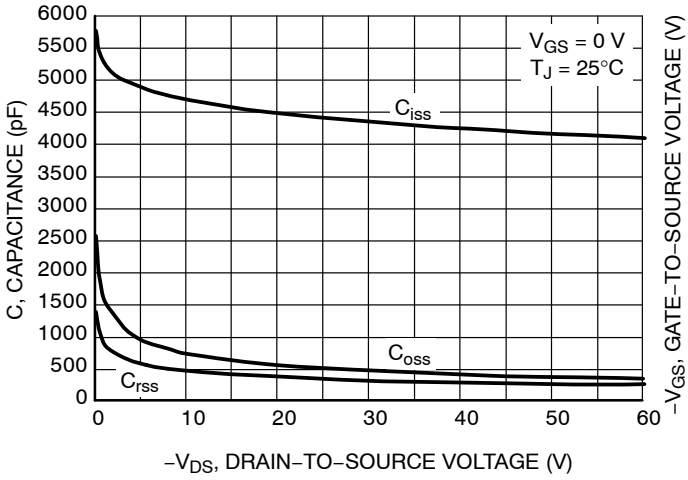


Figure 7. Capacitance Variation

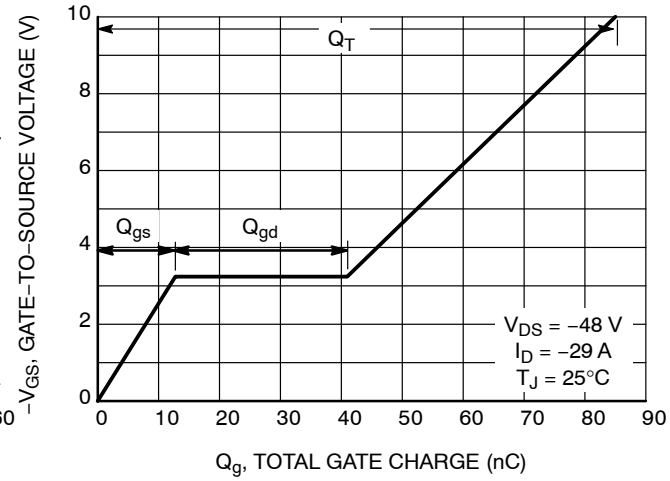


Figure 8. Gate−to−Source vs. Total Charge

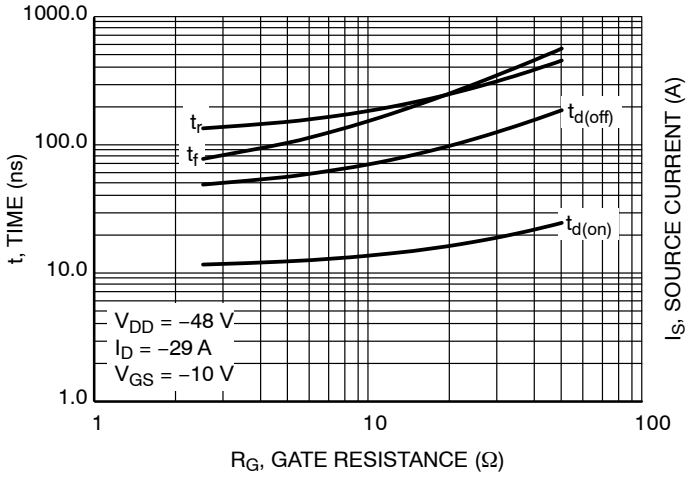


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

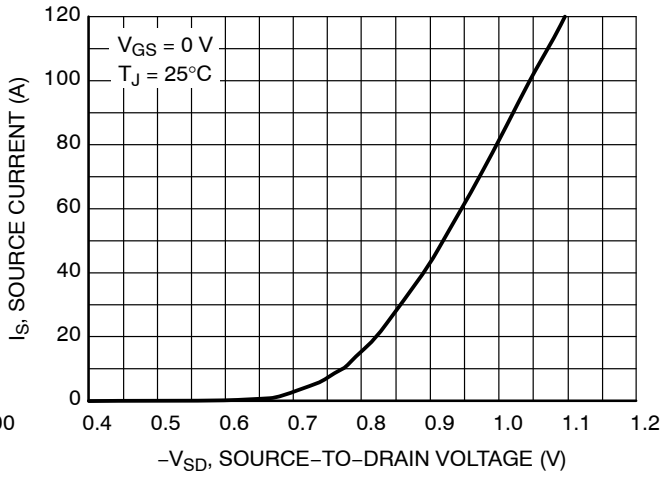


Figure 10. Diode Forward Voltage vs. Current

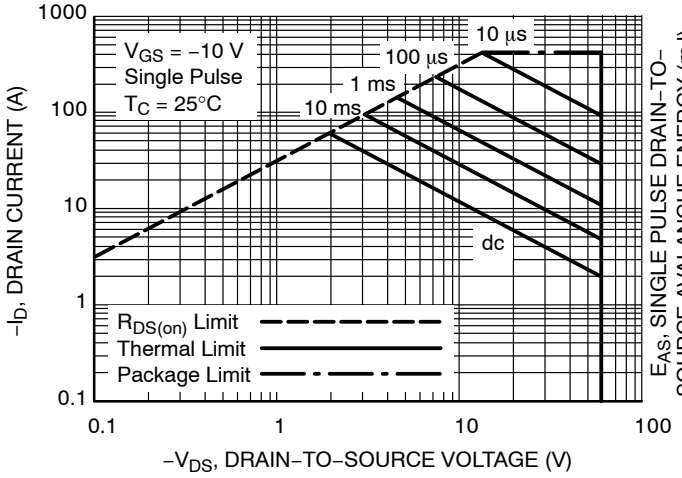


Figure 11. Maximum Rated Forward Biased Safe Operating Area

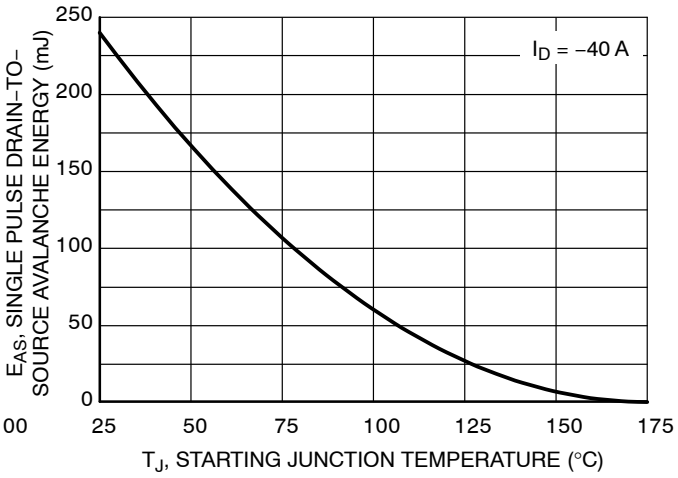


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

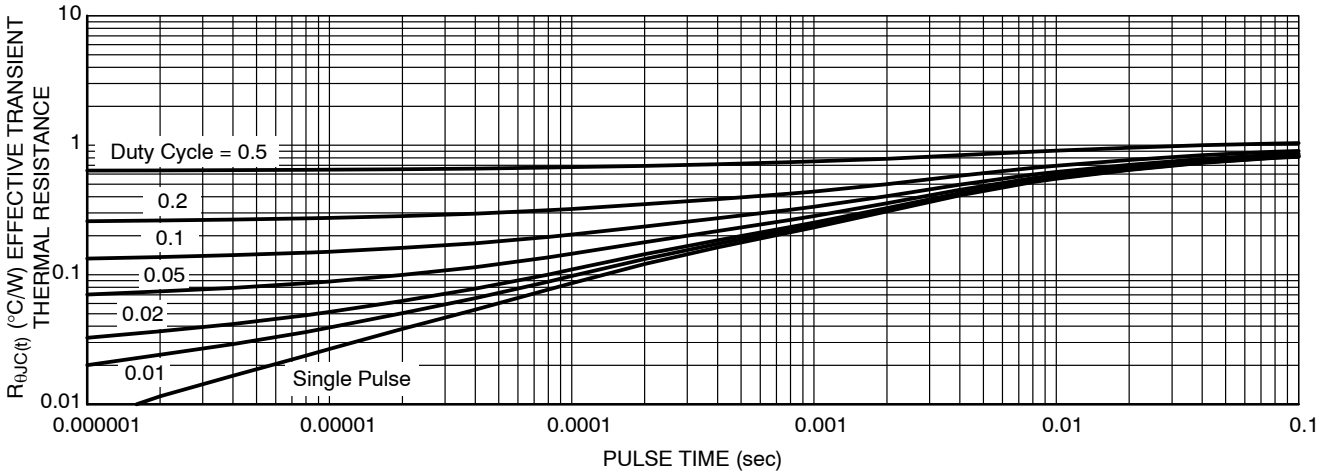
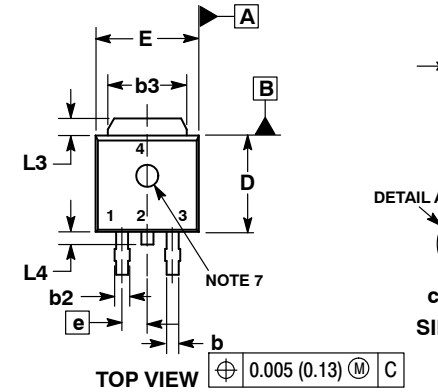


Figure 13. Thermal Response

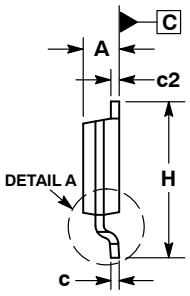
PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

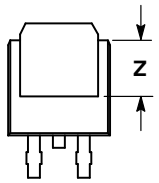


TOP VIEW

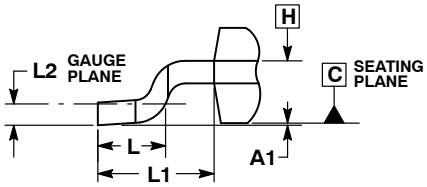
⊕	0.005 (0.13) Ⓜ	C



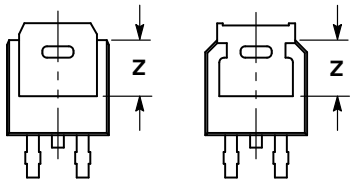
SIDE VIEW



BOTTOM VIEW



DETAIL A
ROTATED 90° CW

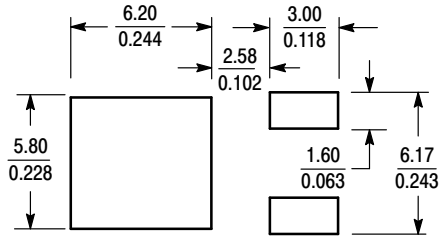


BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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