



P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
- 30	0.012 at V _{GS} = - 10 V	- 11.4			
	0.019 at V _{GS} = - 4.5 V	- 9.1			

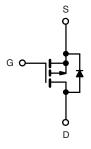
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Advanced High Cell Density Process
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- · Load Switches
 - Notebook PCs
 - Desktop PCs



P-Channel MOSFET

		SO-8		
S			8	D
s	2		7	D
S	3			D
G	3		6	D
G	4		5	D
		Top View		

Ordering Information: Si4425BDY-T1-E3 (Lead (Pb)-free)

Si4425BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	1A - 23 O, unite	1	1	1	
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	- 30		V
Gate-Source Voltage		V _{GS}	± 20		V
O	T _A = 25 °C	I _D	- 11.4	- 8.8	^
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		- 9.1	- 7.0	
Pulsed Drain Current		I _{DM}	- 50		Α
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.1	- 1.3	
Mariana Barra Biratina	T _A = 25 °C	P _D	2.5	1.5	W
Maximum Power Dissipation ^a	T _A = 70 °C	l D	1.6	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55	to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana haratina ta Analianta	t ≤ 10 s	R_{thJA}	40	50	°C/W
Maximum Junction-to-Ambient ^a	Steady State		70	85	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	15	18	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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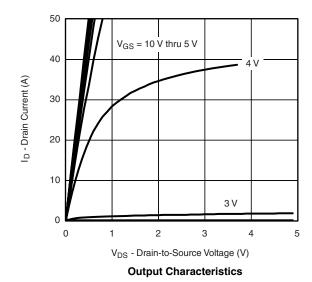
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1.0		- 3.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Drain Current		V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μА	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 50			Α	
	D	V _{GS} = - 10 V, I _D = - 11.4 A		0.010	0.012		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 9.1 A		0.015	0.019	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 11.4 A		29		S	
Diode Forward Voltage ^a	V _{SD}	I _S = - 2.5 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			64	100		
Gate-Source Charge	Q_{gs}	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 11.4 A		11		nC	
Gate-Drain Charge	Q _{gd}			17		1	
Turn-On Delay Time	t _{d(on)}			15	25		
Rise Time	t _r	V_{DD} = - 15 V, R_L = 15 Ω		13	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 6 Ω		100	150	ns	
Fall Time	t _f			53	80		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 2.5 A, dI/dt = 100 A/μs		41	80		

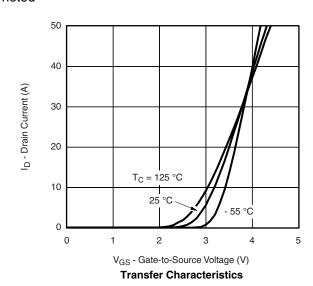
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

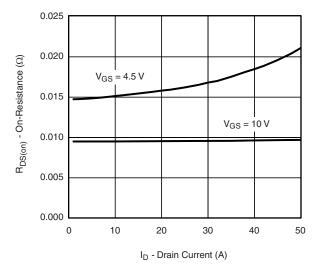




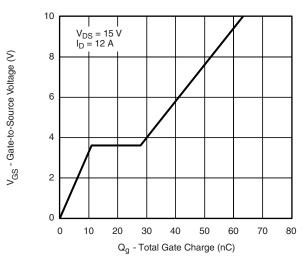




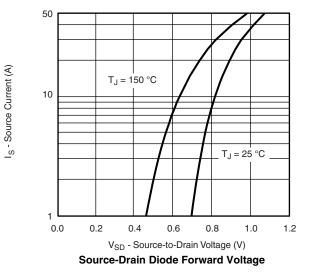
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Drain Current



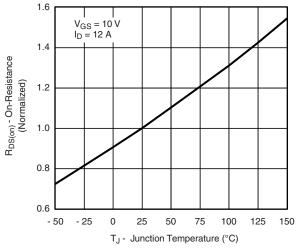
Gate Charge



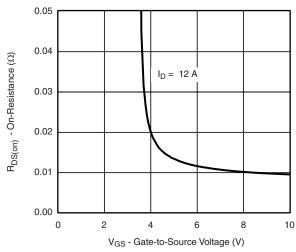
5000 4000 4000 C_{iss} 3000 2000 1000 C_{rss} 0 6 12 18 24 30

V_{DS} - Drain-to-Source Voltage (V)





On-Resistance vs. Junction Temperature

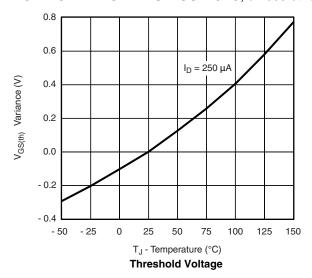


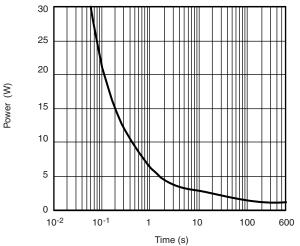
On-Resistance vs. Gate-to-Source Voltage

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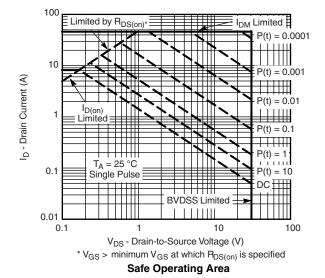
VISHAY

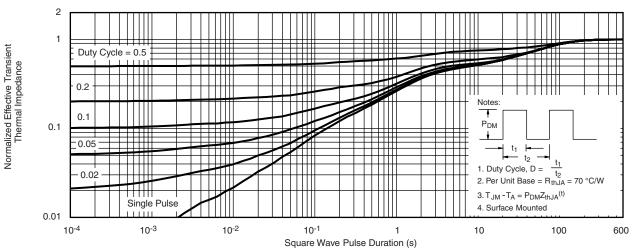
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





Single Pulse Power, Junction-to-Ambient

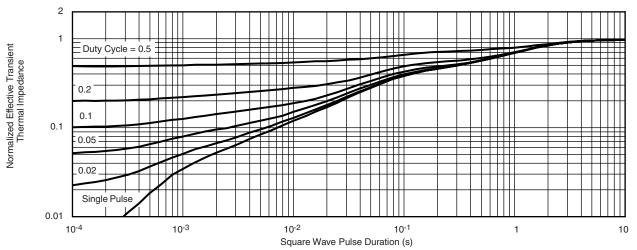




Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

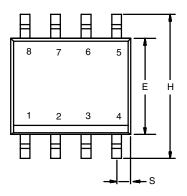


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg272000.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC		0.050 BSC	
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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