Dual Channel Output LCD Bias Power

Description

The FP7720 boost converter PMU is designed for TFT-LCD panel application and support bias power positive AVDD / negative AVEE output that connected to the Source Driver IC.

The FP7720 uses current mode, fixed frequency of approximately 1MHz architecture to regulate output voltage and goes automatically into PSM mode at light load. Besides the converter includes a N-channel MOSFET switch and P-channel synchronous rectifier. So no external Schottky diode is required and could get better efficiency near 85%.

Other features include current limit protection, thermal shutdown protection and under-voltage lockout (UVLO). The FP7720 is available in a space saving CSP 15-ball (0.4mm ball pitch) package.

Features

- Output Current up to 80mA
- Wide V_{IN} Range: 2.5V to 5.5V
- Up to 85% Efficiency
- AVDD Output Voltage+5.1V & +5.5V
- AVEE Output Voltage -5.1V & -5.5V
- High Frequency Operation: 1MHz
- ENP/ENN Power on Sequence Control.
- Built-in Soft Start and Over-Temperature Protection
- Over-Current Protection
- Power-Save Mode for Light-Load Efficiency.
- Space Saving CSP-15 ball (1.4mm x 2.3mm) Package

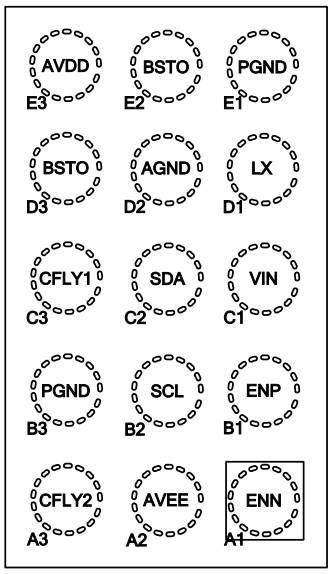
Applications

- TFT LCD Smartphone
- TFT LCD Tablets
- White Brand MID

Pin Assignments

E9 Package 15-Bump (1.4 mm x 2.3 mm x 0.6 mm)

Top View



Ordering Information

FP7720□□

Package Type
E9: WLCSP-15 (1.4mmX2.3mm)

Output Voltage
B : ±5.1V
F : ±5.5V

Typical Application Circuit

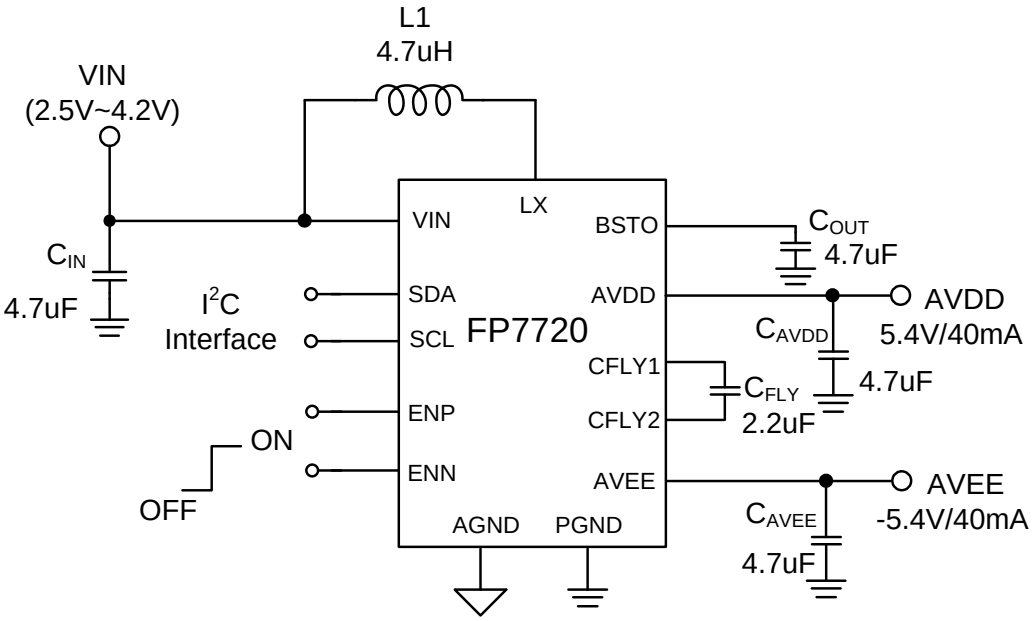


Figure 2. Typical Application Circuit of FP7720

Functional Pin Description

Pin Name	I/O	CSP pin	Pin Function
ENN	I	A1	Logic control shutdown input for AVEE power control.
AVEE	O	A2	Negative voltage output from -4V to-6V.
CFLY2	I	A3	Negative input for the external flying capacitor. Connect a ceramic 2.2μF capacitor close to the pins of the IC
ENP	I	B1	Logic controlled shutdown input for AVDD power control.
SCL	I/O	B2	I^2C interface clock signal. (This pin is for production test only, no connection)
PGND	P	B3,E1	Boost converter power ground.
VIN	P	C1	Input supply pin. Decouple with 4.7μF ceramic capacitor close to the pin.
SDA	I/O	C2	I^2C interface data signal. (This pin is for production test only, no connection)
CFLY1	I	C3	Positive input for the external flying capacitor. Connect a ceramic 2.2μF capacitor close to the pins of the IC
LX	P	D1	Power switching output. Connect an external inductor to this switching node.
AGND	P	D2	Analog ground. Control circuitry returns current to this pin.
BSTO	O	D3,E2	Output of the synchronous rectifier. Decouple with an external capacitor. At least 4.7μF is recommended. Higher capacitor values reduce output ripple.
AVDD	O	E3	Positive voltage output. +4V~+6V

Block Diagram

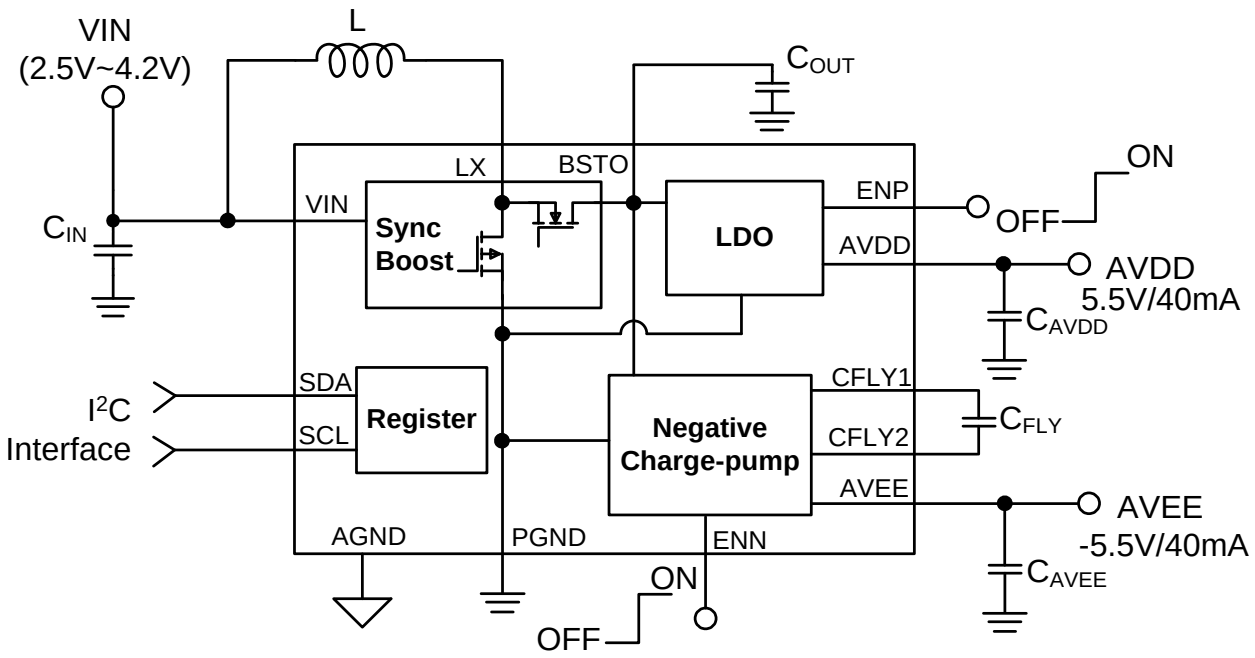


Figure 3. Block Diagram of FP7720

Absolute Maximum Ratings (Note1)

- Supply Voltage V_{IN}, V_{CFLY1} ---------- -0.3V to +7V
- Positive Output Voltage (V_{BSTO}), AVDD---------- -0.3V to +7V
- Negative Output Voltage AVEE, V_{CFLY2} ---------- +0.3V to -7V
- LX Voltage V_{LX} ---------- -0.3V to +10V
- SDA,SCL Voltage ---------- -0.3V to +7V
- Junction Temperature (T_J) ---------- +150°C
- Operating Temperature (T_{OP}) ---------- -40°C to +85°C
- Storage Temperature (T_{STG}) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C

Note 1：Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage V_{IN} ---------- +2.5V to +5.5V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{IN} =3.7V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage	V_{IN}		2.5		5.5	V
V_{IN} Supply Current (IC Switching)	Iq	V_{IN}=3.7V, no load Measure V_{IN}		1	2	mA
		V_{IN}=3.7V, ENN=ENP=Low Measure V_{IN}		5		uA
High-Side MOSFET Leakage Current	$I_{LX(leak)}$	V_{LX}=6.5V, V_{BSTO}=0V			10	μA
Low-Side MOSFET Leakage Current		V_{LX}=6.5V			10	μA
Oscillation Frequency	F_{OSC}		800	1000	1200	kHz
Maximum Duty Cycle	D_{MAX}	V_{IN}=3.7V		90		%
Switch Current Limit		V_{IN} = 3.7V		1.5		A
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{IN} rising	2.1	2.3	2. 5	V
Under Voltage Lockout Threshold Hysteresis	$V_{UVLO(HYS)}$	V_{IN} falling		200		mV
Thermal Shutdown Threshold (Note 2)	T_{SD}			160		°C
Thermal Shutdown Hysteresis				30		°C
Output Voltage AVDD						
Output Voltage AVDD Range	V_{AVDD}	21 steps, each step=100mV	4		6.0	V
Output Voltage AVDD Accuracy		No load	-1.5		+1.5	%
Output current capability	I_{AVDD}		80			mA
Dropout voltage		V_{AVDD}=5.4V, I_{AVDD}=150mA		160		mV
Load Regulation		I_{AVDD}=10 to 100mA, AVDD=5V		0.5		%
Line Regulation		VIN=2.5V to 4.2V, AVDD=5V, I_{AVDD}=40mA		1		%
AVDD Discharge resistor	R_{AVDD}			70		Ω
ENP Input Low Voltage	$V_{ENP\ (L)}$				0.5	V
ENP Input High Voltage	$V_{ENP\ (H)}$		1.5			V
Enable Pulldown Resistor	R_{ENP}			300		kΩ
Output Voltage AVEE						
Output Voltage AVEE Range	V_{AVEE}	21 steps, each step=100mV	-4		-6.0	V
Output Voltage AVEE Accuracy		No load	-1.5		+1.5	%
Output current capability	I_{AVEE}				-80	mA
UVP Threshold Voltage on AVEE Pin		V_{AVEE} falling under target percentage		80		%
Charge pump Switching Frequency	$F_{OSC-AVEE}$		400	500	600	kHz
Load Regulation		I_{AVEE}=-10 to -100mA, AVEE=-5V		0.5		%
Line Regulation		VIN=2.5V to 4.2V, AVEE=-5V, I_{AVEE}=-40mA		1		%

Electrical Characteristics (Continued)

(V_{IN} =3.7V, T_A=25°C, unless otherwise specified)

AVEE Discharge resistor	R_{AVEE}			20		Ω
ENN Input Low Voltage	$V_{ENN\ (L)}$				0.5	V
ENN Input High Voltage	$V_{ENN\ (H)}$		1.5			V
Enable Pulldown Resistor	R_{ENN}			300		kΩ

Note 2：Not production tested.

Power On/ Off Sequence

ENP / ENN Control

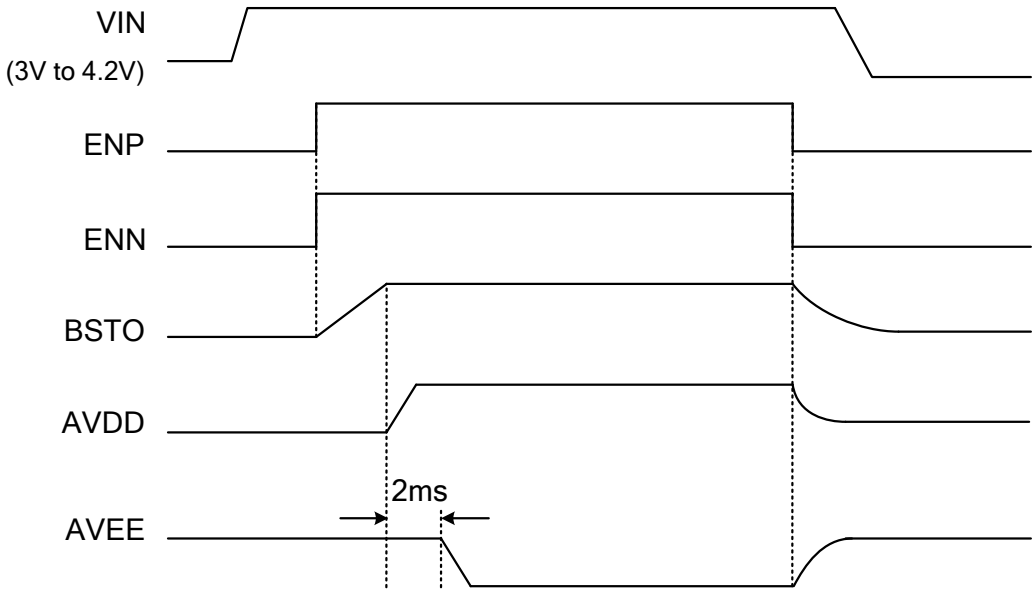


Figure 4. ENP/ENN Control

Independent ENP / ENN Control

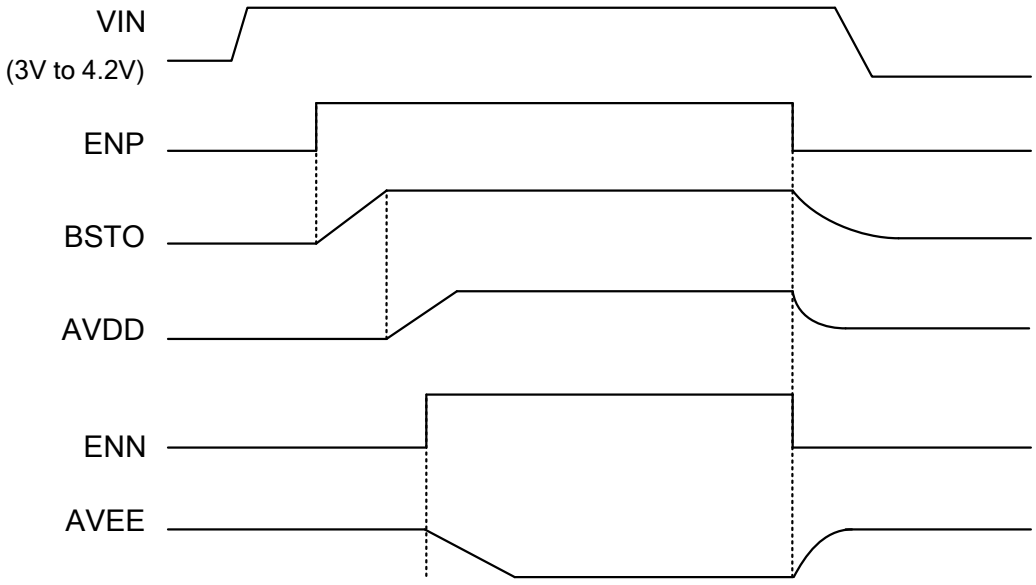


Figure 5. Independent ENP / ENN Control

Application Information

The FP7720 is a dual channel power supply for LCD panel. It contains a boost, a LDO and a negative charge pump. The output voltage of boost converter is BSTO. The LDO generates the positive voltage (AVDD) by regulating down BSTO. The negative charge pump generates the negative voltage VNEG by regulating the BSTO.

Under Voltage Lockout (UVLO)

When the FP7720 is power on, the internal circuits will be held inactive until VIN voltage exceeds the UVLO threshold voltage. And all outputs will be disabled when VIN is below the input UVLO threshold voltage.

Control Sequencing

The LDO (AVDD) and the negative charge pump (AVEE) are enabled and disable by external enable signal. ENP is for AVDD and ENN is for AVEE.

Boost Converter

The FP7720 integrates a PWM synchronous boost converter operating with current mode control. Switching frequency is 1MHz (typ.). The device is designed for high efficiency over wide output current range. Even at light load, the efficiency stays high because the switching losses of the converter are minimized by effectively reducing the switching frequency. The controller will enter a power saving mode if certain conditions are met. In this mode, the controller only switches on the transistor if the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses, and goes again into PSM mode once the output voltage exceeds a set threshold voltage.

Power OFF and Discharge

When VIN is below UVLO or ENP / ENN becomes low, boost converter and AVDD / AVEE turns off. When ENP / ENN go low, AVDD / AVEE will be discharged to GND.

Over Temperature Protection

The FP7720 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the protection temperature 160°C (typ.), all outputs will stop operation. As soon as IC cool down, outputs will re-start.

Layout Consideration

The proper PCB layout and component placement are critical for all switching regulators. The careful attention should be taken to the high-frequency, high current loops to prevent electromagnetic interference (EMI) problems. Here are some suggestions to the layout of FP7720 design.

a. The input capacitor should be located as closed as possible to the VIN and ground plane.

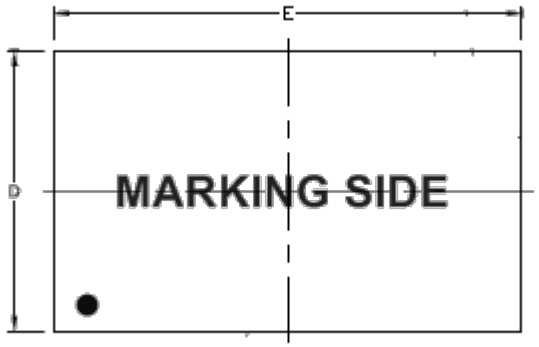
b. Minimize the distance of all traces connected to the LX node. The external components, COUT and L1 should be placed as close to the device as possible with short and wide route to obtain optimum efficiency.

c. The ground terminal of COUT must be located as closed as possible to ground plane.

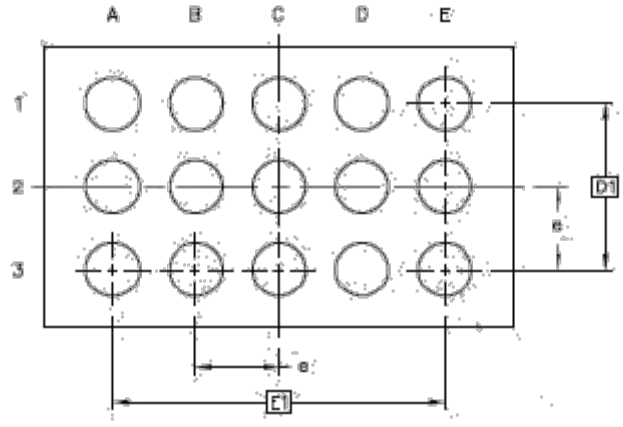
d. The CFLY should be placed close to CFLY1 and CFLY2 pins.

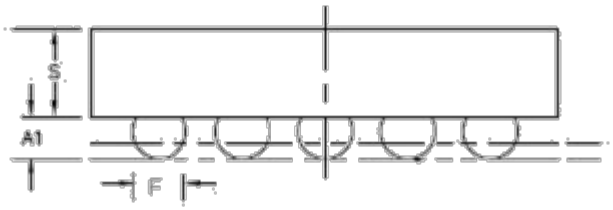
Outline Information

WLCSP-15 ball Package (1.38x2.28) pitch 0.4 (Unit: mm)

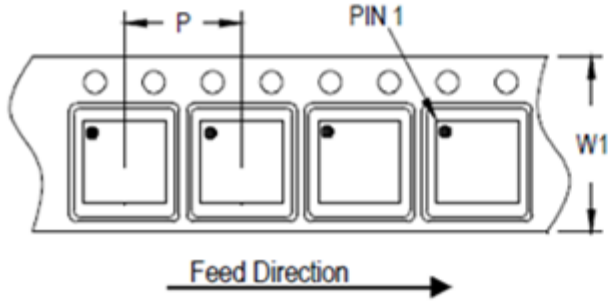


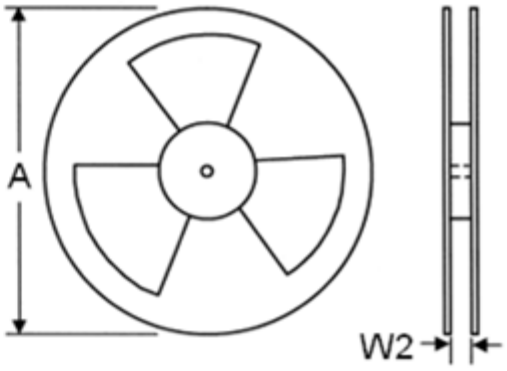
SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
D	1.310	1.380
E	2.210	2.280
S	0.400	0.450
D1	0.750	0.850
E1	1.550	1.650
A1	0.170	0.230
F	0.225	0.275
e	0.4	





Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	400~1000	3,000

Datasheet Revision History

Version	Date	Item	Description
0.1	2015/2/17		First edition
0.2	2015/3/11	Power On/ Off Sequence	Modify
0.3	2015/3/25	Electrical Characteristics	Modify
0.4	2015/5/12	Description Feature Functional Pin Description Electrical Characteristics Power On/ Off Sequence Application Information	Modify
0.5	2015/6/8	Description Feature Pin Assignments Ordering Information Functional Pin Description Outline Information	Modify

IC Revision History

Version	Date	Item	Description
0.1	2015/2/26		New version
0.2	2015/3/25	The compensation of boost converter VSN delay time from 256us to 2ms	Modify