DESCRIPTION

The devices are full bridge drivers to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +600 V. The six independent drivers are controlled at the low-side using CMOS and LSTTL compatible signals, down to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic and over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut down of all six switches. An error signal is provided at the $\overline{\text{FAULT}}$ open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. Therefore, the resistor R_{RCIN} is optional. The typical output current can be given with 200mA for pull-up and 400mA for pull down. Because of system safety reasons a 0.29us dead time has been realized. The function of inputs EN and ITRIP can optionally be extended with over-temperature detection, using an external NTC resistor, diodes and resistor network.

FEATURES

- Drives up to six IGBT/MOSFET power devices
- All high side channels fully operate up to +600V
- Gate drive supplies up to 18 V per channel
- Under-voltage lockout for all channels
- Over-current protection
- Flexible over-temperature shutdown input
- Advanced input filter
- Built-in dead-time protection
- Shoot-through (cross-conduction) protection
- Independent Enable/disable input and fault reporting
- Shut down all switches during error conditions
- Adjustable fault clear timing
- Separate logic and power grounds
- 3.3 V/5V input logic compatible (positive logic)
- Designed for use with bootstrap power supplies
- Matched propagation delays for all channels
- Matched dead time
- -40°C to 125°C operating range
- SOP28 Package available
- Lead-free

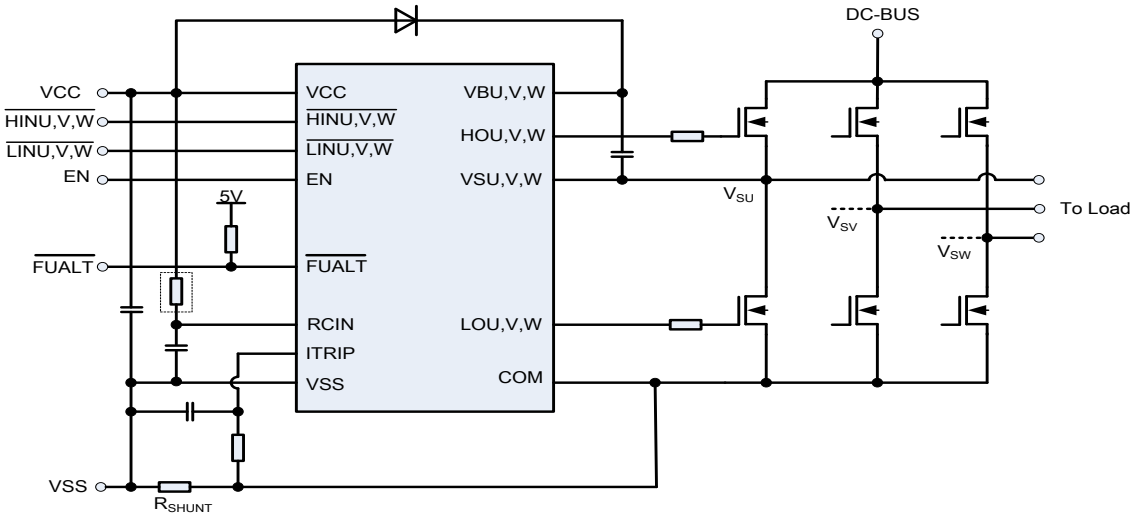
APPLICATIONS

- Appliance motor drives—air conditioners, washing machines, refrigerator, dish washer, Fans
- Servo drives
- Industrial inverters. General purpose three phase inverters

FEATURES COMPARISON

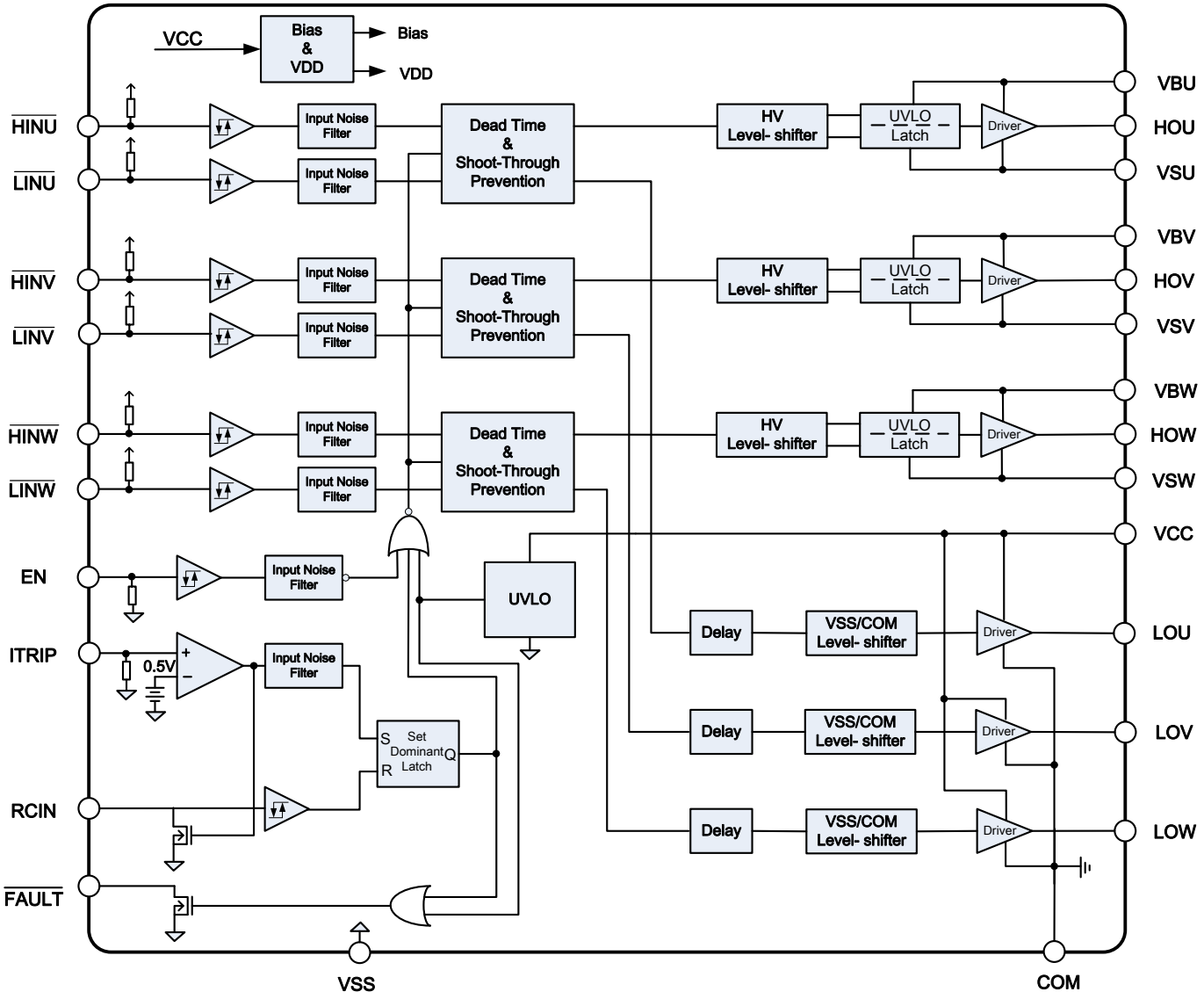
Part	Input Logic	Dead Time	t_{ON}	t_{OFF}	V_{CCUV+}	V_{CCUV-}
PT5616	LIN/HIN	500ns	600ns	600ns	9.5V	9V
PT5616A	$\overline{\text{LIN}}/\overline{\text{HIN}}$	290ns	500ns	480ns	8.9V	8.2V

TYPICAL APPLICATION



Typical connection of 3-phase HV motor driver

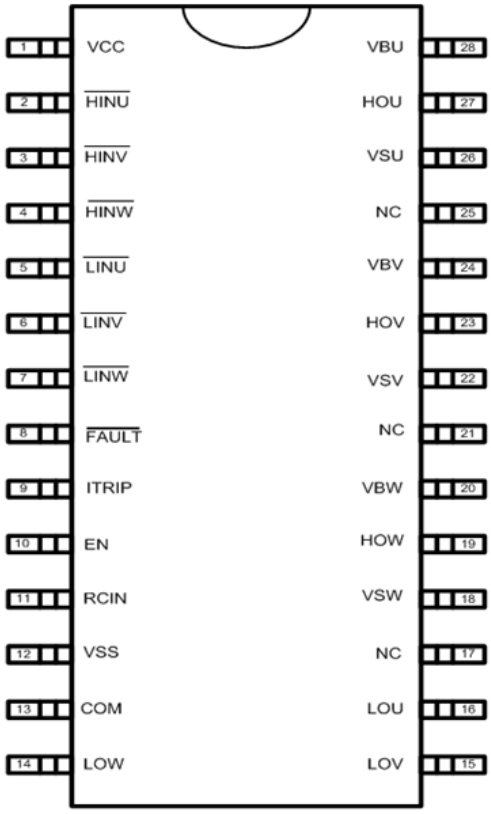
BLOCK DIAGRAM



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT5616A-S	SOP28, 300MIL	PT5616A-S

PIN CONFIGURATION



SOP28

PIN DESCRIPTION

Pin Name	Description	Pin No.
VCC	Logic and low-side gate drivers power supply voltage	1
$\overline{\text{HINU}}$	Logic inputs for high-side gate driver outputs (phase U); input is out-phase with output	2
$\overline{\text{HINV}}$	Logic inputs for high-side gate driver outputs (phase V); input is out -phase with output	3
$\overline{\text{HINW}}$	Logic inputs for high-side gate driver outputs (phase W); input is out -phase with output	4
$\overline{\text{LINU}}$	Logic inputs for low-side gate driver outputs (phase U); input is out -phase with output	5
$\overline{\text{LINV}}$	Logic inputs for low-side gate driver outputs (phase V); input is out -phase with output	6
$\overline{\text{LINW}}$	Logic inputs for low-side gate driver outputs (phase W); input is out -phase with output	7
$\overline{\text{FAULT}}$	Indicates over-current, over-temperature (ITRIP), or low-side under-voltage lockout has occurred. This pin has negative logic and an open-drain output. The use of over-current and over-temperature protection requires the use of external components.	8
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates $\overline{\text{FAULT}}$ and RCIN low. When ITRIP becomes inactive, $\overline{\text{FAULT}}$ stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).	9
EN	Logic input to shutdown functionality. Logic functions when EN is high (i.e., positive logic). No effect on $\overline{\text{FAULT}}$ and not latched. EN can also be extended as input of over-temperature protection when equipped with an external NTC resistor.	10
RCIN	An external RC network input used to define the FAULT CLEAR delay (t_{FLTCLR}) approximately equal to R*C. When RCIN > 8 V, the $\overline{\text{FAULT}}$ pin goes back into an open-drain high-impedance state.	11
VSS	Logic ground	12
COM	Low-side gate drive return	13
LOW	Low-side gate driver W-phase output	14
LOV	Low-side gate driver V-phase output	15
LOU	Low-side gate driver U-phase output	16
NC.	Not Connected	17
VSW	High-side driver W-phase floating supply offset voltage	18
HOW	High-side driver W-phase gate driver output	19
VBW	High-side driver W-phase floating supply	20
NC.	Not Connected	21
VSV	High-side driver V-phase floating supply offset voltage	22
HOV	High-side driver V-phase gate driver output	23
VBV	High-side driver V-phase floating supply	24
NC.	Not Connected	25
VSU	High-side driver U-phase floating supply offset voltage	26
HOU	High-side driver U-phase gate driver output	27
VBU	High-side driver U-phase floating supply	28

FUNCTION DESCRIPTION

LOW SIDE POWER SUPPLY (VCC, VSS, COM)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit. Output power stage is referenced to COM ground. COM ground is floating respect to VSS ground with a recommended range of operation of +/-5V, which guarantees enough margin of gate to source voltage, V_{GS}, to driver power devices such as power MOSFET.
The built-in under-voltage lockout circuit enables the device to operate at sufficient power on when a typical VCC supply voltage higher than V_{CCUV+}=8.9 is present, shown as FIG1. The IC shuts down all the gate drivers outputs, when the VCC supply voltage is below V_{CCUV-}=8.2 V, shown as FIG1. This prevents the external power devices from extremely low gate voltage levels during on-state and therefore from excessive power dissipation.

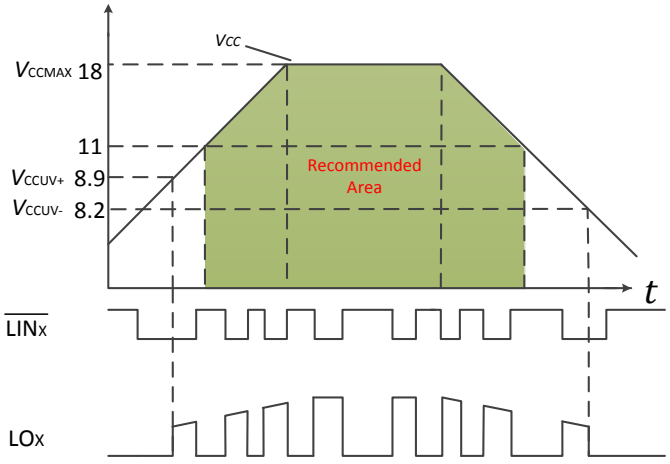


FIG.1 VCC supply UVLO operating area

HIGH SIDE POWER SUPPLY (VBU-VSU, VBV-VSV, VBW-VSW)

VB to VS is the high side supply voltage. The totally high side circuitry can float with respect to VSS following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to VCC, and it can be powered with small bootstrap capacitors.
The device operating area as a function of the supply voltage is given in Figure2.

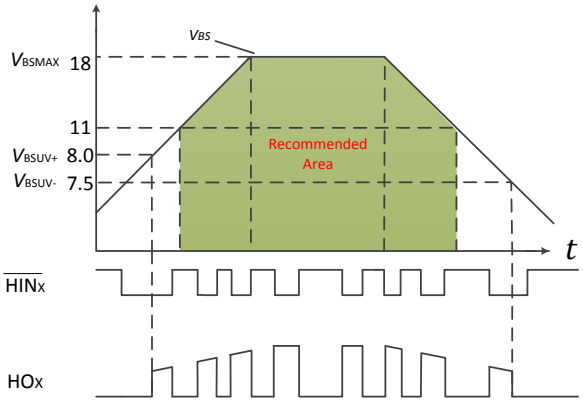


FIG.2 VBS supply UVLO operating area

LOW SIDE AND HIGH CONTROL INPUT LOGIC (HINU,V,W, LINU,V,W)

The Schmitt trigger threshold of each input is designed enough low such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and advanced noise filter provide beneficial noise rejection to short input pulses. An internal pull-down resistor of about 50kΩ (positive logic) pre-biases each input during VCC supply start-up state. It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 800ns.

SHOOT-THROUGH PREVENTION

The IC is equipped with shoot-through prevention circuitry (also known as cross conduction prevention circuitry). Figure 3 shows how this prevention circuitry prevents both the high- and low-side switches from conducting at the same time. During the inputs controlling high side driver and low side driver are both “low”, the both driver outputs are pulled down “low” to shutdown two power devices in the same bridge.

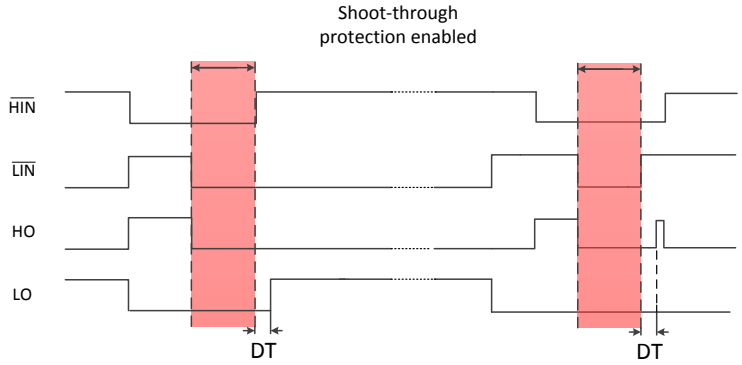


FIG.3 Shoot-through prevention

DEAD TIME

This PT5616A features integrated a fixed dead-time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver. Figure 4 illustrates the dead time period and the relationship between the output gate signals.

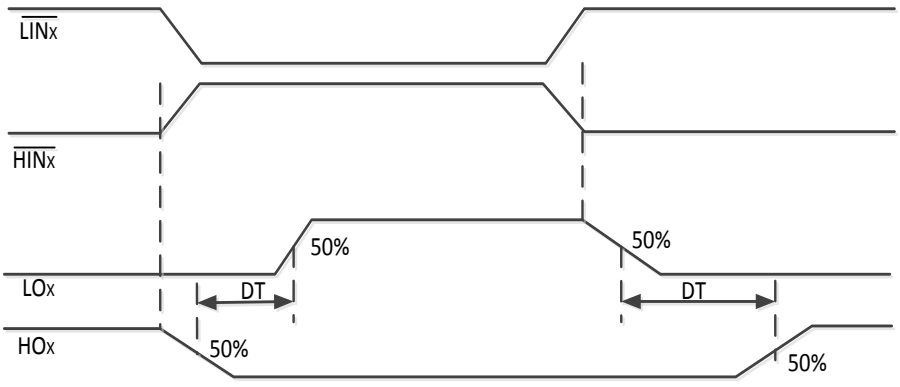


FIG.4 Dead Time

ENABLE INPUT (EN)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at “low” logic level. The switching levels of the Schmitt-Trigger are here $V_{EN,\,TH+}$ = 2.0 V and $V_{EN,\,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} =400 ns. There is an internal pull up resistor of about 100kΩ, which keeps the gate driver outputs on in case of EN pin floating and is extended to some special purpose.

FAULT INDICATOR ($\overline{FAULT}$)

$\overline{FAULT}$ pin is an active low open-drain output indicating the states of the gate driver (see Figure 6). The pin is active (i.e. forces low voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).
- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished and RCIN input is released (please refer to ITRIP pin).

OVER CURRENT PROTECTION (ITRIP)

The PT5616A are equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the power ground or DC-bus. Once the IC detects an over-current event through the ITRIP pin, the gate driver outputs are shutdown, a fault is reported through the $\overline{FAULT}$ pin, and RCIN is pulled down to V_{SS}.

The level of current at which the over-current protection is activated is determined by the shunt resistor, R_{SHUNT}, placed between power devices source/emitter and VSS, which is shown in the FIG.5. The circuit designer will need to determine the maximum allowable level of motor current in the power ground or DC- bus through the followed equation:

$$I_{MOTOR} = \frac{V_{IT,TH+}}{R_{SHUNT}}$$

The ITRIP comparator threshold, $V_{IT,\,TH+}$ (typical 0.45 V), is referenced to VSS ground. An internal blank time (typ. t_{BL} = 250 ns) prevents the IC to detect false over-current events.
RCIN input/output pin is used to determine the reset time of the fault condition. As soon as ITRIP threshold is exceeded the external capacitor connected to RCIN is fully discharged. The capacitor is then recharged by the internal RCIN current generator when the over-current condition is finished. As soon as RCIN voltage exceeds the rising threshold of typical $V_{RCIN,TH}$ = 8 V, the fault condition releases and the driver returns operational following the control input pins. The relationship of $\overline{FAULT}$, ITRIP and RCIN is given in the FIG.6.

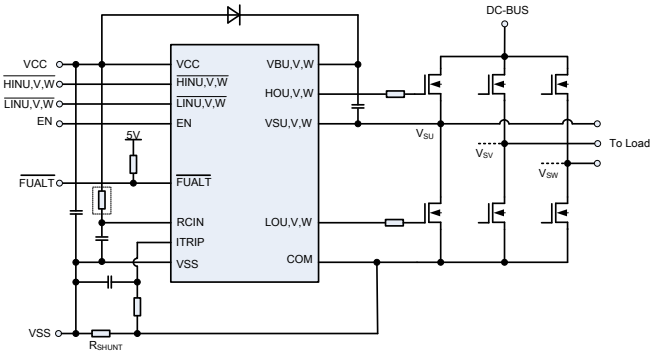


FIG.5

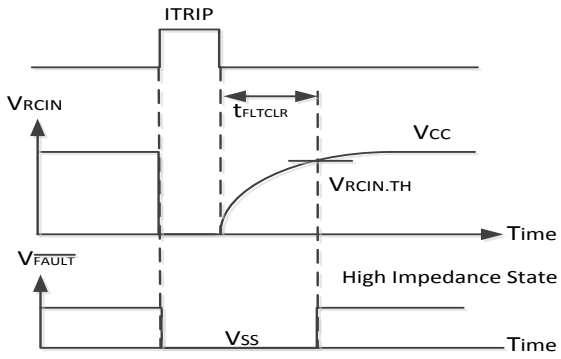


FIG.6

GATE DRIVER (HOU, V, W, LOU, V, W)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive the power devices such as IGBT and MOSFET. Low side outputs (i.e. LOU, V, W) are state triggered by the respective inputs, while high side outputs (i.e. HOU, V, W) are only changed at the edge of the respective inputs. In particular, after releasing from an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after releasing from a under voltage condition of the VCC supply, the low side outputs can directly switch to the state of their respective inputs and don't suffer from the trouble as high side driver.

SEPARATE LOGIC AND POWER GROUNDS

The PT5616A has separate logic and power ground pin (V_{SS} and COM respectively) to eliminate some of the noise problems that can occur in power conversion applications. Current sensing shunt resistors are commonly used in many applications for power inverter protection (i.e., over-current protection), and in the case of motor drive applications, for motor current measurements. In these situations, it is often beneficial to separate the logic and power grounds. Figure 5 also shows an IC with separate V_{SS} and COM pins and how these two grounds are used in the system. The V_{SS} is used as the reference point for the logic and over-current circuitry. Alternatively, the COM pin is the reference point for the low-side gate drive circuitry. The driver output voltage used to drive the low-side gate is V_{LO}-COM.

TIMING DIAGRAM, FIG.7

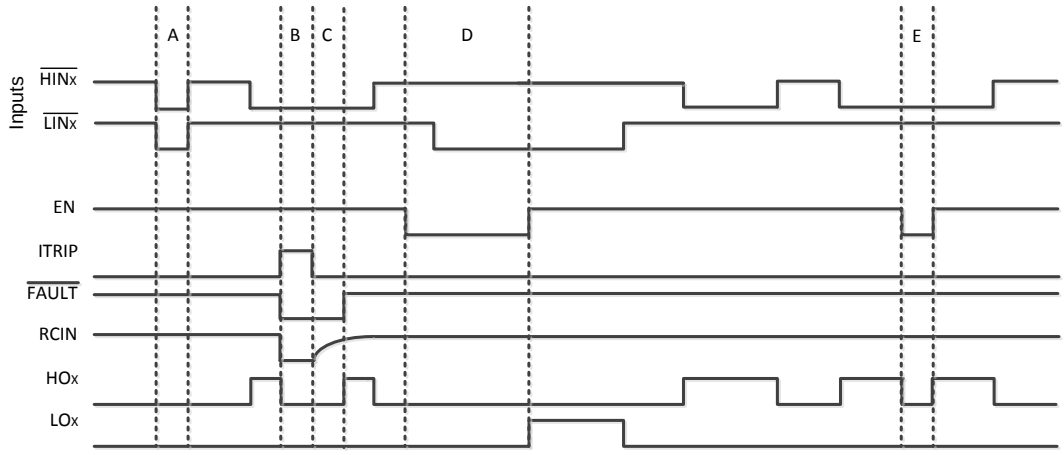


FIG.7 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to VSS unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	$V_{B.U.V.W}$	-0.3	600	V
High-side offset voltage	$V_{S.U.V.W}$	$V_{B.U.V.W}$ -20	$V_{B.U.V.W}$ +0.3	
High-side gate driver output voltage	$V_{HO.U.V.W}$	$V_{S.U.V.W}$-0.3	$V_{S.U.V.W}$ +0.3	
Low-side gate driver output voltage	$V_{LO.U.V.W}$	COM-0.3	V_{CC}+0.3	
Logic input voltage($\overline{HINX}$, $\overline{LINX}$,, ITRIP, EN)	$V_{\overline{HINU,V,W}}$ $V_{\overline{LINU,V,W}}$	-0.3	20	
Low-side supply voltage	V_{CC}	-0.3	20	
Logic gate driver return	COM	V_{CC}-20	V_{CC}+0.3	
$\overline{FAULT}$output voltage	V_{FLT}	-0.3	VCC+0.3	V
RCIN input voltage	V_{RCIN}	-0.3	VCC+0.3	V
High-side input pulse width	$PW_{\overline{HIN}}$	600	-	ns
Allowable Offset Voltage Slew Rate	DV/DT	-	50	V/ns
Package power dissipation @ $T_A \leqslant +25℃$	PD	-	1.6	W
Thermal resistance, junction to ambient, SOP28L-W	Rth_{JA}		78	°C/W
Junction temperature	T_J	-50	+150	°C
Storage temperature	T_S	-40	+150	
Lead temperature (soldering, 10 seconds)	T_L	-	300	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Low-side supply voltage	V_{CC}	11	15	18	V
High-side Floating Supply Offset Voltage(note1)	$V_{S.U.V.W}$	V_B-18	-	V_B-11	
High-side Floating Supply Voltage	$V_{B.U.V.W}$	-10	-	600	
High-side gate driver output voltage	$V_{HO.U.V.W}$	V_S	-	V_B	
Low-side gate driver output voltage	$V_{LO.U.V.W}$	COM	-	V_{CC}	
Logic gate driver return	COM	-3		3	
Logic input voltage	$V_{\overline{HINU,V,W}}$ $V_{\overline{LINU,V,W}}$	0	-	5	
EN input voltage	V_{EN}	0	-	V_{CC}	V
$\overline{FAULT}$ output voltage	V_{FLT}	0	-	V_{CC}	V
RCIN input voltage	V_{RCIN}	0	-	V_{CC}	V
ITRIP input voltage	V_{ITRIP}	0	-	V_{CC}	V
IC operating junction temperature	T_J	-40	-	+125	°C

Note1: For VBS=15V, normal Logic operation for VS of –10 V to 600 V. The parameter is only guaranteed by design.

STATIC ELECTRICAL CHARACTERISTICS

（VCC-VSS）=(VB-VS)=15V. T_{AMB}=25℃ unless otherwise specified .the V_{IN}, V_{TH} and I_{IN} Parameters are reference to VSS and are applicable to all six channels. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads. The V_{CCUV} parameters are referenced to VSS. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
VCC quiescent current	I_{QVCC}	VH$\overline{IN}$U,V,W =0 or 5V VL$\overline{IN}$U,V,W =0 or 5V	-	1	1.5	mA
VCC supply under-voltage positive going threshold	V_{CCUV+}		7.9	8.9	10	V
VCC supply under-voltage negative going threshold	V_{CCUV-}		7.2	8.2	9.2	
V_{CC} supply under-voltage lockout hysteresis	V_{CCHYS}		-	0.7	-	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V_{BSUV+}		6.0	8.0	10.0	V
High side VBS supply under-voltage negative going threshold	V_{BSUV-}		5.5	7.5	9.5	
High side VBS supply under-voltage lockout hysteresis	$V_{BSUVHYS}$		-	0.5	-	
High side VBS quiescent current	I_{QBS}	V_{BS}=15V	45	65	85	μA
Offset supply leakage current	I_{LK}	V_B=V_S=600V V_{CC}=0V	-	-	1	
Gate Driver Output Section						
Output High Short-Circuit Pulse Current	I_{O+}	V_{HO}=V_S=0, V_{HO}=V_B=15V, V_{LO}=COM=0, V_{LO}=V_{CC}=15V	-	200	-	mA
Output Low Short-Circuit Pulse Current	I_{O-}		-	400	-	
High level output voltage drop, V_{CC}-V_{LO},V_{BS}-V_{HO}	V_{OH}	IO+= 20 mA	-	0.8	1.5	V
Low level output voltage drop	V_{OL}	IO-= 20 mA	-	0.3	0.5	V
Allowable Negative VS Pin Voltage for H$\overline{IN}$U,V,W Signal Propagation to HOU.V.W	V_{SN}	Fixed V_{BS}=15V	-	-10	-	V
Logic Input Section						
Logic"1" Input voltage H$\overline{IN}$U,V,W and L$\overline{IN}$U,V,W	V_{IH}		2.5	-	-	V
Logic"0" Input voltage H$\overline{IN}$U,V,W and L$\overline{IN}$U,V,W	V_{IL}		-	-	0.8	
Input positive going threshold	$V_{IN,TH+}$		-	2.0	-	
Input negative going threshold	$V_{IN,TH-}$		-	1.3	-	
Logic "1" Input bias current	I_{IN+}	V_{IN}=5V	-	0	-	uA
Logic "0" Input bias current	I_{IN-}	V_{IN}=0	-	100	150	
Shut down and protection Section						
RCIN positive going threshold	$V_{RCIN,TH}$		-	8	-	V
RCIN hysteresis	$V_{RCIN,HY}$		-	3	-	V
RCIN internal charge current	I_{RCIN}	V_{RCIN}=3V	-	2	-	uA
RCIN low on resistance of pull down MOSFET	$R_{ON,RCIN}$	I_{SINK}=2mA	-	40	80	Ω
ITRIP positive going threshold	$V_{IT,TH+}$		0.3	0.45	0.6	V
ITRIP hysteresis	$V_{IT,HYS}$		40	70	-	mV
"High" ITRIP input bias current	I_{ITRIP+}	V_{IT}=5V	-	50	80	uA
"Low" ITRIP input bias current	I_{ITRIP-}	V_{IT}=0V	-	0	1	uA
Enable positive going threshold	$V_{EN,TH+}$		-	2.0	2.5	V
Enable negative going threshold	$V_{EN,TH-}$		0.8	1.3	-	V
"High" enable input bias current	I_{EN+}	V_{EN}=5V	-	100	-	uA
"Low" enable input bias current	I_{EN-}	V_{EN}=0V	-	0	-	uA
$\overline{FAULT}$ low on resistance	$R_{ON,FLT}$	I_{SINK}=2mA	-	40	80	Ω

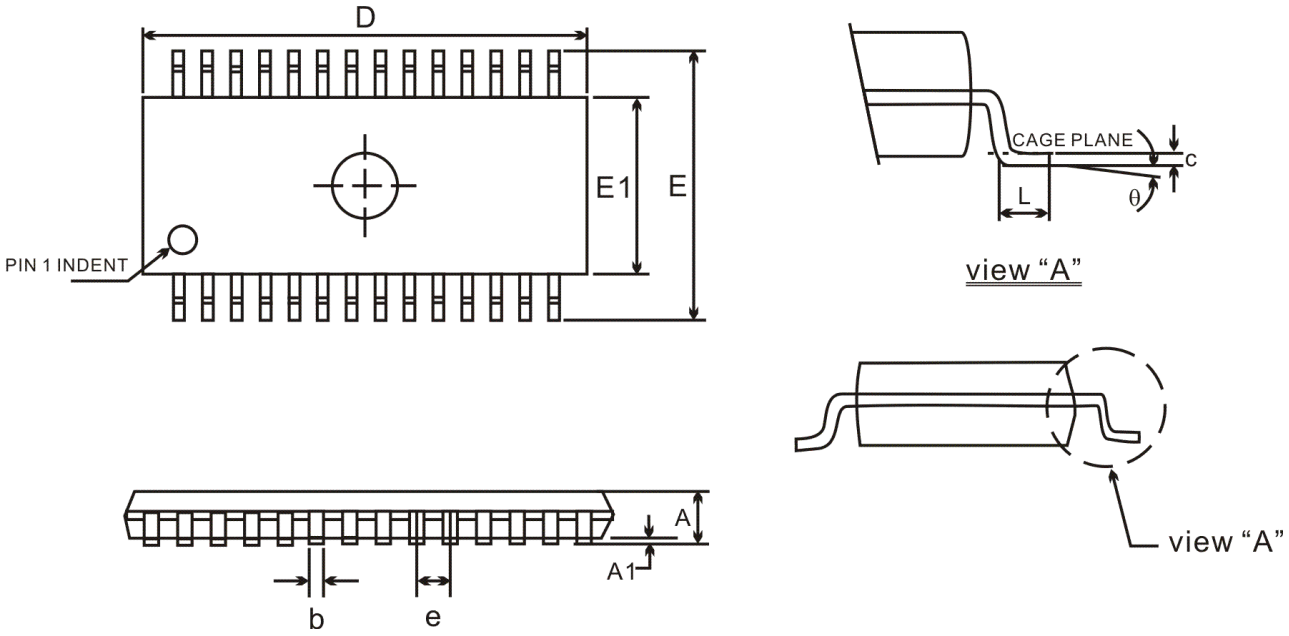
DYNAMIC ELECTRICAL CHARACTERISTICS

（VCC-VSS）=(VB-VS)=15V ,$V_{SU,V,W}$=VSS=COM, and C_{HO}=C_{LO}=1nF unless otherwise specified, T_{AMB}=25℃.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCC operating Vcc supply current	I_{VCCOP}	f $\overline{\text{LINU,V,W}}$=20k, f $\overline{\text{HINU,V,W}}$=20k,	-	4	6	mA
Turn-On propagation delay	t_{ON}	$V_{\overline{HINU,V,W}}$ or $V_{\overline{LINU,V,W}}$ =0V, $V_{S.U.V.W}$=5V	250	500	750	ns
Turn-Off Propagation delay	t_{OFF}	$V_{\overline{HINU,V,W}}$ or $V_{\overline{LINU,V,W}}$ =5V, $V_{S.U.V.W}$=5V	240	480	720	
Turn-On Rise time	t_R	$V_{\overline{HINU,V,W}}$ or $V_{\overline{LINU,V,W}}$ =0V, $V_{S.U.V.W}$=5V	-	120	-	
Turn-Off Fall time	t_F	$V_{\overline{HINU,V,W}}$ or $V_{\overline{LINU,V,W}}$ =5V, $V_{S.U.V.W}$=5V	-	50	-	
Input Filtering Time	$t_{FIL,IN}$		150	250	350	
Dead Time	DT	$\overline{\text{HIN}}$ and $\overline{\text{LIN}}$ inputs without external dead time	300	500	700	
Dead-Time Matching(All Six Channels)	MDT	$\overline{\text{HIN}}$ and $\overline{\text{LIN}}$ inputs without external dead time	-	-	80	
Delay Matching(t_{ON}, t_{OFF}, All Six Channels)	MT	$\overline{\text{HIN}}$ and $\overline{\text{LIN}}$ inputs with external dead time >2us	-	-	80	
Output Pulse-Width Matching	PM	PW_{IN}=5us, PM=PW_{OUT}-PW_{IN}	-	-	80	
Enable low to output shutdown propagation delay	t_{EN}	$V_{\overline{HINU,V,W}}$ or $V_{\overline{LINU,V,W}}$ =0V, V_{EN} = 0 V ,$V_{HOU,V,W}$ or $V_{LOU,V,W}$=0	200	400	600	ns
Enable input filter time	$t_{FILTER,EN}$		100	200		ns
FAULT clear time	t_{FLTCLR}	RCIN: R = 2 MΩ, C = 1 nF	1.2	1.6	2.0	ms
ITRIP to output shutdown propagation delay	t_{ITRIP}	$V_{\overline{HINU,V,W}}$ or $V_{\overline{LINU,V,W}}$ =5V, $V_{HOU,V,W}$ or $V_{LOU,V,W}$=0, V_{IT} = 5 V	500	700	900	ns
ITRIP blanking time	t_{BL}	V_{IT} = 5 V, V_{FAULT} “Low”		120		ns
ITRIP to FAULT propagation delay	t_{FLT}	V_{IT} = 5 V, V_{FLT} “Low”	250	450	650	ns

PACKAGE INFORMATION

28-PIN, SOP 300MIL



Symbol	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	-	0.30
b	0.31	-	0.51
c	0.20	-	0.33
e	1.27 BSC.		
D	17.90 BSC.		
E	10.30 BSC.		
E1	7.50 BSC.		
L	0.38	-	1.27
θ	0°	-	8°

Notes:
1. All controlling dimensions are in millimeter.
2. Refer to JEDEC MS-013 AD.

IMPORTANT NOTICE

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