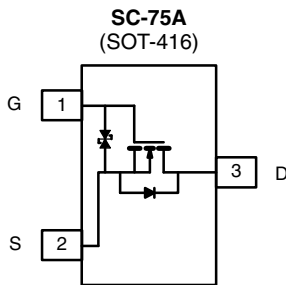


N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS(min.)}$ (V)	$R_{DS(on)}$ (Ω)	$V_{GS(th)}$ (V)	I_D (mA)
60	1.25 at $V_{GS} = 10$ V	1 to 2.5	330



Marking Code: E

Ordering Information: Si1022R-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- Low On-Resistance: 1.25 Ω
- Low Threshold: 2.5 V
- Low Input Capacitance: 30 pF
- Fast Switching Speed: 25 ns
- Low Input and Output Leakage
- Miniature Package
- ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid State Relays

BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Error Voltage
- Small Board Area

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_A = 25$ °C	330
		$T_A = 85$ °C	240
Pulsed Drain Current ^a	I_{DM}	650	mA
Power Dissipation ^a	P_D	$T_A = 25$ °C	250
		$T_A = 85$ °C	130
Thermal Resistance, Maximum Junction-to-Ambient ^a	R_{thJA}	500	°C/W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

Notes:

a. Surface mounted on FR4 board, power applied for $t \leq 10$ s.

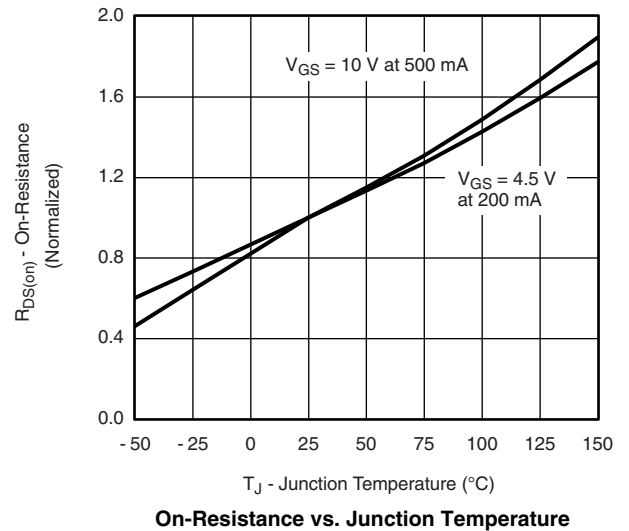
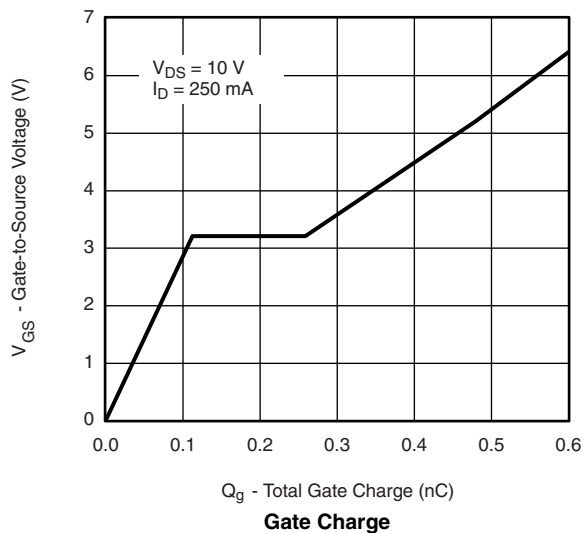
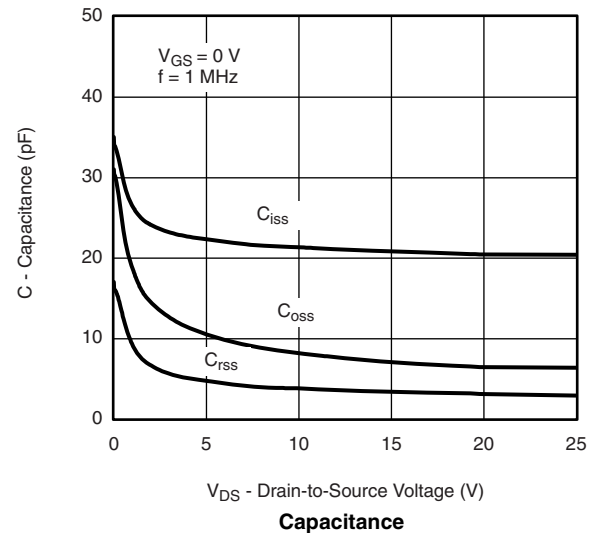
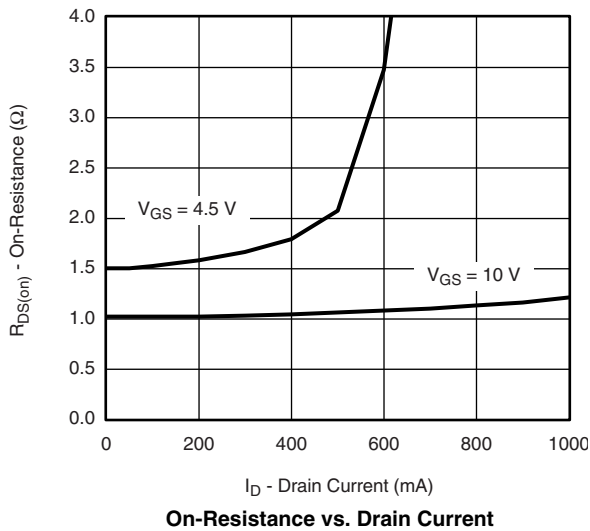
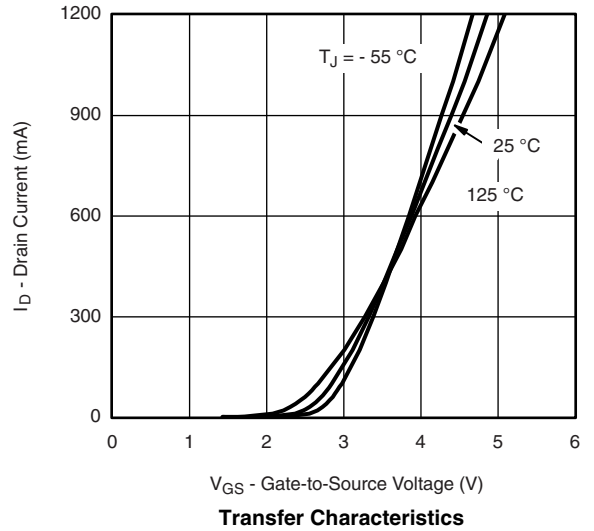
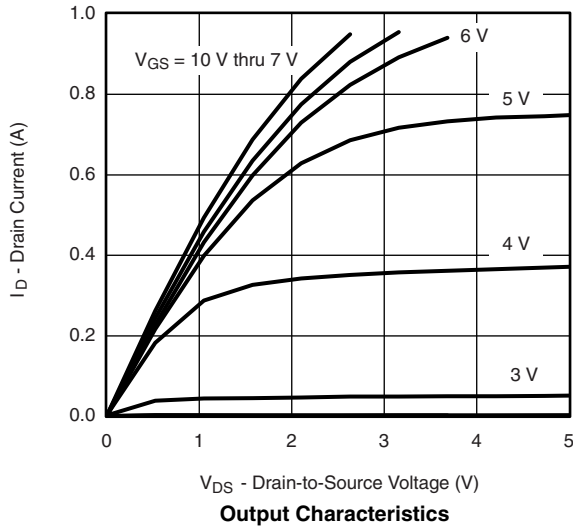
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 10\text{ }\mu\text{A}$	60			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 0.25\text{ mA}$	1		2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 10\text{ V}$			± 150	nA
		$T_J = 85\text{ }^\circ\text{C}$			± 500	
		$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 5\text{ V}$			± 20	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$			10	
		$T_J = 85\text{ }^\circ\text{C}$			100	
		$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$	500			mA
		$V_{DS} = 7.5\text{ V}$, $V_{GS} = 10\text{ V}$	800			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$, $I_D = 200\text{ mA}$			3.0	Ω
		$T_J = 125\text{ }^\circ\text{C}$			5.0	
		$V_{GS} = 10\text{ V}$, $I_D = 500\text{ mA}$			1.25	
		$T_J = 125\text{ }^\circ\text{C}$			2.25	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 200\text{ mA}$	100			mS
Diode Forward Voltage ^a	V_{SD}	$V_{GS} = 0\text{ V}$, $I_S = 200\text{ mA}$			1.3	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		30		pF
Output Capacitance	C_{oss}			6		
Reverse Transfer Capacitance	C_{rss}			2.5		
Gate Charge	Q_g	$V_{DS} = 10\text{ V}$, $I_D = 250\text{ mA}$, $V_{GS} = 4.5\text{ V}$			0.6	nC
Switching^{b, c}						
Turn-On Time	$t_{(on)}$	$V_{DD} = 30\text{ V}$, $R_L = 150\text{ }\Omega$, $I_D = 200\text{ mA}$, $V_{GEN} = 10\text{ V}$, $R_g = 10\text{ }\Omega$			25	ns
Turn-Off Time	$t_{(off)}$				35	

Notes:

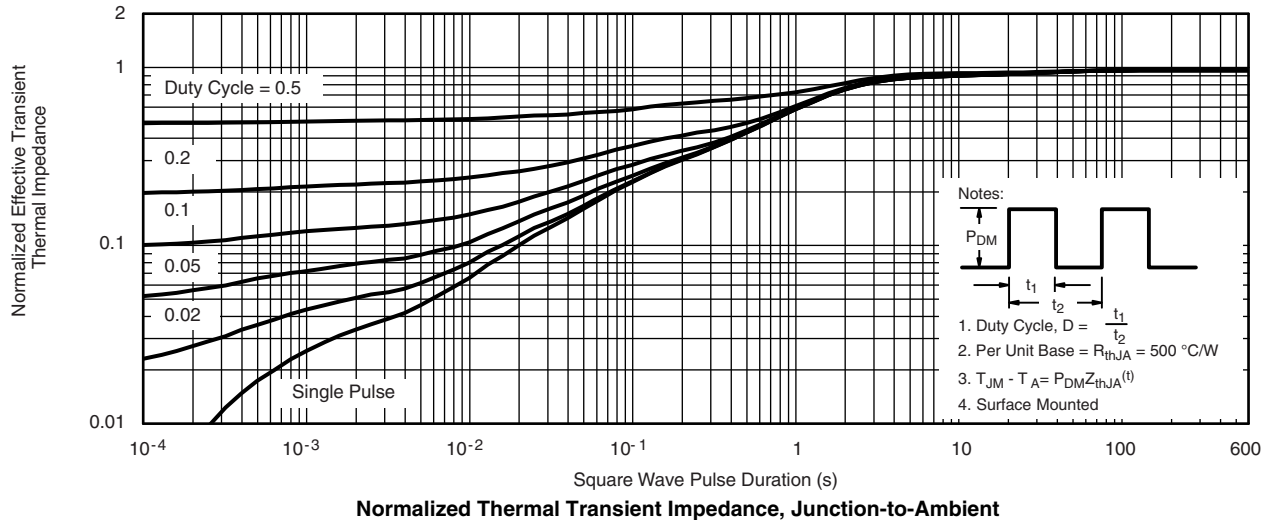
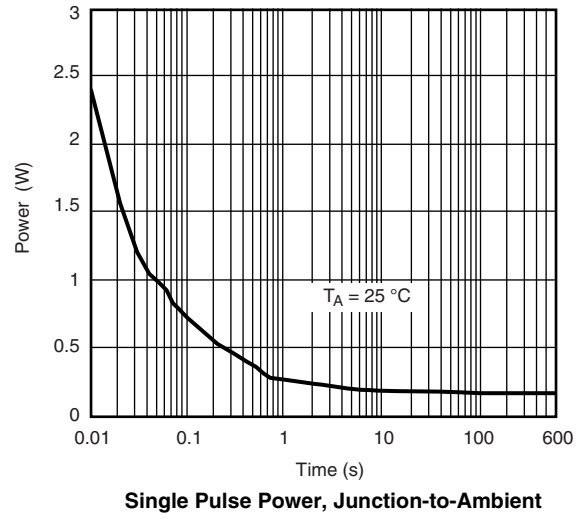
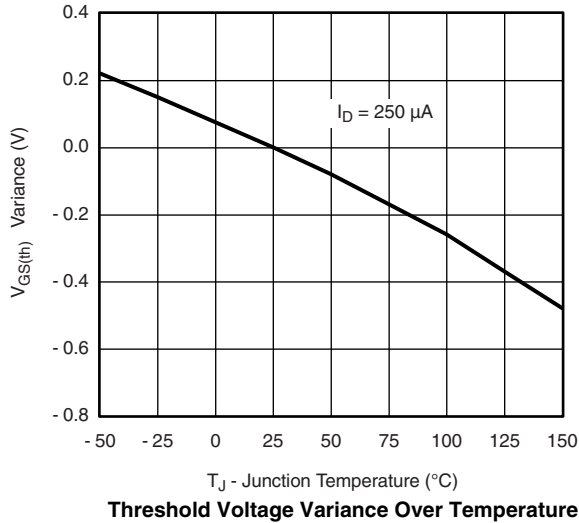
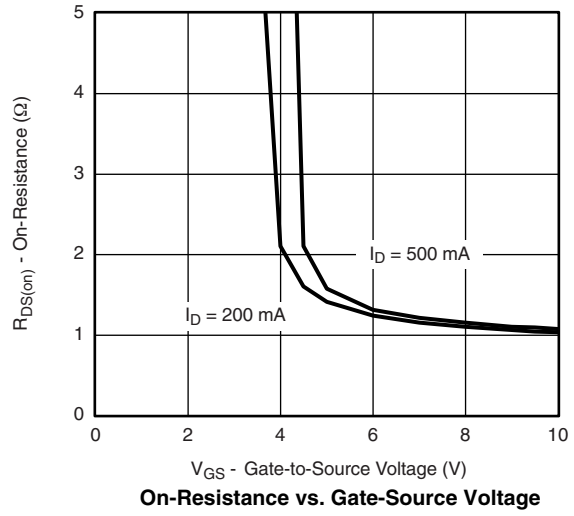
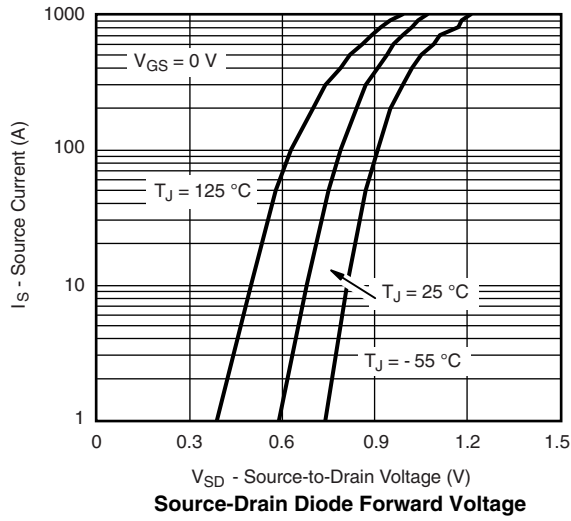
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

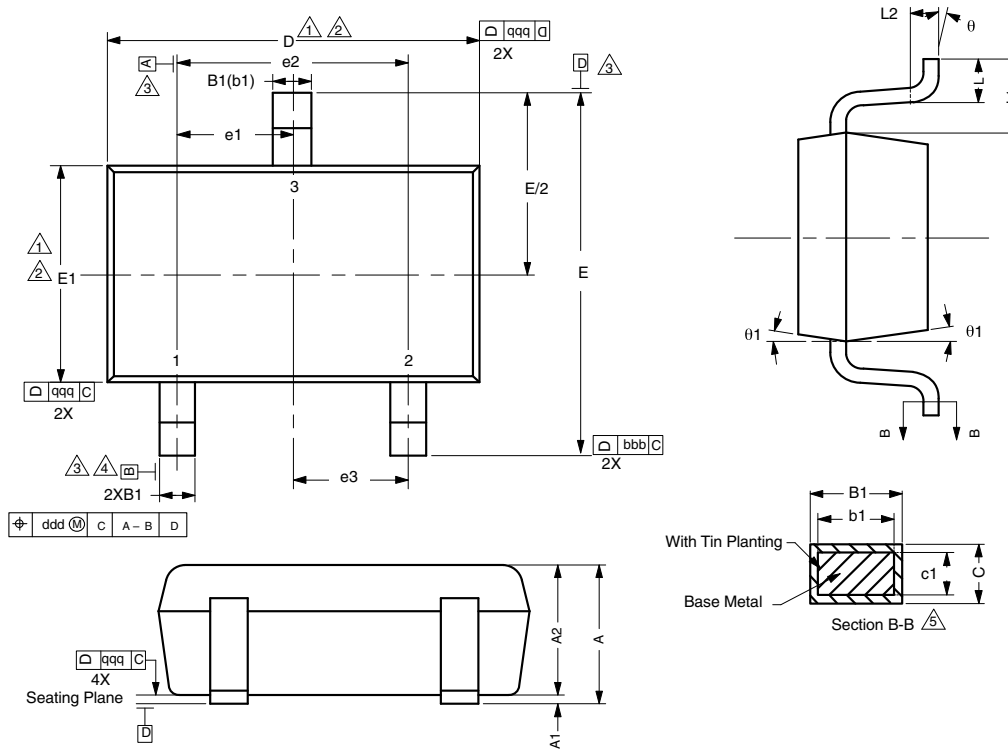


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?71331.

SC-75A: 3 Leads



DWG: 5868

Notes

Dimensions in millimeters will govern.

- 1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
- 2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- 3. Datums A, B and D to be determined 0.10 mm from the lead tip.
- 4. Terminal positions are shown for reference only.
- 5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	-	0.80	
A1	0.00	-	0.10	
A2	0.65	0.70	0.80	
B1	0.19	-	0.24	5
b1	0.17	-	0.21	
c	0.13	-	0.15	5
c1	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E1	0.66	0.76	0.86	1, 2
e1	0.50 BSC			
e2	1.00 BSC			
e3	0.50 BSC			
L	0.15	0.205	0.30	
L1	0.40 ref.			
L2	0.15 BSC			
q	0°	-	8°	
q1	4°	-	10°	

RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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