

LESD8L3.3CT5G

Transient Voltage Suppressors

ESD Protection Diodes with Ultra-Low Capacitance

The ESD8L is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Specification Features:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- This is a Pb-Free Device

Mechanical Characteristics:

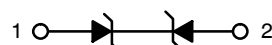
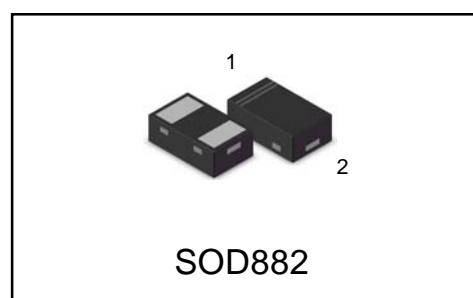
CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

LESD8L3.3CT5G



Ordering information

Device	Marking	Shipping
LESD8L3.3CT1G	S	5000/Tape&Reel
LESD8L3.3CT3G	S	8000/Tape&Reel
LESD8L3.3CT5G	S	10000/Tape&Reel

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		±10 ±15	kV
Total Power Dissipation on FR-5 Board (Note 1) @ T _A = 25°C	P _D	150	mW
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature Range	T _J	-55 to +125	°C
Lead Solder Temperature - Maximum (10 Second Duration)	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

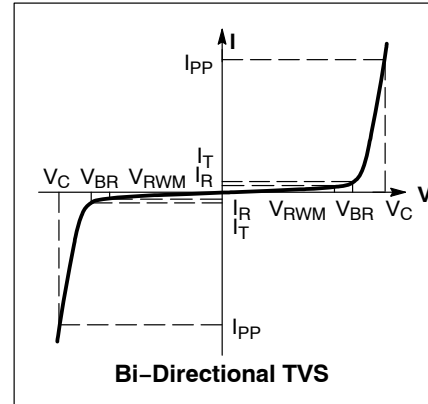
1. FR-5 = 1.0 x 0.75 x 0.62 in.

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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
I _F	Forward Current
V _F	Forward Voltage @ I _F
P _{pk}	Peak Power Dissipation
C	Capacitance @ V _R = 0 and f = 1.0 MHz



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.0 V Max. @ I_F = 10 mA for all types)

Device	Device Marking	V _{RWM} (V)	I _R (μA) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	I _T (mA)	C (pF)		V _C (V) @ I _{PP} = 1 A (Note 3)	V _C (Per IEC61000-4-2 (Note 4))
		Max	Max	Min		Typ	Max	Max	
LESD8L3.3CT5G	S	3.3	1.0	4.8	1.0	0.5	0.9	10	Figures 1 and 2 See Below

- V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
- Surge current waveform per Figure 5.
- For test procedure see Figures 3 and 4.

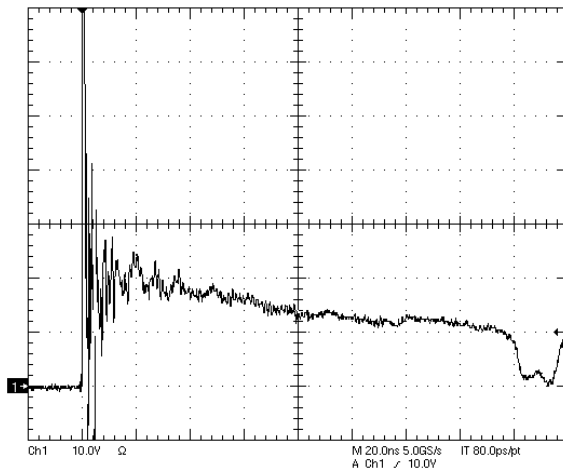


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

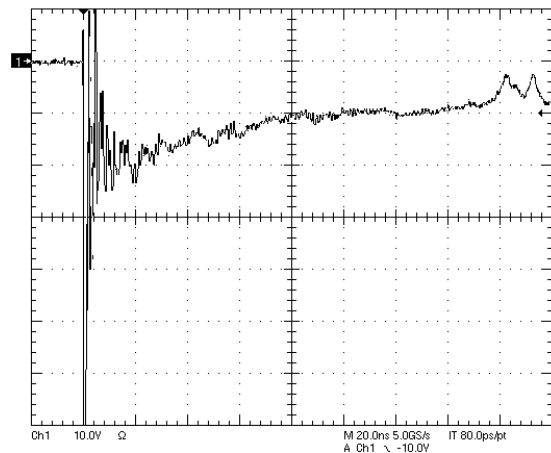


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

IEC61000-4-2 Waveform

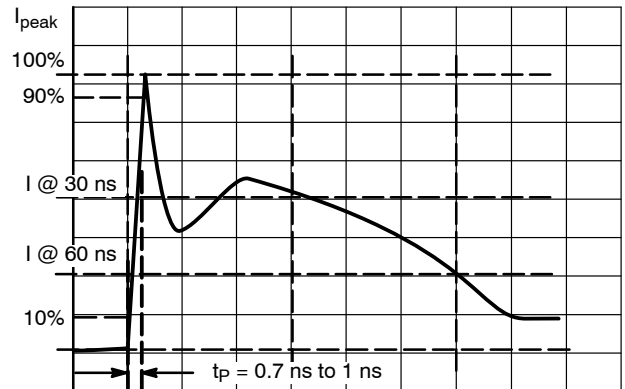


Figure 3. IEC61000-4-2 Spec

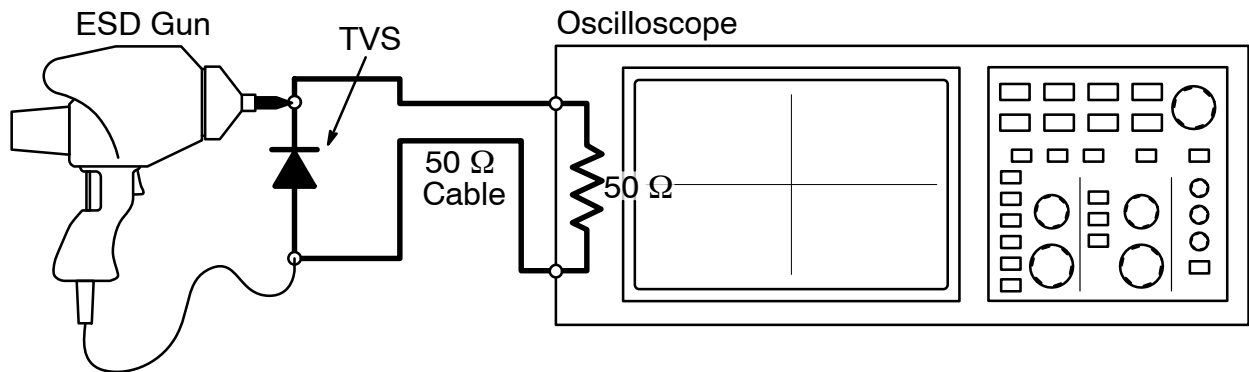


Figure 4. Diagram of ESD Test Setup

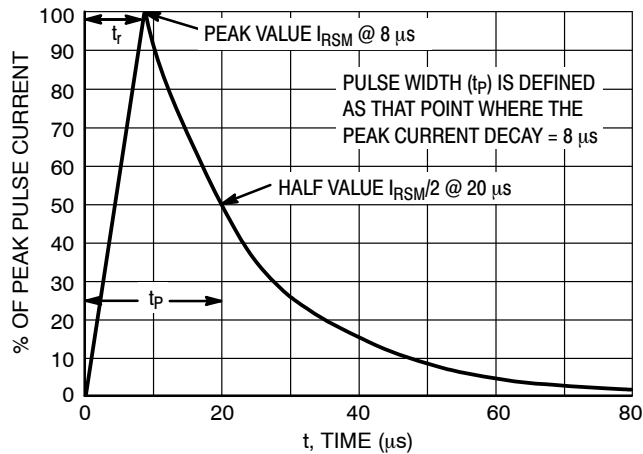
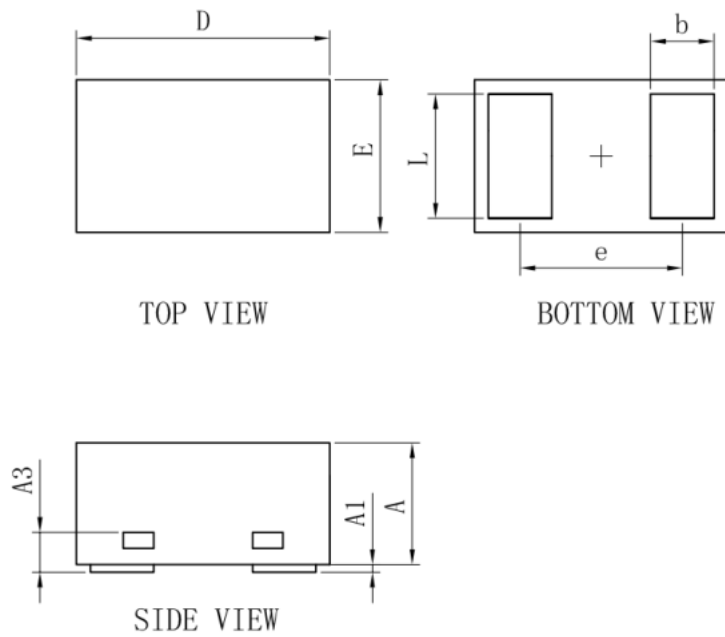


Figure 5. 8 X 20 μs Pulse Waveform

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OUTLINE AND DIMENSIONS

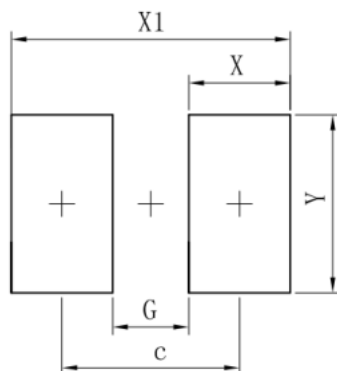
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Dim	Min	Typ	Max
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	-	0.64	-
L	0.44	0.49	0.54
b	0.20	0.25	0.30
A	0.43	0.48	0.53
A1	0	-	0.05
A3	0.127REF.		
All Dimensions in mm			

SOLDERING FOOTPRINT

SOD882



Dimensions	(mm)
c	0.70
G	0.30
X	0.40
X1	1.10
Y	0.70