

# CSD17309Q3 30-V N-Channel NexFET™ Power MOSFET

## 1 Features

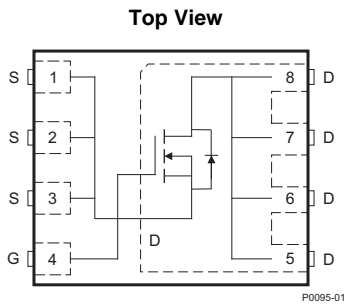
- Optimized for 5 V Gate Drive
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm x 3.3 mm Plastic Package

## 2 Applications

- Notebook Point of Load
- Point of Load Synchronous Buck in Networking, Telecom, and Computing Systems

## 3 Description

This 30 V, 4.2 mΩ NexFET™ power MOSFET is designed to minimize losses in power conversion applications and optimized for 5 V gate drive applications.



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	30		V
$Q_g$	Gate Charge Total (4.5 V)	7.5		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	1.7		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 3\text{ V}$	6.3	mΩ
		$V_{GS} = 4.5\text{ V}$	4.9	
		$V_{GS} = 8\text{ V}$	4.2	
$V_{GS(th)}$	Threshold Voltage	1.2		V

### Ordering Information<sup>(1)</sup>

Device	Media	Qty	Package	Ship
CSD17309Q3	13-Inch Reel	2500	SON 3.3 x 3.3 mm Plastic Package	Tape and Reel
CSD17309Q3T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

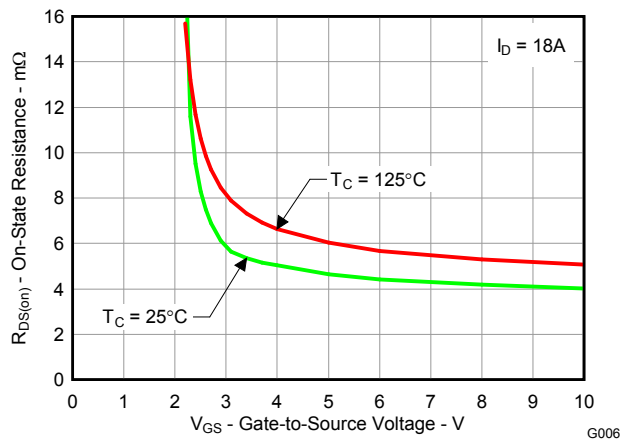
### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current <sup>(1)</sup>	20	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	112	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.8	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 57\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	162	mJ

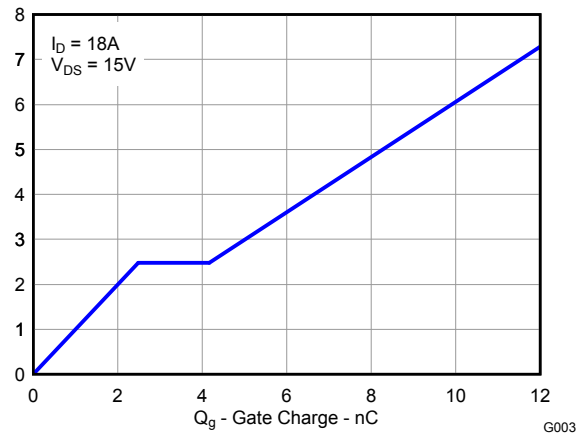
(1) Typical  $R_{\theta JA} = 45^\circ\text{C/W}$  when mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

**$R_{DS(on)}$  vs  $V_{GS}$**



**Gate Charge**



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Specifications</b> ..... 3 5.1 Electrical Characteristics..... 3 5.2 Thermal Information ..... 3 5.3 Typical MOSFET Characteristics..... 4 <b>6 Device and Documentation Support</b> ..... 8	6.1 Trademarks ..... 8 6.2 Electrostatic Discharge Caution ..... 8 6.3 Glossary ..... 8 <b>7 Mechanical, Packaging, and Orderable Information</b> ..... 9 7.1 Q3 Package Dimensions ..... 9 7.2 Recommended PCB Pattern..... 10 7.3 Recommended Stencil Opening ..... 10 7.4 Q3 Tape and Reel Information..... 11
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## 4 Revision History

Changes from Revision A (October 2010) to Revision B	Page
• .....	1
• Added 7" reel to Ordering Information .....	1
• Updated mechanical information .....	9

Changes from Original (March 2010) to Revision A	Page
• Deleted the Package Marking Information section .....	11

## 5 Specifications

### 5.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-Source Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V			1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +10 / -8 V			100	nA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.9	1.2	1.7	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = 3 V, I <sub>D</sub> = 18 A		6.3	8.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A		4.9	6.3	mΩ
		V <sub>GS</sub> = 8 V, I <sub>D</sub> = 18 A		4.2	5.4	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 18 A		67		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 15 V, f = 1 MHz		1150	1440	pF
C <sub>OSS</sub>	Output Capacitance			580	750	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			43	56	pF
R <sub>g</sub>	Series Gate Resistance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 18 A		1.2	2.4	Ω
Q <sub>g</sub>	Gate Charge Total (4.5 V)			7.5	10	nC
Q <sub>gd</sub>	Gate Charge Gate-to-Drain			1.7		nC
Q <sub>gs</sub>	Gate Charge Gate-to-Source			2.5		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			1.3		nC
Q <sub>OSS</sub>	Output Charge		V <sub>DS</sub> = 13 V, V <sub>GS</sub> = 0 V		15	
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A, R <sub>G</sub> = 2 Ω		6.1		ns
t <sub>r</sub>	Rise Time			9.9		ns
t <sub>d(off)</sub>	Turn Off Delay Time			13.2		ns
t <sub>f</sub>	Fall Time			3.6		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>DS</sub> = 18 A, V <sub>GS</sub> = 0 V		0.85	1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = 13 V, I <sub>F</sub> = 18 A, di/dt = 300 A/μs		30		nC
t <sub>rr</sub>	Reverse Recovery Time			23		ns

### 5.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-Case Thermal Resistance <sup>(1)</sup>			2.0	°C/W
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance <sup>(1)(2)</sup>			57	

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), Cu pad on a 1.5 inches x 1.5 inches thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch<sup>2</sup> 2-oz.Cu.

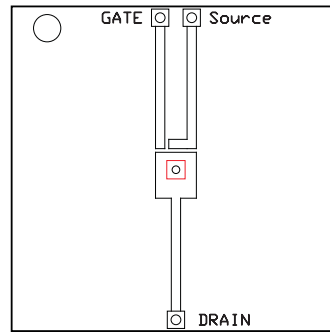
**CSD17309Q3**

SLPS261B – MARCH 2010 – REVISED SEPTEMBER 2014

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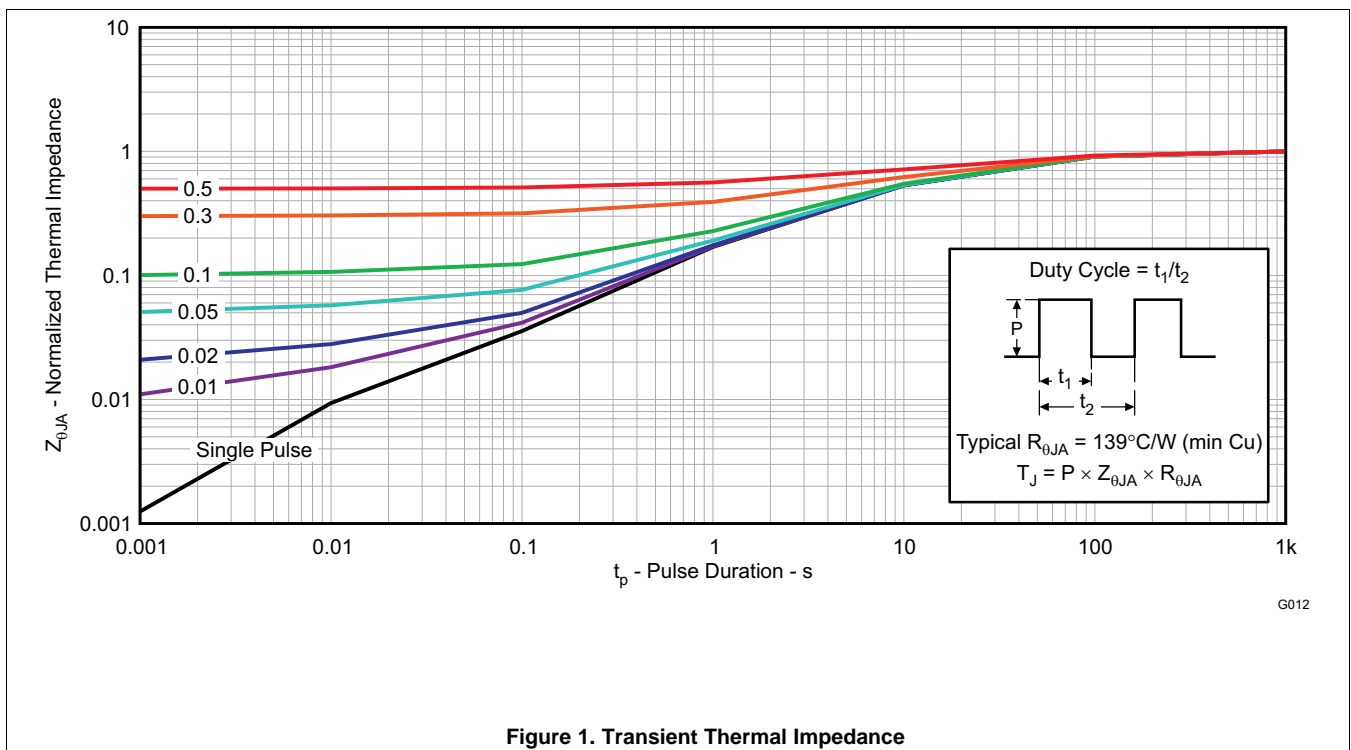
Max  $R_{\theta JA} = 57^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2 oz. (0.071 mm thick)  
Cu.



Max  $R_{\theta JA} = 174^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2 oz. (0.071 mm thick)  
Cu.

**5.3 Typical MOSFET Characteristics**

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

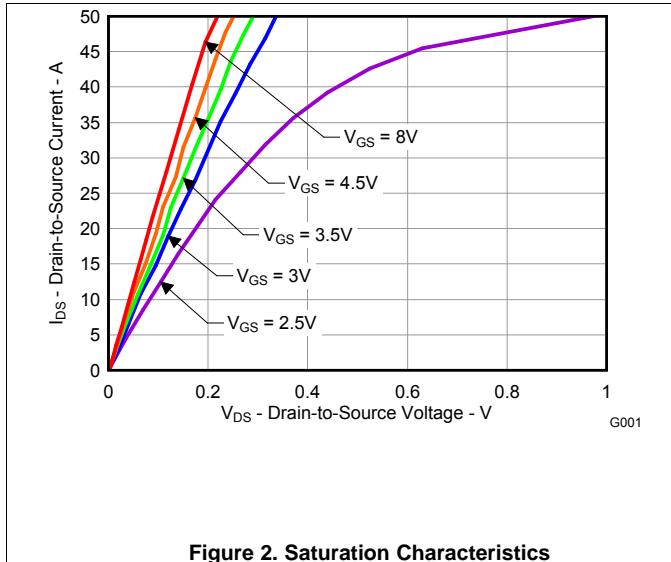


Figure 2. Saturation Characteristics

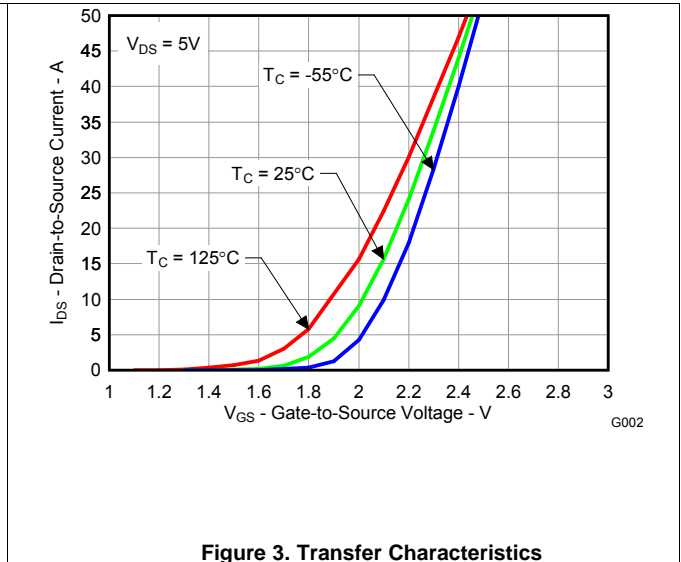


Figure 3. Transfer Characteristics

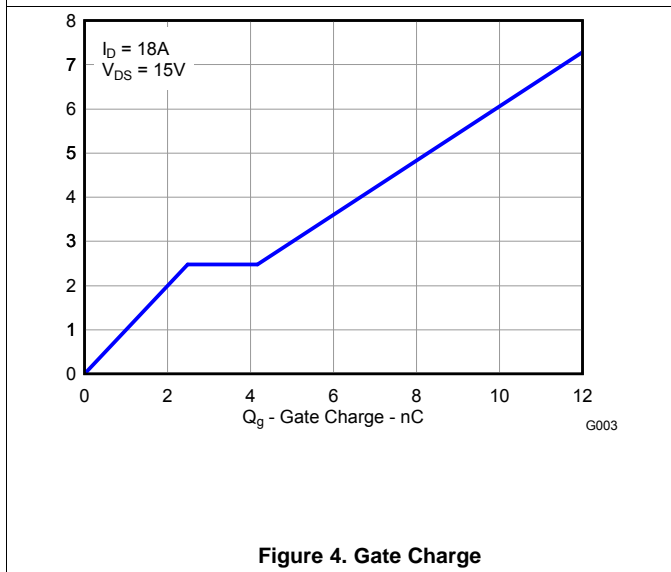


Figure 4. Gate Charge

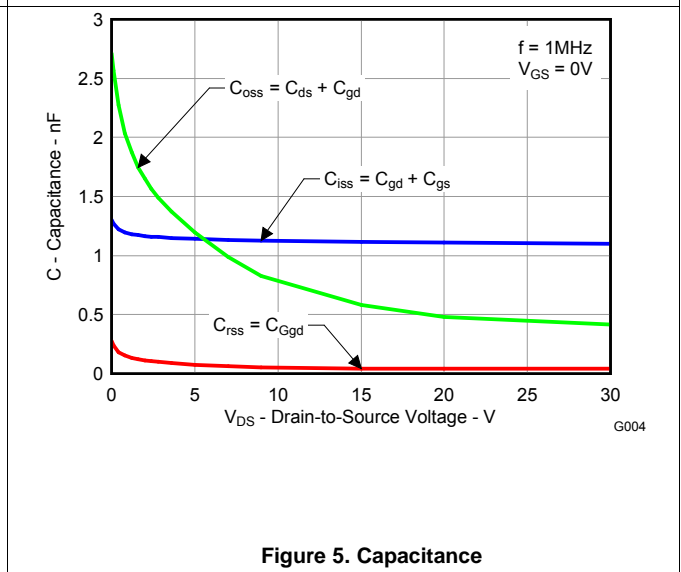
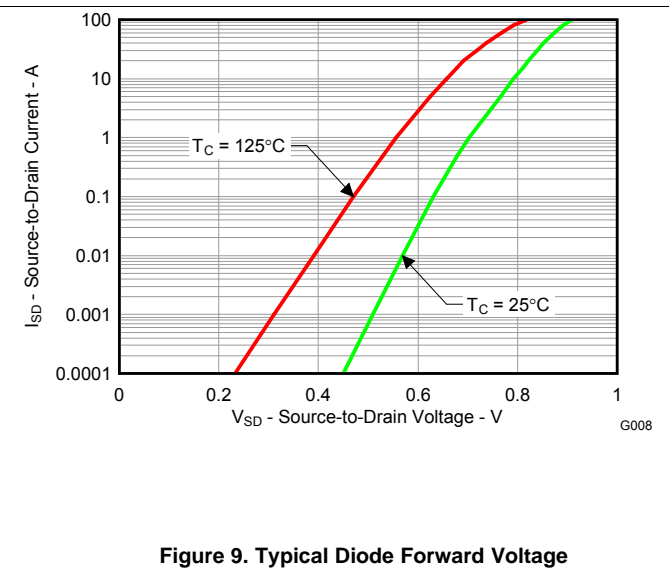
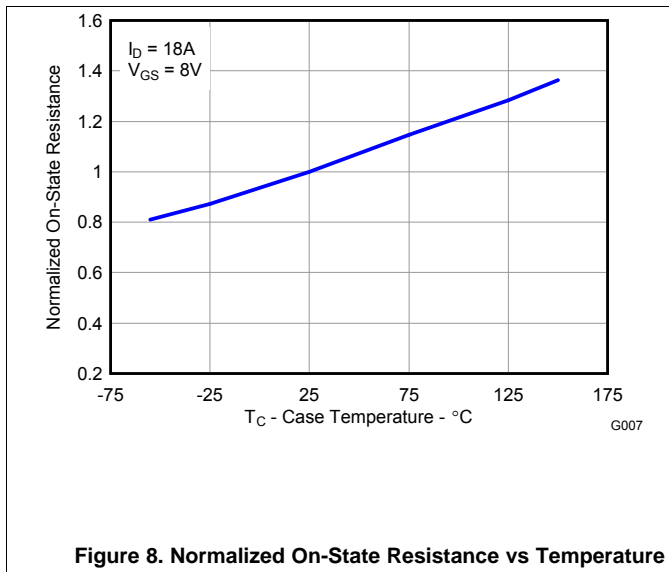
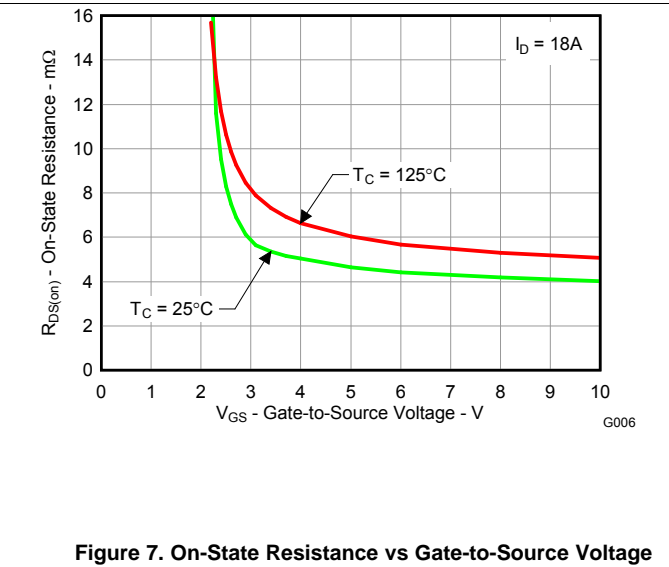
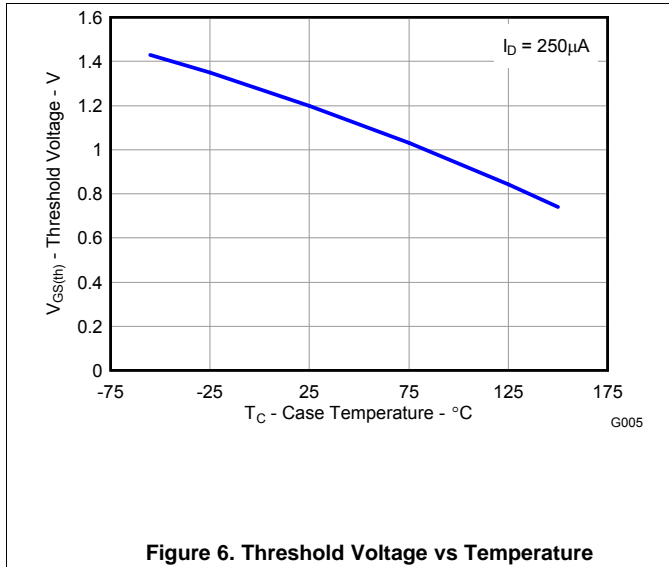


Figure 5. Capacitance

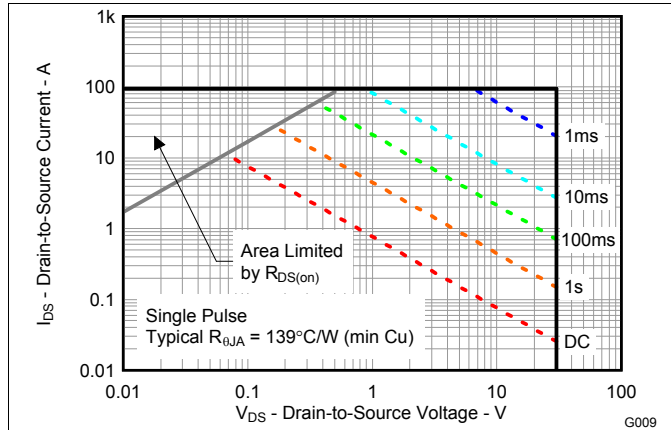
Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

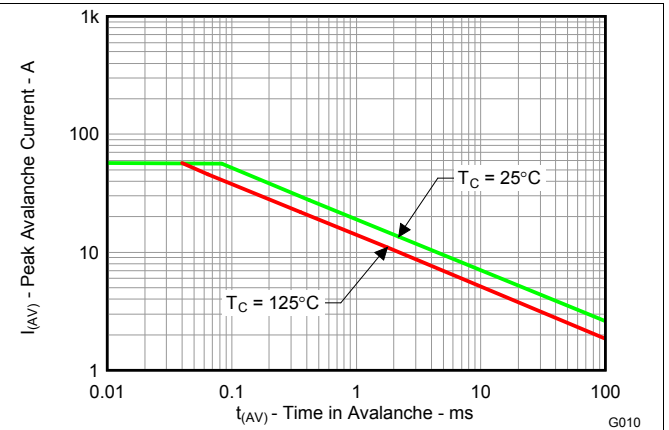


**Typical MOSFET Characteristics (continued)**

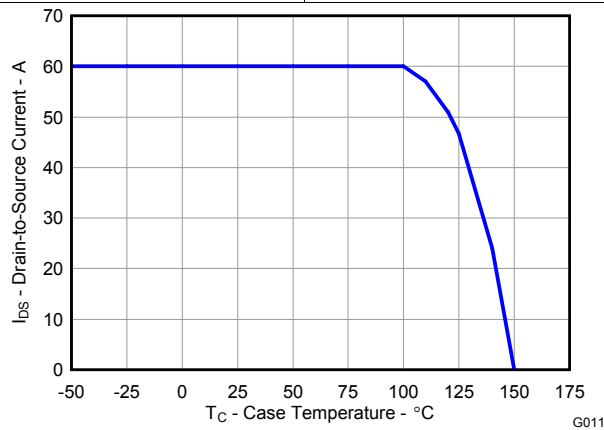
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



**Figure 10. Maximum Safe Operating Area (SOA)**



**Figure 11. Single Pulse Unclamped Inductive Switching**



**Figure 12. Maximum Drain Current vs Temperature**

## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

[SLYZ022](#) — *TI Glossary*.

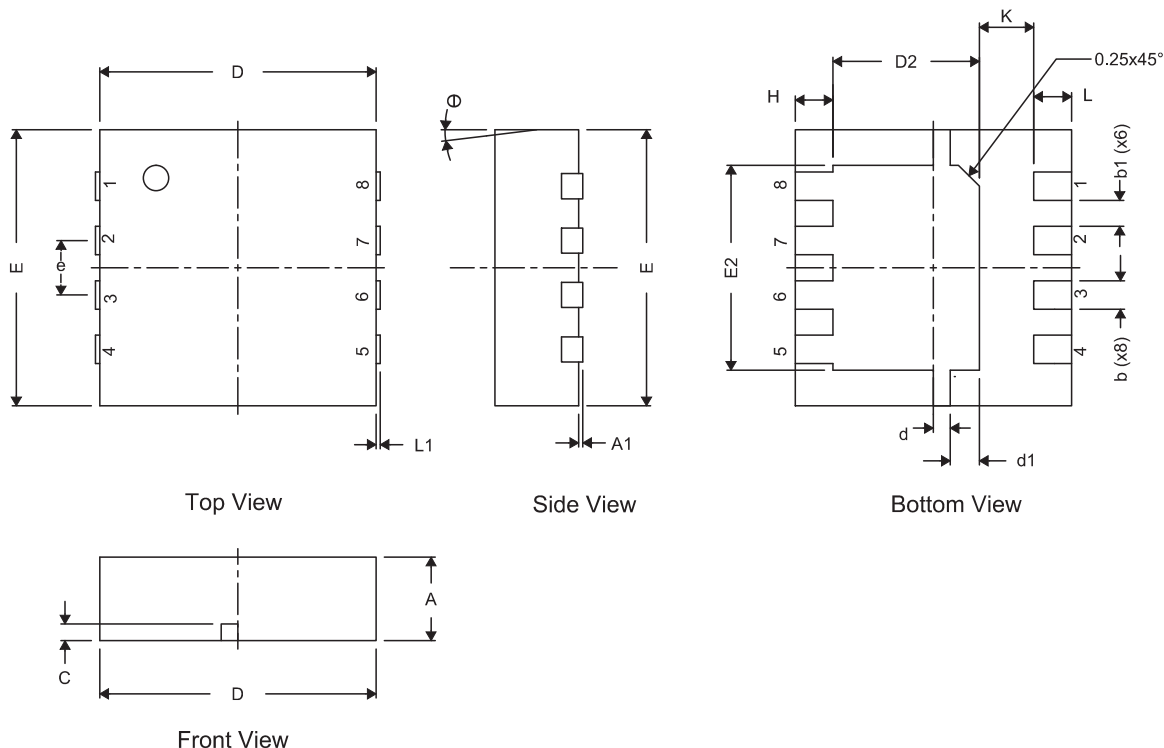
This glossary lists and explains terms, acronyms, and definitions.



## 7 Mechanical, Packaging, and Orderable Information

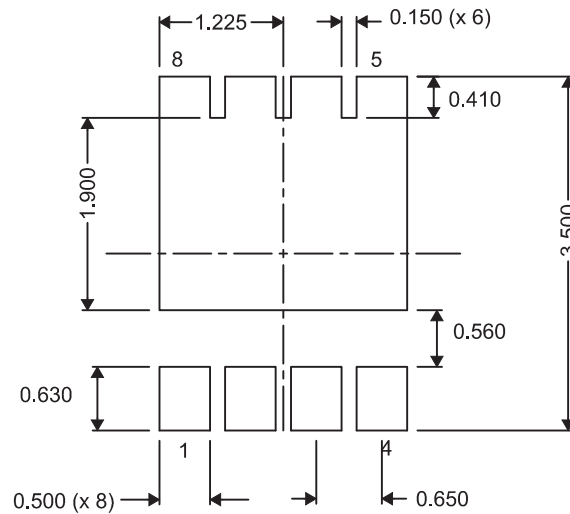
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q3 Package Dimensions



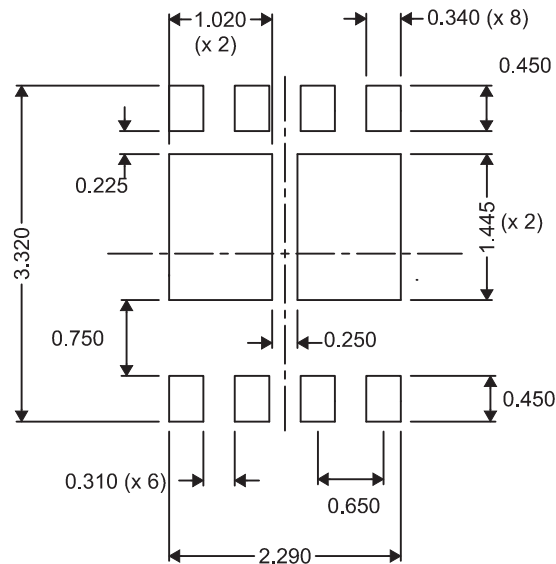
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
$\theta$	0	—	0	0	—	0

## 7.2 Recommended PCB Pattern



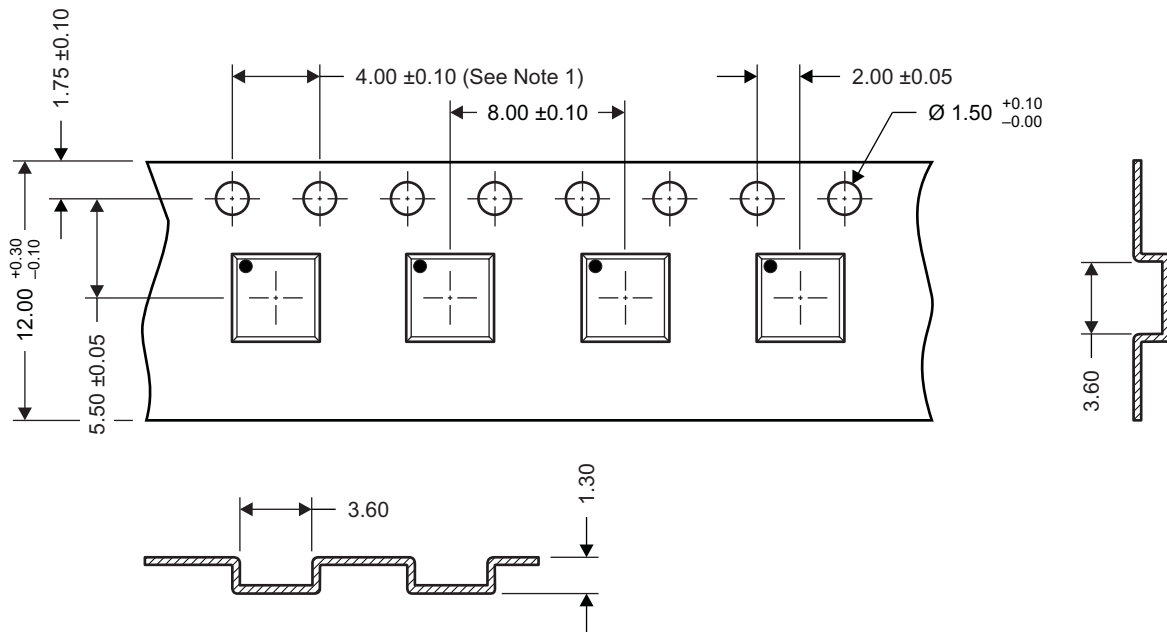
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

## 7.4 Q3 Tape and Reel Information



M0144-01

### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness:  $0.30 \pm 0.05$  mm
6. MSL1 260°C (IR and Convection) PbF-Reflow compatible

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17309Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	SN	Level-1-260C-UNLIM	-55 to 150	CSD17309	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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