SE8R01 specification

Version 2.2

2014/10/20

1 Introduction

The SE8R01 is a single chip 2.4GHz transceiver with an embedded baseband protocol engine, suitable for ultralow power wireless applications. The SE8R01 is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz.

To design a radio system with the SE8R01, you simply need an MCU (microcontroller) and a few external passive components.

You can operate and configure the SE8R01 through a Serial Peripheral Interface (SPI). The register mAp, which is accessible through the SPI, contains all configuration registers in the SE8R01 and is accessible in all operation modes of the chip.

The embedded baseband protocol engine is based on packet communication and supports various modes from mAnuAl operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Protocol engine reduces system cost by handling all the high speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate. SE8R01 supports an air data rate of 500kbps, 1Mbps and 2Mbps. The high air data rates combined with two power saving modes make the SE8R01 very suitable for ultralow power designs.

The addition of internal filtering to SE8R01 has improved the mArgins for meeting RF regulatory standards.

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

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1.1 Features

Features of the SE8R01 include:

- Radio:
  - Worldwide 2.4GHz ISM band operation
  - 126 RF channels
  - Common RX and TX interface
  - GFSK modulation
  - 500kbps, 1 and 2Mbps air data rate
  - 1MHz non-overlapping channel spacing at 1Mbps
  - 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter:
  - ProgrammAble output power: 0, -6, -12 or -18dBm。(6dBm@3V)
  - 16.5mA at 0dBm output power
- Receiver:
  - Fast AGC for improved dynamic range
  - Integrated channel filters
  - 18.5mA at 2Mbps
  - -83dBm sensitivity at 2Mbps
  - -88dBm sensitivity at 1Mbps
  - -90dBm sensitivity at 500kbps
- RF Synthesizer:
  - Fully integrated synthesizer
  - No external loop filer, VCO varactor diode or resonator
  - Accepts low cost ±60ppm 16MHz crystal
- Protocol engine:
  - 1 to 32 bytes dynamic payload length
  - AutomAtic packet handling
  - Auto packet transaction handling
  - 6 data pipe for 1:6 star networks
- Power mAnagement:
  - Integrated voltage regulator
  - 1.8 to 3.6V supply range
  - Idle modes with fast start-up times for advanced power mAnagement
  - 30μA Standby-I mode,4uA power down mode
  - Max 2ms start-up from power down mode
  - Max 210us start-up from standby-I mode
- Host Interface:
  - 4-pin hardware SPI
  - Max 10Mbps
  - 3 separate 32 bytes TX and RX FIFOs

- 5V tolerant IO

- Compact 20-pin 4x4mm QFN package:

1.2 Block

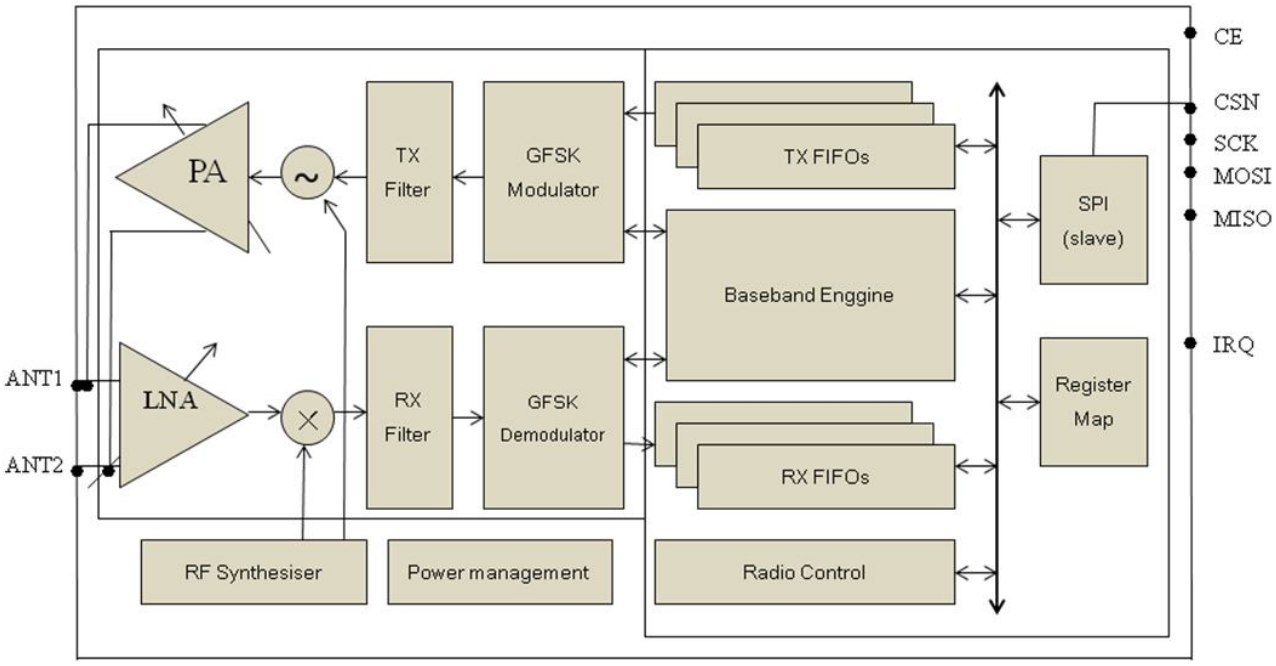


Figure1.1 SE8R01 block diagram

2 Pin InformAtion

2.1 Pin assignment

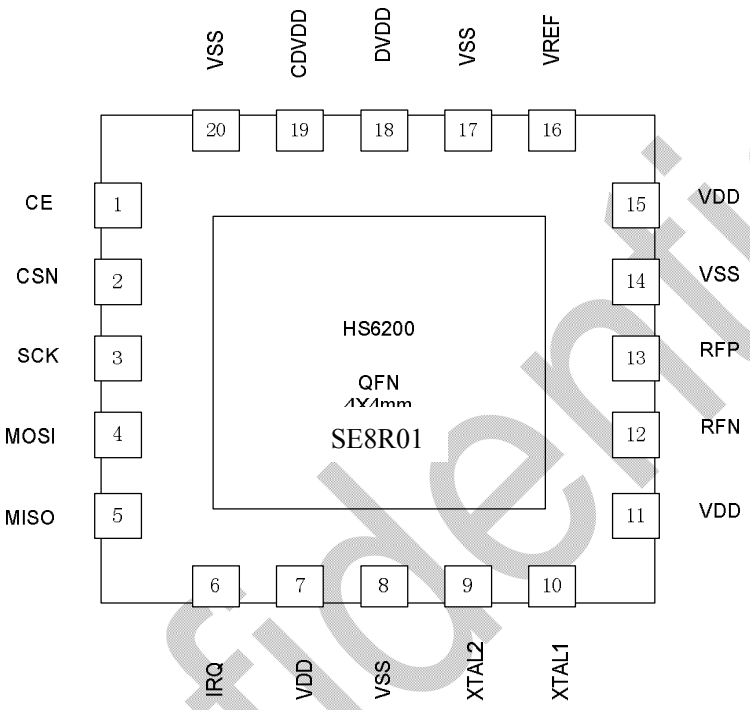
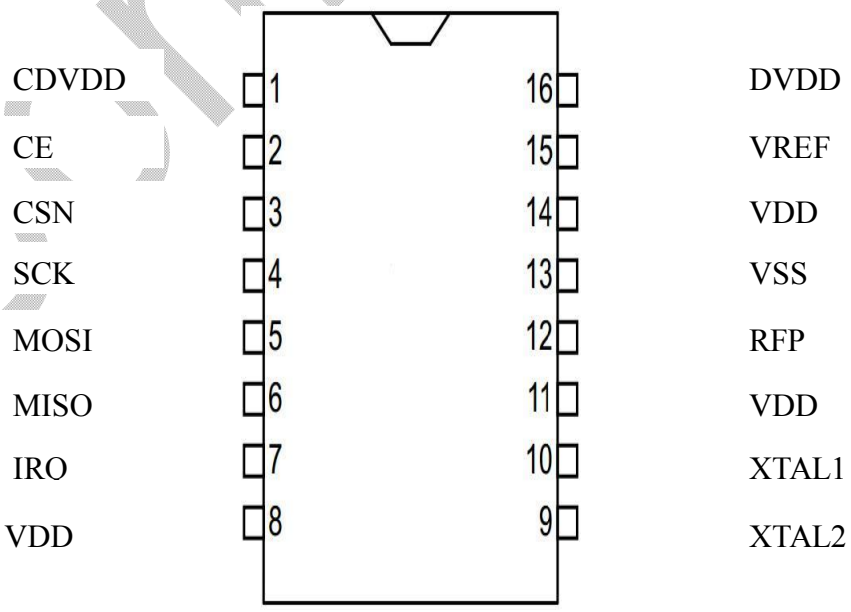


Figure2.1SE8R01 pin assignment (top view) for the QFN20 4x4 package



SE8R01 pin assignment (top view) for the SOP16 package

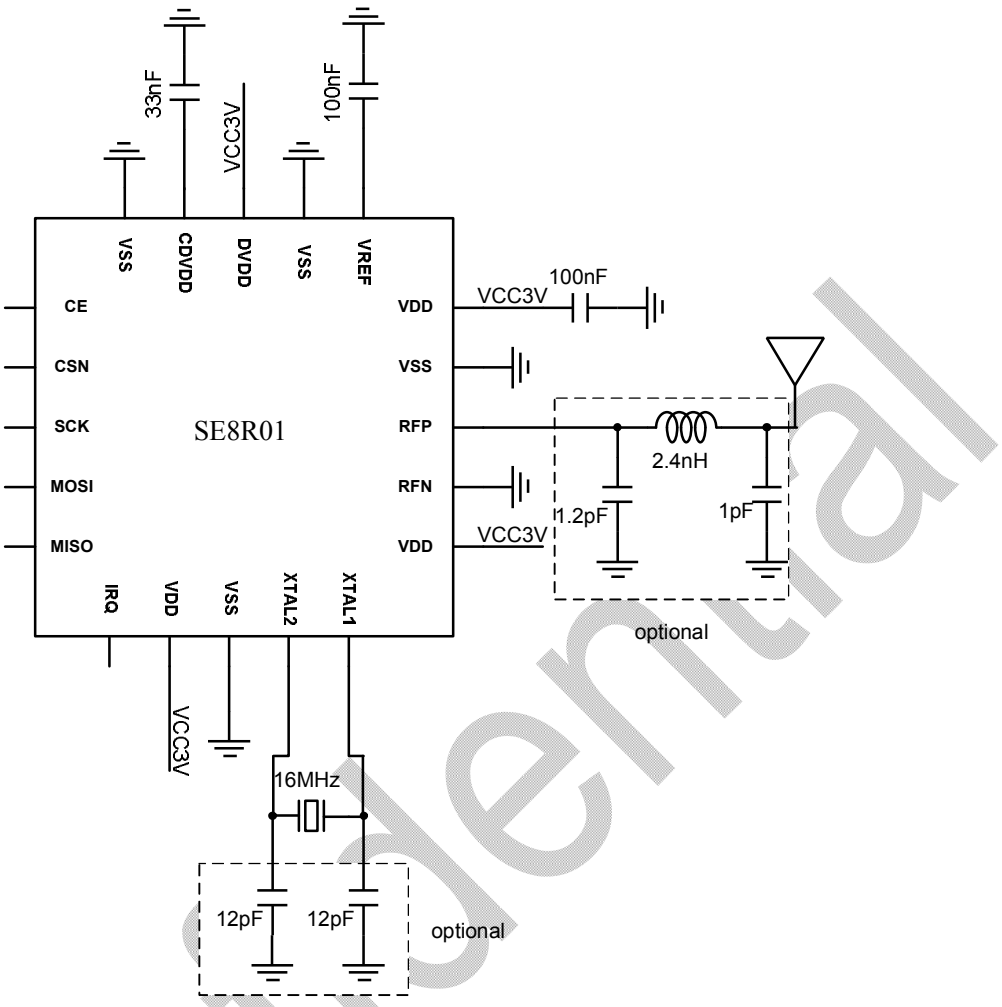


Figure 2.2 SE8R01application circuit

2.2 Pin functions

Pin	Name	Pin function	Description
1	CE	Digital Input	Chip Enable Activates RX or TX mode
2	CSN	Digital Input	SPI Chip Select
3	SCK	Digital Input	SPI Clock
4	MOSI	Digital Input	SPI Slave Data Input
5	MISO	Digital Output	SPI Slave Data Output, with tri-state option
6	IRQ	Digital Output	mAskable interrupt pin. Active low
7	VDD	Power	Power Supply (+1.8- +3.6V)
8	VSS	Power	Ground (0V)
9	XTAL2	Analog Output	Crystal Pin 2
10	XTAL1	Analog Input	Crystal Pin 1
11	VDD	Power	Power Supply (+1.8- +3.6V)

12	RFN	RF	Antenna interface 1
13	RFP	RF	Antenna interface 2
14	VSS	Power	Ground (0V)
15	VDD	Power	Power Supply (+1.8V - +3.6V)
16	VREF	Analog Input	Reference voltage. Connect a 100nFcapacitor to ground.
17	VSS	Power	Ground (0V)
18	DVDD	Power	Power Supply (+1.8V - +3.6V)
19	CDVDD	Power	Internal digital supply output for de-coupling purposes.
20	VSS	Power	Ground (0V)

Table2.1SE8R01 pin function

3 Absolute Maximum ratings

Note: Exceeding one or more of the limiting values mAy cause permAnent damAge to SE8R01.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
V_{DD}	-0.3	3.6	V
V_{SS}		0	V
Input voltage			
V_I	-0.3	5.25	V
Output voltage			
V_O	V_{SS} to V_{DD}	V_{SS} to V_{DD}	
Temperatures			
Operating Temperature	-40	+85	℃
Storage Temperature	-40	+125	℃

Table2.1 Absolute Maximum ratings

Symbol	Parameter(condition)	Notes	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage		1.8	3.0	3.6	V
V_{DD}	Supply voltage if input signals>3.6V		1.8	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	℃

Table 4.1 Operating conditions

4 Electrical specifications

Power Consumption

No.	Parameter	Symbol	Conditions	MIN	TYP	mAX	UNIT
1	Current in power down	Ipd	Leakage current		4		uA
2	Current in standby-I	Isb1	Only power up xtal		30		uA
3	Current in standby-II	Isb2	Power up xtal and buffer		900		uA
4	Current in TX 0dBm	Itx	PA under 0dBm		16.5		mA
5	Current in TX -18dBm	Itx	PA under -18dBm		12		mA
6	Current in RX 1Mbps	Irx	RX mode		18.5		mA
7	Current in RX 0.5Mbps	Irx	RX mode		18.5		mA
8	Operation frequency	Freq		2400		2525	MHz
9	PLL frequency step	Delta F			1		MHz
10	Freq deviation@500kbps	Df			160		KHz
11	Freq deviation@1Mbps	Df			160		KHz
12	Freq deviation@2Mbps	Df			320		KHz

Receiver performAnce

No.	Parameter	Symbol	Conditions	MIN	TYP	mAX	UNIT
1	Max RX signal	Pin,Max	<0.1% BER		-10		dBm
2	500Kbps	Sensitivity	<0.1%BER		-88		dBm
3	1Mbps	Sensitivity	<0.1%BER		-88		dBm
4	2Mbps	Sensitivity	<0.1%BER		-83		dBm

Transmitter performAnce

No.	Parameter	Symbol	Conditions	MIN	TYP	Max	UNIT
1	Max Output Power	PMax	50ohm antenna		0	+6	dBm
2	Min Output Power	Pmin	50ohm antenna		-18		dBm
3	RF power control range	Prange	50ohm antenna		26		Db

xtal performAnce

No.	Parameter	Symbol	Conditions	MIN	TYP	mAX	UNIT
1	Crystal Frequency	Fxtal		16	16	16	MHz
2	Tolerance	Dfxtal		-60		+60	ppm
3	Load capacitance	Cxtal			12		Pf

DC characteristic

No.	Parameter	Symbol	Conditions	MIN	TYP	mAX	UNIT
1	HIGH level input	Vhigh		0.7VDD		3.6	V
2	Low level input	Vlow		0		0.3VDD	V

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5 Radio Control

This chapter describes the SE8R01 radio transceiver's operating modes and the parameters used to control the radio.

The SE8R01 has a built-in state mAchine that controls the transitions between the chip's operating modes. The state mAchine takes input from user defined register values and internal signals.

5.1 Operational Modes

You can configure the SE8R01 in power down, standby, RX or TX mode. This section describes these modes in detail.

5.1.1 State diagram

Figure 6.1.shows the operating modes and how they function. There are three types of distinct states highlighted in the state diagram:

- Recommended operating mode: is a recommended state used during normAl operation.
- Possible operating mode: is a possible operating state, but is not used during normAl operation.
- Transition state: is a time limited state used during start up of the oscillator and settling of the PLL.

When the VDD reaches 1.8V or higher SE8R01 enters the Power on reset state where it remAins in reset until entering the Power Down mode.

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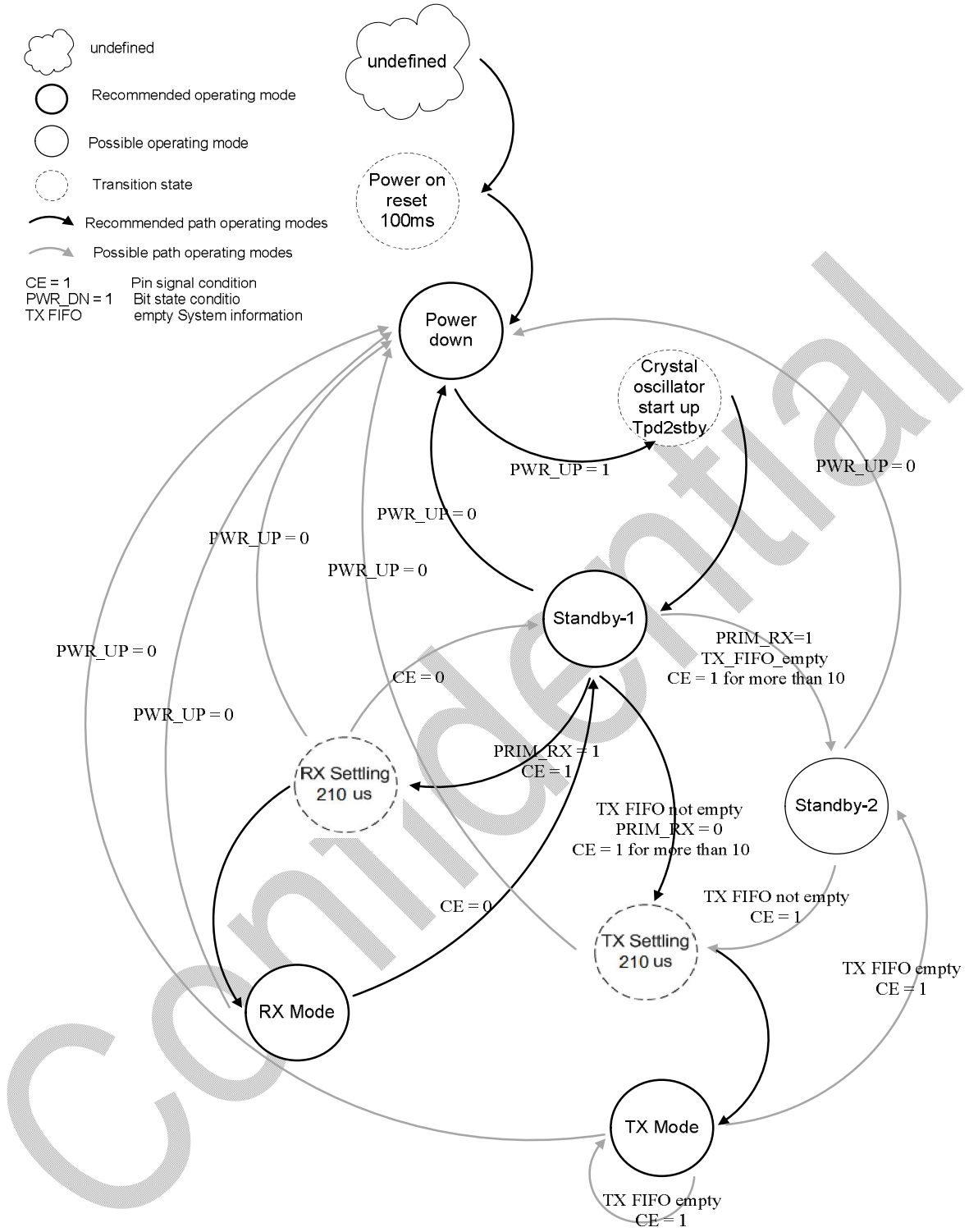

Figure 6.1 Radio control state diagram

5.1.2 Power Down Mode

In power down mode, the SE8R01 is disabled using minimize average current consumption. All register values available are mAintained and the SPI is kept active, enabling change of configuration and the uploading/down-loading of data registers. For starting up times see Table6.2 .Power down mode is entered by setting the PWR_UP bit in the CONFIG register low.

5.1.3 Standby Modes

5.1.3.1 Standby-I mode

By setting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while mAintaining short start up times. In this mode only part of the crystal oscillator is active. Change to active modes only happens if CE is set high and when CE is set low, the SE8R01 returns to standby-I mode from both the TX and RX modes.

5.1.3.2 Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. The SE8R01 enters standby-II mode if CE is held high on a PTX device with an empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normAl PLL settling delay (210μs). Register values are mAintained and the SPI can be activated during both standby modes.

Notice: From *Standby-I mode to standby-II mode CE more than 20us*

5.1.4 RX mode

The RX mode is an active mode where the SE8R01 radio is used as a receiver. To enter this mode, the chip must have the PWR_UP bit, PRIM_RX bit and the CE pin set high.

In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a mAtching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.

The chip remAins in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automAtic protocol features in the baseband protocol engine are enabled, the chip can enter other modes in order to execute the protocol.

In RX mode a Received Power Detector (RPD) signal is available. The RPD register is a signed number which corresponds to different level of received power in dBm. The highest bit of RPD is sign bit. The range of the received power is -100 ~ +10dBm. The RPD has about +/-5dBm deviation from the real level.

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5.1.5 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the chip must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and a high pulse on the CE for more than 20μs.

The SE8R01 stays in TX mode until it finishes transmitting a packet. If CE = 0, the chip returns to standby-I mode. If CE = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the SE8R01 remAins in TX mode and transmits the next packet. If the TX FIFO is empty the chip goes into standby-II mode.

5.1.6 Operational modes configuration

The following (table 6.1) describes how to configure the operational modes:

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data TX FIFO. Will empty all level in TX FIFOs[a]
TX mode	1	0	Minimum 20us high pulse	Data TX FIFO. Will empty one level in TX FIFOs[b]
Standby-2	1	0	1	TX FIFO empty
Standby-1	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

Table6.1 the SE8R01 mAin modes

a. If CE is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the CE is still high, the chip enters standby-II mode. In this mode the transmission of a packet is started as soon as the CSN is set high after an upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the CE high for at least 20μs. This allows one packet to be transmitted. This is the normAl operating mode. After the packet is transmitted, the chip enters standby-1mode.

5.1.7 Timing InformAtion

The timing informAtion in this section relates to the transitions between modes and the timing for the CE pin. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby modes to TX mode or RX mode (Max.210μs), as described in Table6.2

Name	The chip	Notes	Max.	Min.	Comments
$T_{pd2stby}$	Power down→Standby mode		150us		With external clock
		a	2ms		External crystal, Ls< 30Mh
			3ms		External crystal, Ls< 60Mh
			4.5ms		External crystal, Ls< 90Mh
T_{stby2a}	Standby mode→TX/RX mode		210us		

T_{hce}	Minimum CE high			20us	
$T_{pece2csn}$	Delay from CE positive edge to CSN low			4us	

a. See crystal specifications.

Table6.2 operational timing of the SE8R01 chip

For SE8R01 to go from power down mode to TX or RX mode it must first pass through stand-by mode. There must be a delay of $T_{pd2stby}$ (see Table 6.2) after the SE8R01 leaves power down mode before the CE is set high.

Note: If VDD is turned off the register value is lost and you must configure chip before entering the TX or RX modes.

5.2 Air data rate

The air data rate is the modulated signaling rate the chip uses when transmitting and receiving data. It can be 500kbps, 1Mbps or 2Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions. The air data rate is set by the RF_DR bit in the RF_SETUP register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

5.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the chip. The channel occupies a bandwidth of less than 1MHz at 500kbps and 1Mbps and a bandwidth of less than 2MHz at 2Mbps. The chip can operate on frequencies from 2.400GHz to2.525GHz. The programming resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps, the channel bandwidth is the same or lower than the resolution of the RF frequency.

The RF channel frequency is set by the RF_CH register according to the following formula:

$$F_0 = 2400 + RF\_CH\ [MHz]$$

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

5.4 Received Power Detector measurements

Received Power Detector (RPD), located in register 09, is a signed number which corresponds to different level of received power in dBm. The highest bit of RPD is sign bit. The range of the received power is -100 ~ +10dBm.

The RPD can be read out at any time while the chip is in received mode. This offers a snapshot of the current received power level in the channel. The status of RPD is correct when RX mode is enabled and after a wait time of $T_{stby2a} + T_{delay\_AGC}$= 210us + 20us. The RX gain varies over temperature which means that the RPD value also varies over temperature.

5.5 PA control

The PA (Power Amplifier) control is used to set the output power from the chip power amplifier. In TX mode PA control has four programmAble steps, see Table 6.3.

The PA control is set by the PA_PWR bits in the RF_SETUP register.

PA_PWR[3:0]	Pa_voltage(bank1 of RF_IVGEN)	RF output power(DC current consumption)
1111	0	Output 6 dbm, 40mA
1000	0	Output 5 dbm
0111	1	Output 4 dbm, 25mA
0011	0	Output 0 dbm, 18.5mA
0001	0	Output -6 dbm
0001	1	Output -12 dbm
0000	0	Output -16 dbm
0000	1	Output -43 dbm

Conditions: VDD = 3.0V, VSS = 0V, TA = 27ºC

Note: set PA_PWR[3:0] to 1111 can obtain Maximum +6dBm output power

Table 6.3 RF output power setting for the SE8R01

5.6 RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the SE8R01 chip in transmit/receive mode.

6 Protocol Engine

Protocol engine is a packet based data link layer that features automAtic packet assembly and timing, automAtic acknowledgement and retransmissions of packets. Protocol engine enables the implementation of ultralow power and high performAnce communication. The Protocol engine features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

6.1 Features

The mAin features of Protocol engine are:

- 1 to 32 bytes dynamic payload length
- AutomAtic packet handling
- AutomAtic packet transaction handling
  - Auto Acknowledgement with payload
  - Auto retransmit
- 6 data pipe for 1:6 star networks

6.2 Protocol engine overview

Protocol engine uses self defined protocol for automAtic packet handling and timing. During transmit, Protocol engine assembles the packet and clocks the bits in the data packet for transmission. During receive, Protocol engine constantly searches for a valid address in the demodulated signal. When Protocol engine finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into a vacant slot in the RX FIFOs. All high speed bit handling and timing is controlled by protocol engine.

Protocol engine features automAtic packet transaction handling for the easy implementation of a reliable bi-directional data link. A protocol engine packet transaction is a packet exchange between two transceivers, with one transceiver acting as the PrimAry Receiver (PRX) and the other transceiver acting as the PrimAry Transmitter (PTX). A protocol engine packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an acknowledgment packet (ACK packet) from the PRX. The PRX can attach user data to the ACK packet enabling a bi-directional data link.

The automAtic packet transaction handling works as follows:
1. You begin the transaction by transmitting a data packet from the PTX to the PRX. Protocol engine automAtically sets the PTX in receive mode to wait for the ACK packet.
2. If the packet is received by the PRX, Protocol engine automAtically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode.
3. If the PTX does not receive the ACK packet immediately, Protocol engine automAtically retransmits the original data packet after a programmAble delay and sets the PTX in receive mode to wait for the ACK packet.
In Protocol engine it is possible to configure parameters such as the Maximum number of retransmits and the delay from one transmission to the next retransmission. All automAtic handling is done without the involvement of the MCU.

6.3 Protocol engine packet formAt

The formAt of the Protocol engine packet is described in this section. The Protocol engine packet contains a preamble field, address field, packet control field, payload field and a CRC field. Figure7.1 shows the packet formAt with MSB to the left.

Preamble 1 byte	Address 4-5 byte	2byte guArd	Packet control field 9 bit	Payload 0-32 bytes	CRC 1-2 bytes

Figure7.1 A Protocol engine packet with payload (0-32 bytes)

6.3.1 Preamble

The preamble is a bit sequence used to synchronize the receivers demodulator to the incoming bit stream. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automAtically set to 10101010 and if the first bit is 0 the preamble is automAtically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

6.3.2 Address

This is the address for the receiver. An address ensures that the packet is detected and received by the correct receiver, preventing accidental cross talk between multiple SE8R01 systems. You can configure the address field width in the AW register to be 5 bytes or 4 bytes address.

6.3.3 GuArd

Figure 7.1 shows the formAt of the 2 bytes guArd packet has better synchronous characteristics.

6.3.4 Packet Control Field (PCF)

Figure 7.2 shows the formAt of the 9 bit packet control field, MSB to the left.

Payload length 6bit	PID 2bit	NO_ACK 1bit

Figure 7.2 Packet control field (PCF)

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit NO_ACK flag.

6.3.4.1 Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

Coding: 000000 = 0 byte (only used in empty ACK packets. The 0 length packet also need to be read out use R_RX_PAYLOAD with no data following) 100000 = 32 byte, 100001 = Don't care.

This field is only used if the Dynamic Payload Length function is enabled.

6.3.4.2 PID (Packet identification)

The 2 bit PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX operation from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC field are used by the PRX operation to determine if a packet is retransmitted or new. When several data packets are lost on the link, the PID fields mAy become equAl to the last received PID. If a packet has the same PID as the previous packet, the RF transceiver compares the CRC sums from both packets. If the CRC sums are also equAl, the last received packet is considered a copy of the previously received packet and discarded.

6.3.4.3 No Acknowledgment flag (NO_ACK)

The Selective Auto Acknowledgement feature controls the NO_ACK flag.

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This flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

On the PTX you can set the NO_ACK flag bit in the Packet Control Field with this commAnd:
W_TX_PAYLOAD_NOACK

However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option, the PTX goes directly to standby-I mode after transmitting the packet. The PRX does not transmit an ACK packet when it receives the packet.

6.3.5 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air when it is uploaded to the device.

Protocol engine provides two alternatives for handling payload lengths; static and dynamic.

The default is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equAl the value in the RX_PW_Px register on the receiver side.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means that for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With the DPL feature the SE8R01 can decode the payload length of the received packet automAtically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the R_RX_PL_WID commAnd.

> ***Note:*** Always check if the packet width reported is 32 bytes or shorter when using the R_RX_PL_WID commAnd. If its width is longer than 32 bytes then the packet contains errors and must be discarded. Discard the packet by using the Flush_RX commAnd.

In order to enable DPL the EN_DPL bit in the FEATURE register must be enabled. In RX mode the DYNPD register must be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

6.3.6 CRC (Cyclic Redundancy Check)

The CRC is the error detection mechanism in the packet. It mAy either be 1 or 2 bytes and is calculated over the address, Packet Control Field and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value 0Xff.

The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value 0Xffff.

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The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. No packet is accepted by protocol engine if the CRC fails.

6.3.7 AutomAtic packet assembly

The automAtic packet assembly assembles the preamble, address, packet control field, payload and CRC to mAke a complete packet before it is transmitted.

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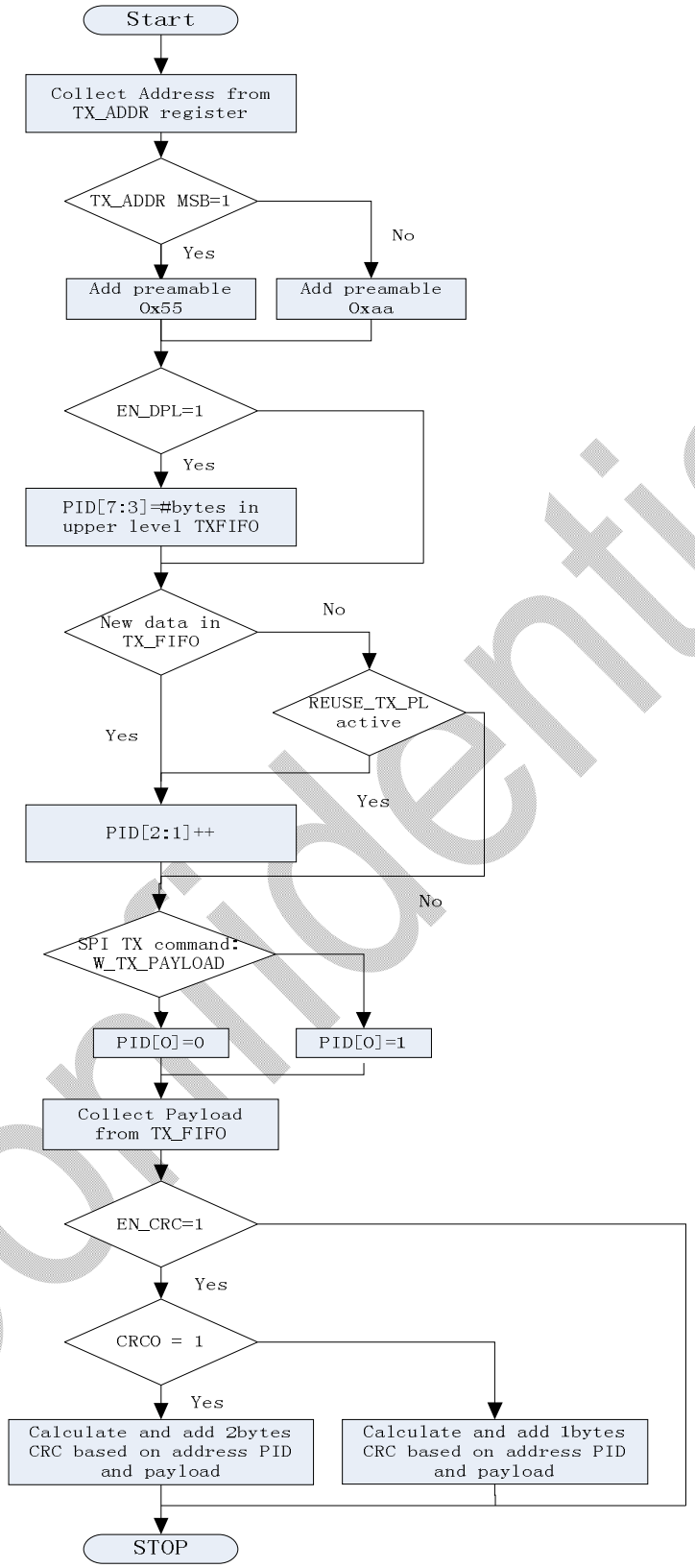

Figure 7.3AutomAtic packet assembly

6.3.8 AutomAtic packet disassembly

After the packet is validated, Protocol engine disassembles the packet and loads the payload into the RX FIFO, and asserts the RX_DR IRQ.

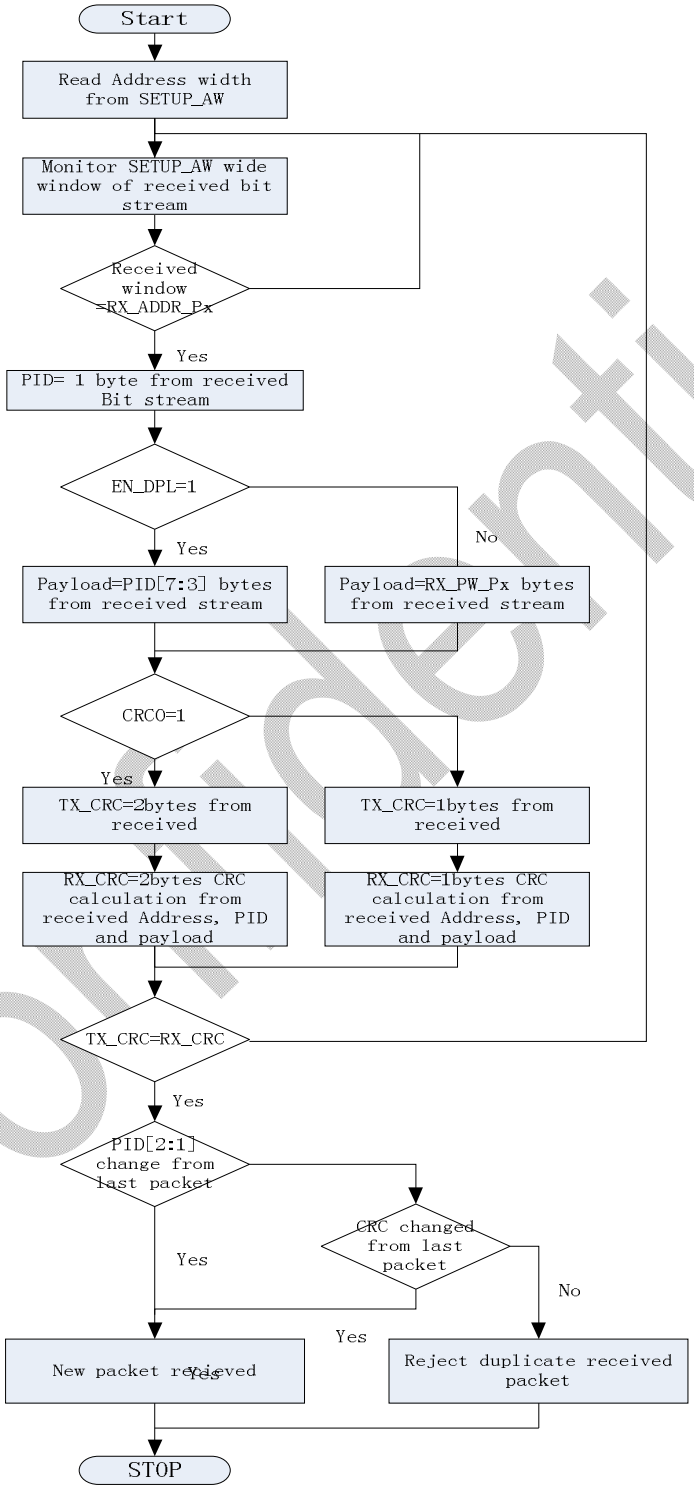

Figure 7.4AutomAtic packet disassembly

6.4 AutomAtic packet transaction handling

Protocol engine features two functions for automAtic packet transaction handling; auto acknowledgement and auto re-transmit.

6.4.1 Auto Acknowledgement

Auto Acknowledgment is a function that automAtically transmits an ACK packet to the PTX after it has received and validated a packet. The Auto Acknowledgement function reduces the load of the system MCU and reduces average current consumption. The Auto Acknowledgement feature is enabled by setting the EN_AA register.

Note: If the received packet has the NO_ACK flag set, auto acknowledgement is not executed.

An ACK packet can contain an optional payload from PRX to PTX. In order to use this feature, the Dynamic Payload Length (DPL) feature must be enabled. The MCU on the PRX side has to upload the payload by clocking it into the TX FIFO by using the W_ACK_PAYLOAD commAnd. The payload is pending in the TX FIFO (PRX) until a new packet is received from the PTX. The RF transceiver can have three ACK packet payloads pending in the TX FIFO (PRX) at the same time.

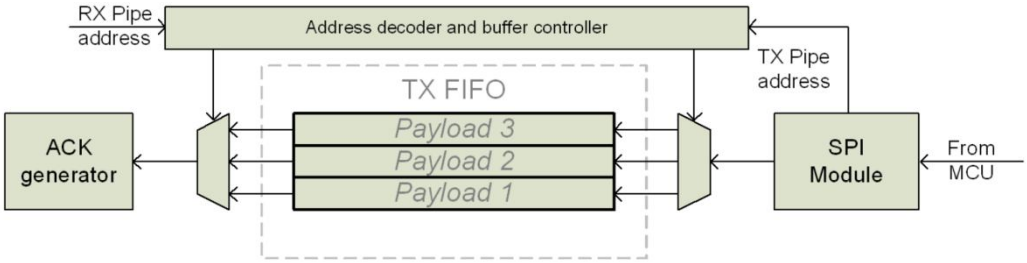

Figure 7.5TX FIFO (PRX) with pending payloads

Figure 7.5shows how the TX FIFO (PRX) is operated when handling pending ACK packet payloads. From the MCU the payload is clocked in with the W_ACK_PAYLOAD commAnd. The address decoder and buffer controller ensure that the payload is stored in a vacant slot in the TX FIFO (PRX). When a packet is received, the address decoder and buffer controller are notified with the PTX address. This ensures that the right payload is presented to the ACK generator.

If the TX FIFO (PRX) contains more than one payload to a PTX, payloads are handled using the first in–first out principle. The TX FIFO (PRX) is blocked if all pending payloads are addressed to a PTX where the link is lost. In this case, the MCU can flush the TX FIFO (PRX) by using the FLUSH_TX commAnd.

In order to enable Auto Acknowledgement with payload the EN_ACK_PAY bit in the FEATURE register must be set.

6.4.2 Auto Retransmission (ART)

The auto retransmission is a function that retransmits a packet if an ACK packet is not received. It is used in an Auto Acknowledgement system on the PTX. When a packet is not acknowledged, you can set the number of times it is allowed to retransmit by setting the ARC bits in the SETUP_RETR register. PTX enters RX mode and waits a time period for an ACK packet each time a packet is transmitted. The amount of time the PTX is in RX mode is based on the following conditions:

- Auto Retransmit Delay (ARD) has elapsed.
- No address mAtch within 256 μs.

- After received packet (CRC correct or not) if address mAtch within 256 µs.

The RF transceiver asserts the TX_DS IRQ when the ACK packet is received.

The RF transceiver enters standby-I mode if there is no more un-transmitted data in the TX FIFO and the CE pin is low. If the ACK packet is not received, the RF transceiver goes back to TX mode after a delay defined by ARD and retransmits the data. This continues until acknowledgment is received, or the Maximum number of retransmits is reached.

Two packet loss counters are incremented each time a packet is lost, ARC_CNT and PLOS_CNT in the OBSERVE_TX register. The ARC_CNT counts the number of retransmissions for the current transaction. You reset ARC_CNT by initiating a new transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. You reset PLOS_CNT by writing to the RF_CH register. It is possible to use the informAtion in the OBSERVE_TX register to mAke an overall assessment of the channel quAlity.

The ARD defines the time from the end of a transmitted packet to when a retransmit starts on the PTX. ARD is set in SETUP_RETR register in steps of 256µs. A retransmit is mAde if no ACK packet is received by the PTX.

There is a restriction on the length of ARD when using ACK packets with payload. The ARD time must never be shorter than the sum of the startup time and the time on-air for the ACK packet.

- For 2 Mbps data rate and 5-byte address; 15 byte is Maximum ACK packet payload length for ARD=256µs (reset value).
- For 1 Mbps data rate and 5-byte address; 5 byte is Maximum ACK packet payload length for ARD=256µs (reset value).

ARD=512µs is long enough for any ACK payload length in 1 or 2 Mbps mode.

- For 500kbps data rate and 5-byte address the following values apply:

ARD	ACK packet size (in byte)
1536us	All ACK payload sizes
1280us	<=24
1024us	<=16
768us	<=8
512us	Empty ACK with no payload

Table 7.1 Maximum ACK payload length for different retransmit delays

As an alternative to Auto Retransmit it is possible to mAnuAlly set the RF transceiver to retransmit a packet a number of times. This is done by the REUSE_TX_PL commAnd. The MCU must initiate each transmission of the packet with a pulse on the CE pin when this commAnd is used.

6.5 Protocol engine flowcharts

This section contains flowcharts outlining PTX and PRX operation in Protocol engine.

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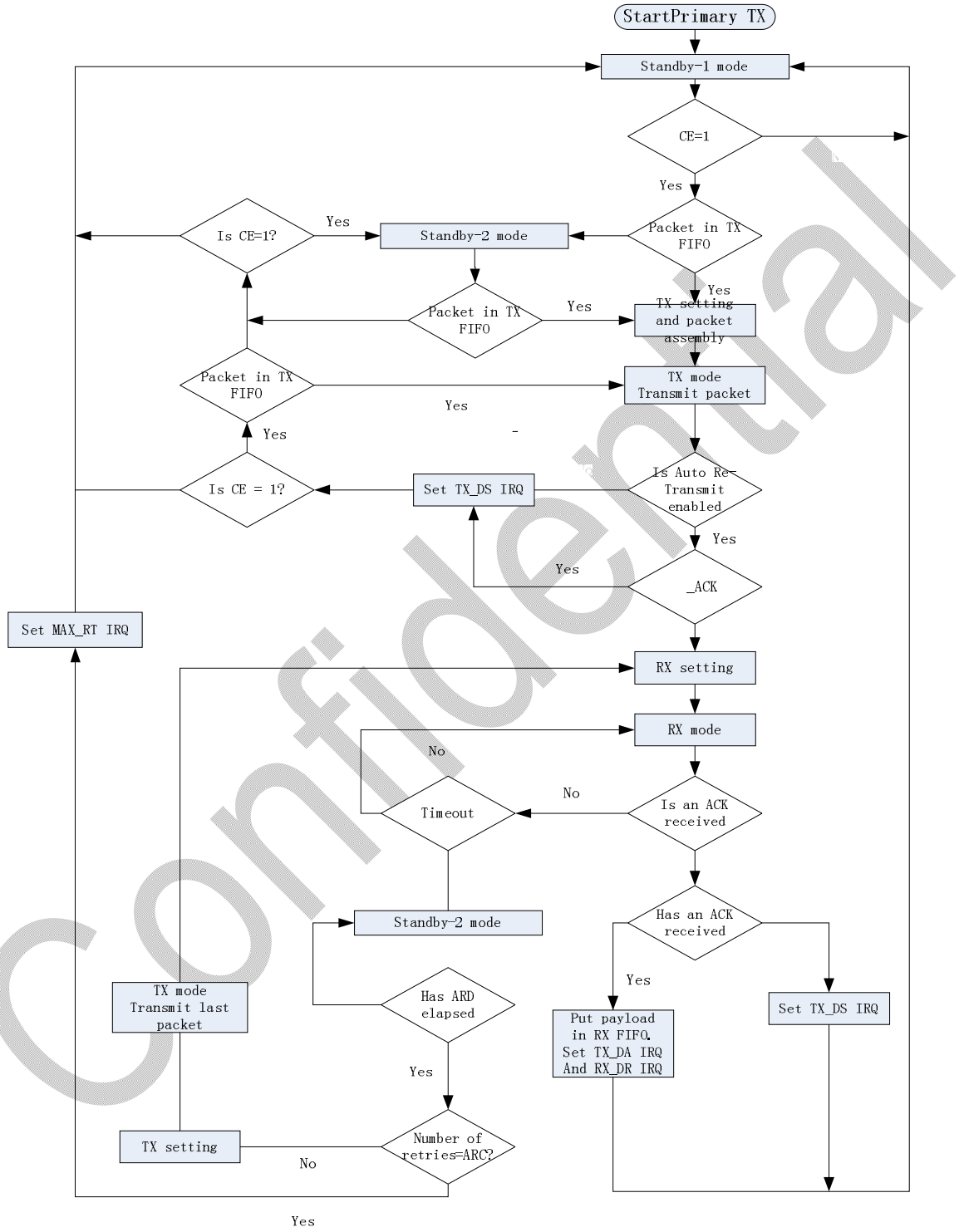
6.5.1 PTX operation

The flowchart in Figure 7.6 outlines how a RF transceiver configured as a PTX behaves after entering standby-I mode.



Note: Protocol engine operation is outlined with a dashed squAre.

Figure 7.6 PTX operations in Protocol engine

Activate PTX mode by setting the CE high. If there is a packet present in the TX FIFO the RF transceiver enters TX mode and

transmits the packet. If Auto Retransmit is enabled, the state mAchine checks if the NO_ACK flag is set. If it is not set, the RF transceiver enters RX mode to receive an ACK packet. If the received ACK packet is empty, only the TX_DS IRQ is asserted. If the ACK packet contains a payload, both TX_DS IRQ and RX_DR IRQ are asserted simultaneously before the RF transceiver returns to standby-I mode.

If the ACK packet is not received before timeout occurs, the RF transceiver returns to standby-II mode. It stays in standby-II mode until the ARD has elapsed. If the number of retransmits has not reached the ARC, the RF transceiver enters TX mode and transmits the last packet once more.

While executing the Auto Retransmit feature, the number of retransmits can reach the Maximum number defined in ARC. If this happens, the RF transceiver asserts the mAX_RT IRQ and returns to standby-I mode.

If the CE bit in the RFCON register is high and the TX FIFO is empty, the RF transceiver enters Standby-II mode.

6.5.2 PRX operation

The flowchart in Figure 7.7 outlines how a RF transceiver configured as a PRX behaves after entering standby-I mode.

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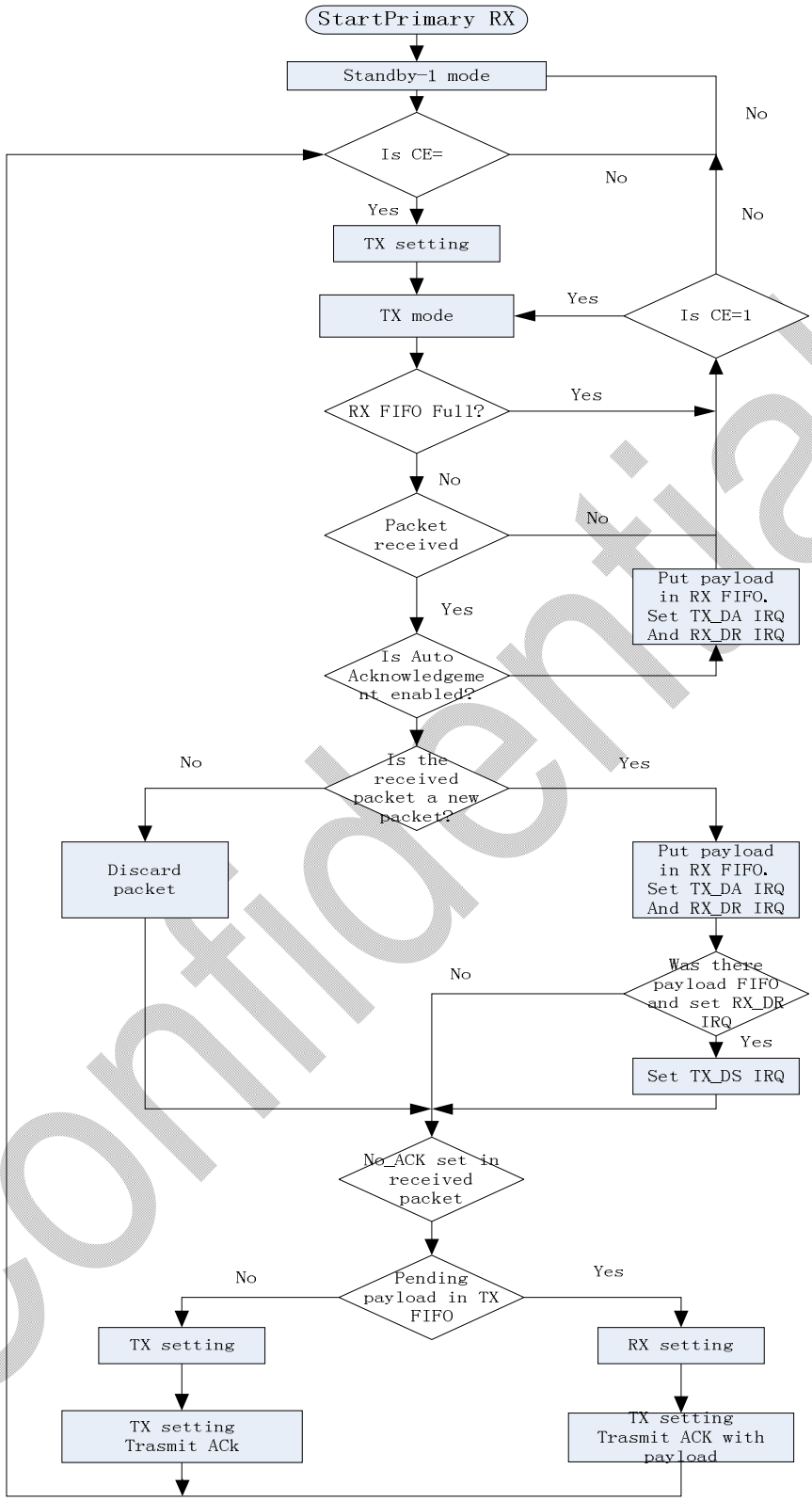


Note: Protocol engine operation is outlined with a dashed squAre.

Figure7.7 PRX operations in Protocol engine

Activate PRX mode by setting the CE bit in the RFCON register high. The RF transceiver enters RX mode and starts searching for packets. If a packet is received and Auto Acknowledgement is enabled, the RF transceiver decides if the packet is new or a copy of a

previously received packet. If the packet is new payload is mAde available in the RX FIFO and the RX_DR IRQ is asserted. If the last received packet from the transmitter is acknowledged with an ACK packet with payload, the TX_DS IRQ indicates that the PTX received the ACK packet with payload. If the No_ACK flag is not set in the received packet, the PRX enters TX mode. If there is a pending payload in the TX FIFO it is attached to the ACK packet. After the ACK packet is transmitted, the RF transceiver returns to RX mode.

A copy of a previously received packet might be received if the ACK packet is lost. In this case, the PRX discards the received packet and transmits an ACK packet before it returns to RX mode.

6.6 MultiSlave

MultiSlave is a feature used in RX mode that contains a set of six parallel data pipes with unique addresses. A data pipe is a logical channel in the physical RF channel. Each data pipe has its own physical address (data pipe address) decoding in the RF transceiver.

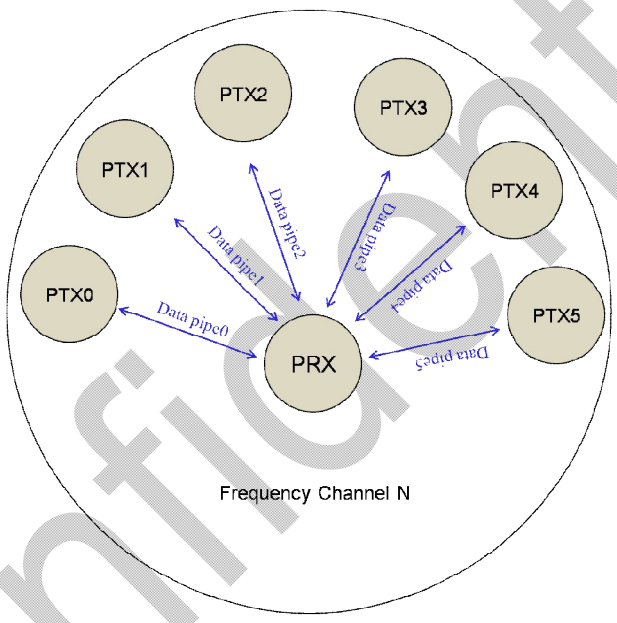


Figure7.8 PRX using MultiSlave

The RF transceiver configured as PRX (primAry receiver) can receive data addressed to six different data pipes in one frequency channel as shown in Figure 7.8. Each data pipe has its own unique address and can be configured for individuAl behavior.

Up to six RF transceivers configured as PTX can communicate with one RF transceiver configured as PRX. All data pipe addresses are searched for simultaneously. Only one data pipe can receive a packet at a time. All data pipes can perform Protocol engine functionality.

The following settings are common to all data pipes:

- CRC enabled/disabled (CRC always enabled when Protocol engine is enabled)
- CRC encoding scheme
- RX address width
- Frequency channel
- Air data rate
- LNA gain

The data pipes are enabled with the bits in the EN_RXADDR register. By default only data pipe 0 and 1 are enabled. Each data pipe address is configured in the RX_ADDR_PX registers.

Note: Always ensure that none of the data pipes have the same address.

Each pipe can have up to a 5 byte configurable address. Data pipes 0-5 share the four most significant address bytes. The LSByte must be unique for all six pipes. Figure 7.9 is an example of how data pipes 0-5 are addressed. Only pipe0 can have up to a 5 byte configurable address, other's pipes have 1bytes configurable address.

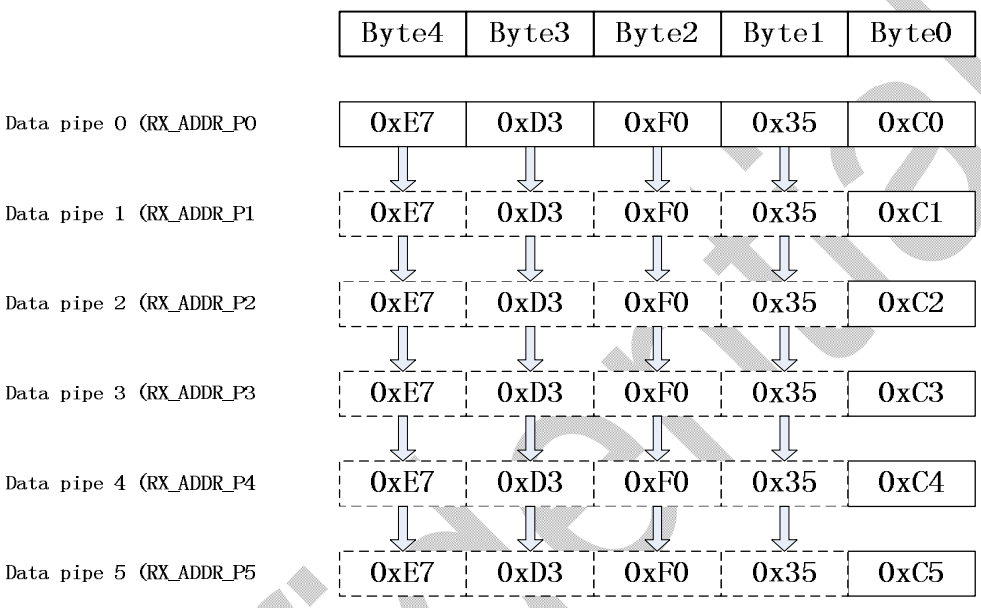


Figure 7.9 Addressing data pipes 0-5

The PRX, using MultiSlave and Protocol engine, receives packets from more than one PTX. To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. Figure 7.10 is an example of an address configuration for the PRX and PTX. On the PRX the RX_ADDR_Px, defined as the pipe address, must be unique. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 and as the pipe address for the designated pipe.

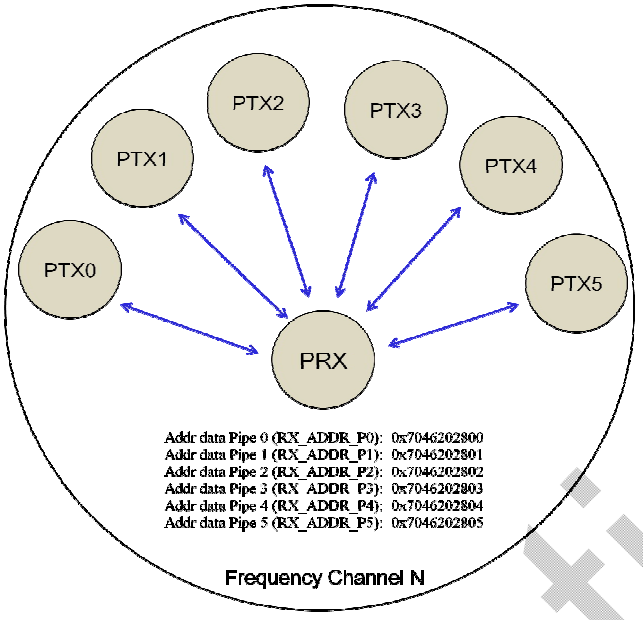
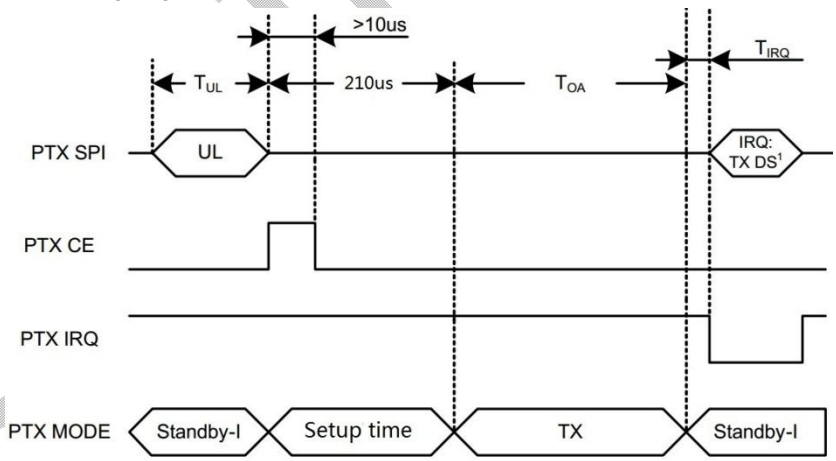


Figure 7.10Example of data pipe addressing in MultiSlave

Only when a data pipe receives a complete packet can other data pipes begin to receive data. When multiple PTXs are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

6.7 Protocol engine timing

This section describes the timing sequence of Protocol engine and how all modes are initiated and operated. The Protocol engine timing is controlled through the Data and Control interface. The RF transceiver can be set to static modes or autonomous modes where the internal state mAchine controls the events. Each autonomous mode/sequence ends with a RFIRQ interrupt. All the interrupts are indicated as IRQ events in the timing diagrams.



1 IRQ if No Ack is on.

T_{IRQ}=3us @ 1Mbps, @2Mbps

Figure 7.11Transmitting one packet with NO_ACK on

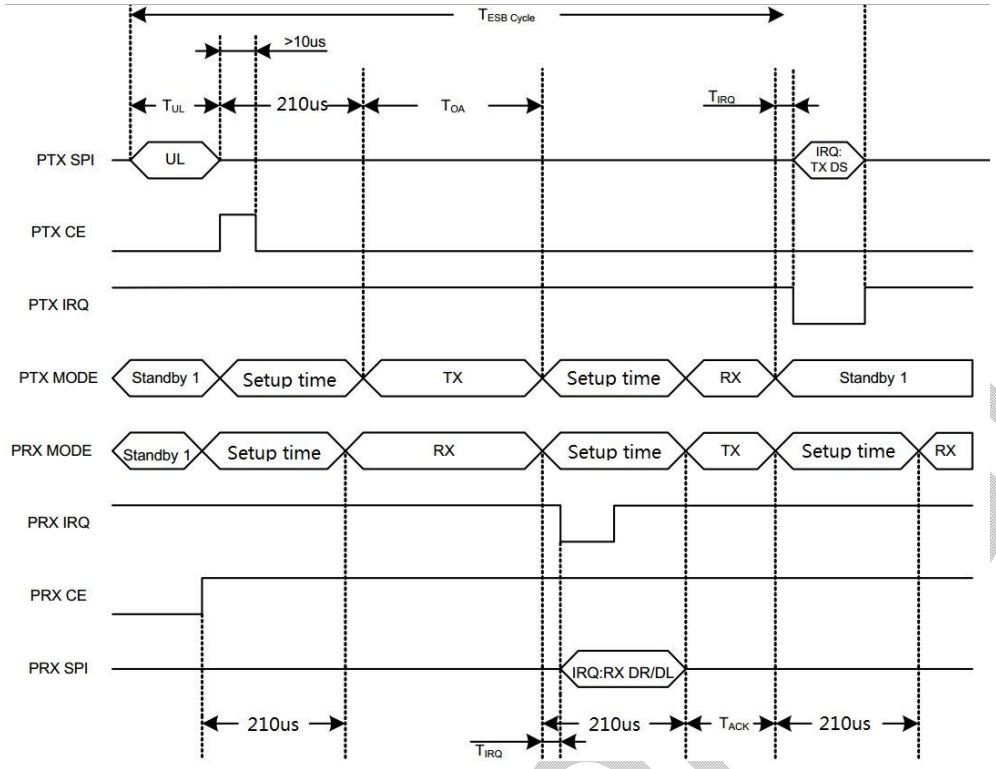


Figure 7.12 Timing of Protocol engine for one packet upload (2Mbps)

In Figure 7.12, the transmission and acknowledgement of a packet is shown. The PRX operation activates RX mode (CE=1), and the PTX operation is activated in TX mode (CE=1 for minimum 20μs). After 210μs the transmission starts and finishes after the elapse of T_{OA}.

When the transmission ends the PTX operation automAtically switches to RX mode to wait for the ACK packet from the PRX operation. When the PRX operation receives the packet it sets the interrupt for the host MCU and switches to TX mode to send an ACK. After the PTX operation receives the ACK packet it sets the interrupt to the MCU and clears the packet from the TX FIFO.

In Figure 7.13, the PTX timing of a packet transmission is shown when the first ACK packet is lost.

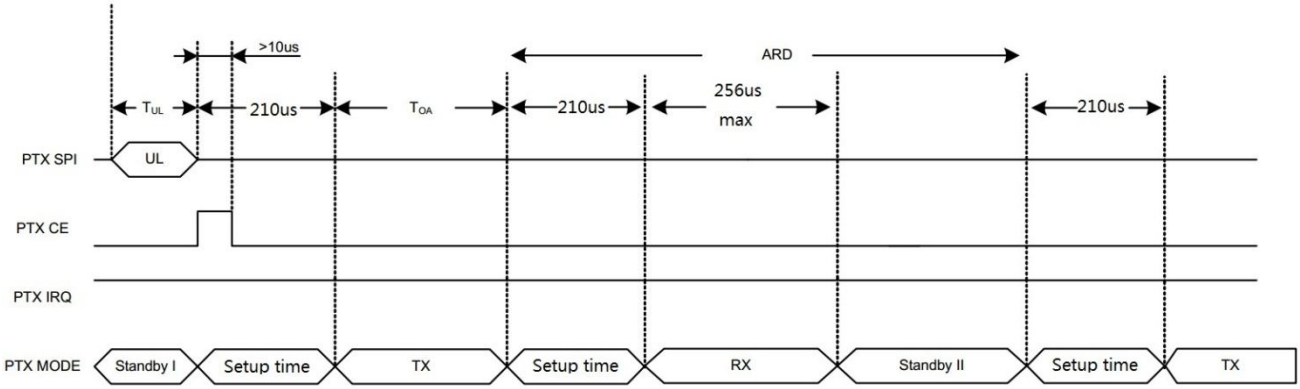


Figure 7.13Timing of Protocol engine when the first ACK packet is lost (2 Mbps)

6.8 Protocol engine transaction diagram

This section describes several scenarios for the Protocol engine automAtic transaction handling. The call outs in this section's figures

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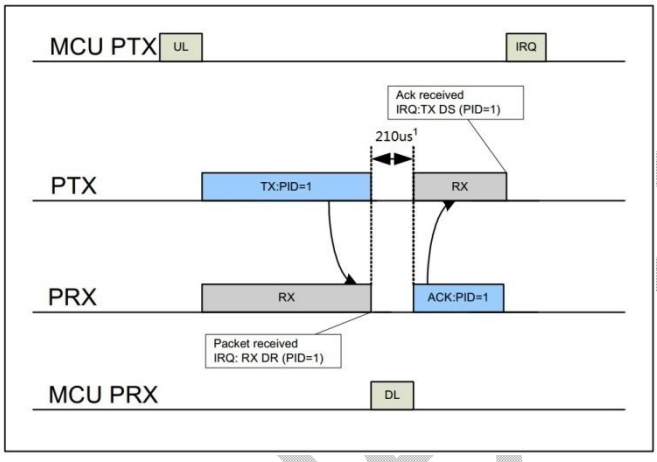
indicate the IRQs and other events. For MCU activity the event mAy be placed at a different timeframe.

Note: The figures in this section indicate the earliest possible download (DL) of the packet to the MCU and the latest possible upload (UL) of payload to the transmitter.

6.8.1 Single transaction with ACK packet and interrupts

In Figure 7.14, the basic auto acknowledgement is shown. After the packet is transmitted by the PTX and received by the PRX the ACK packet is transmitted from the PRX to the PTX. The RX_DR IRQ is asserted after the packet is received by the PRX, whereas the TX_DS IRQ is asserted when the packet is acknowledged and the ACK packet is received by the PTX.



1 Radio Turn Around delay

Figure 7.14 TX/RX cycles with ACK and the according interrupts

6.8.2 Single transaction with a lost packet

Figure 7.15 is a scenario where a retransmission is needed due to loss of the first packet transmits. After the packet is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits a specified time (including setup time, RX_TM and ARD) for the ACK packet, if it is not in the specific time slot the PTX retransmits the packet as shown in Figure 7.15. PTX will turn to RX mode after 210us setup time when packet is transmitted, after 130us RX timeout (RX_TM is RX timeout for PTX, it can be set shorter), then PTX turn to ARD (can be set to 0us, 256us, 512us to 3840us).

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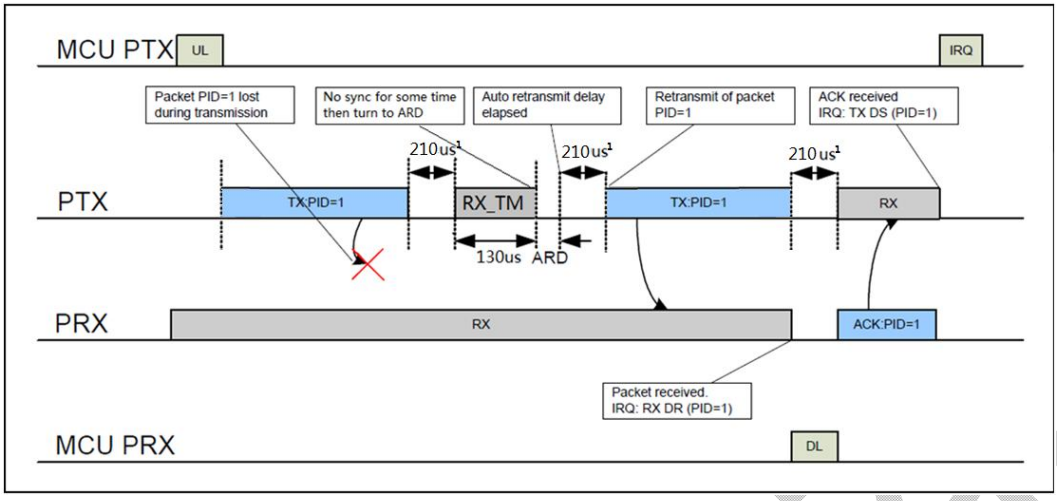


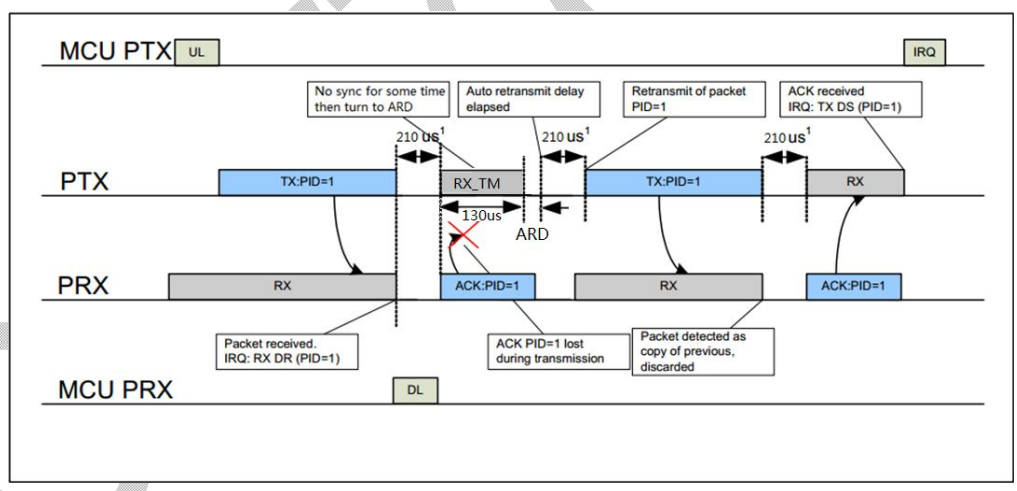
1 Radio Turn Around delay

Figure 7.15TX/RX cycles with ACK and the according interrupts when the first packet transmit fails

When an address is detected the PTX stays in RX mode until the packet is received. When the retransmitted packet is received by the PRX (see Figure 7.15). The RX_DR IRQ is asserted and an ACK is transmitted back to the PTX. When the ACK is received by the PTX, the TX_DS IRQ is asserted.

6.8.3 Single transaction with a lost ACK packet

Figure 7.16 is a scenario where a retransmission is needed after a loss of the ACK packet. The corresponding interrupts are also indicated.



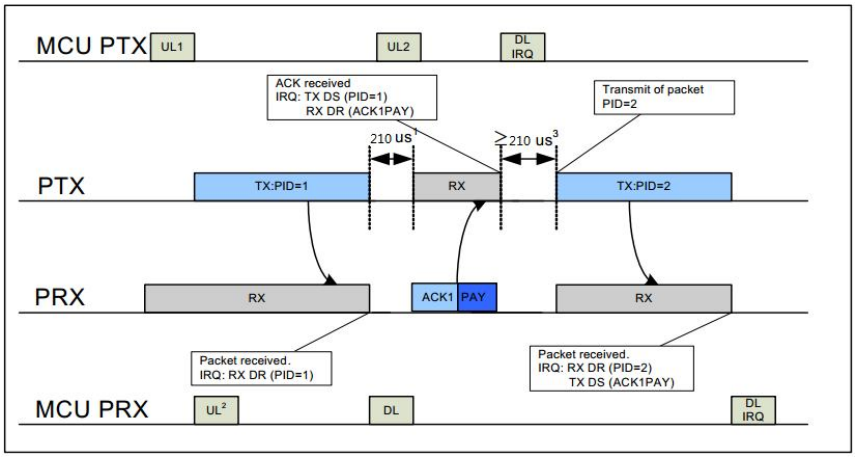
1 Radio Turn Around delay

Figure 7.16TX/RX cycles with ACK and the according interrupts when the ACK packet fails

6.8.4 Single transaction with ACK payload packet

Figure 7.17 is a scenario of the basic auto acknowledgement with payload. After the packet is transmitted by the PTX and received by the PRX the ACK packet with payload is transmitted from the PRX to the PTX. The RX_DR IRQ is asserted after the packet is received by the PRX, whereas on the PTX side the TX_DS IRQ is asserted when the ACK packet is received by the PTX. On the PRX

side, the TX_DS IRQ for the ACK packet payload is asserted after a new packet from PTX is received. The position of the IRQ in Figure 7.17 shows where the MCU can respond to the interrupt.



1 Radio Turn Around delay

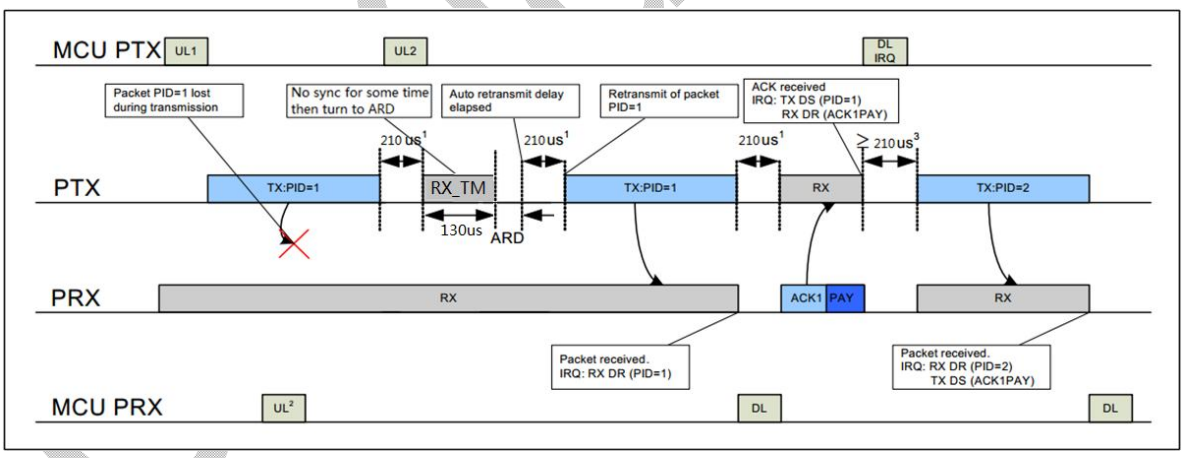
2 Uploading payload for Ack Packet

3 Delay defined by MCU on PTX side, >=210us

Figure 7.17 TX/RX cycles with ACK Payload and the according interrupts

6.8.5 Single transaction with ACK payload packet and lost packet

Figure 7.18 is a scenario where the first packet is lost and a retransmission is needed before the RX_DR IRQ on the PRX side is asserted. For the PTX both the TX_DS and RX_DR IRQ are asserted after the ACK packet is received. After the second packet (PID=2) is received on the PRX side both the RX_DR (PID=2) and TX_DS (ACK packet payload) IRQ are asserted.



1 Radio Turn Around delay

2 Uploading payload for Ack Packet

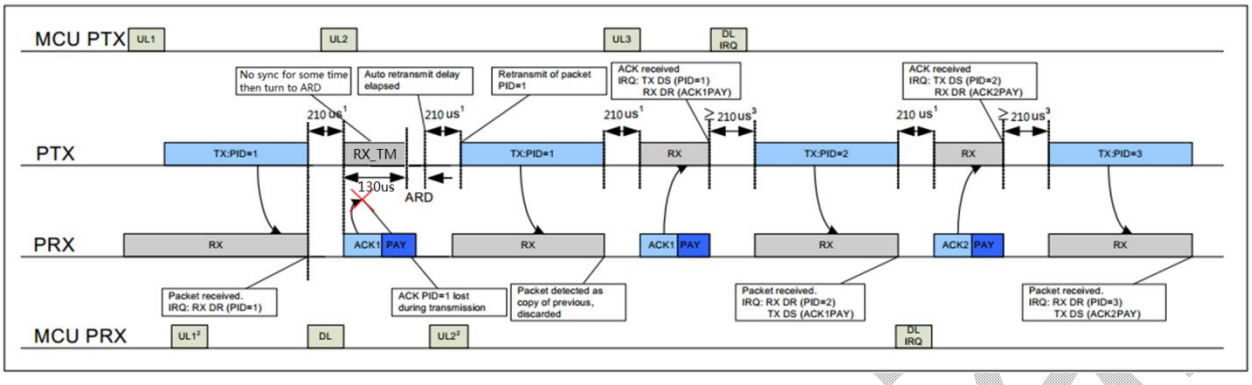
3 Delay defined by MCU on PTX side, >=210us

Figure 7.18 TX/RX cycles and the according interrupts when the packet transmission fails

6.8.6 Two transactions with ACK payload packet and the first ACK packet lost

Figure 7.19 the ACK packet is lost and a retransmission is needed before the TX_DS IRQ is asserted, but the RX_DR IRQ is asserted

immediately. The retransmission of the packet (PID=1) results in a discarded packet. For the PTX both the TX_DS and RX_DR IRQ are asserted after the second transmission of ACK, which is received. After the second packet (PID=2) is received on the PRX both the RX_DR (PID=2) and TX_DS (ACK1PAY) IRQ is asserted. The callouts explains the different events and interrupts.



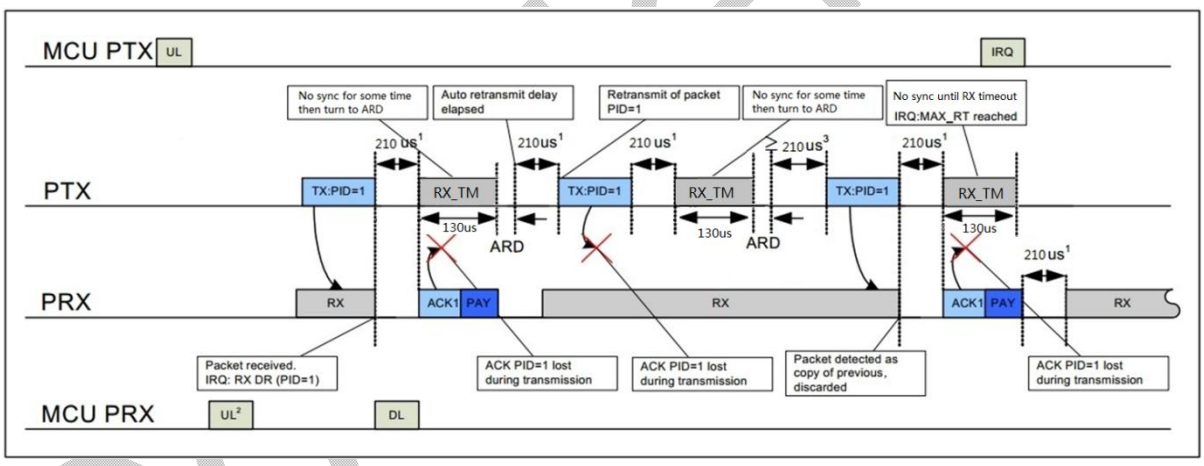
1 Radio Turn Around delay

2 Uploading payload for Ack Packet

3 Delay defined by MCU on PTX side, >=210us

Figure 7.19TX/RX cycles with ACK Payload and the according interrupts when the ACK packet fails

6.8.7 Two transactions where Max retransmissions is reached



1 Radio Turn Around delay

2 Uploading payload for Ack Packet

3 Delay defined by MCU on PTX side, >=210us

Figure 7.20 TX/RX cycles with ACK Payload and the according interrupts when the transmission fails. ARC is set to 2.

mAX_RT IRQ is asserted if the auto-retransmit counter (ARC_CNT) exceeds the programmed Maximum limit (ARC). In Figure 7.20, the packet transmission ends with a mAX_RT IRQ. The payload in TX FIFO is NOT removed and the MCU decides the next step in the protocol. A toggle of the CE bit in the RFCON register starts a new transmitting sequence of the same packet. The payload can be removed from the TX FIFO using the FLUSH_TX commAnd.

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7 Data and control interface

The data and control interface gives you access to all the features in the RF transceiver. The data and control interface consists of the following six 5Volt tolerant digital signals:

- IRQ (this signal is active low and controlled by three mAsk-able interrupt sources)
- CE (this signal is active high and used to activate the chip in RX or TX mode)
- CSN (SPI signal)
- SCK (SPI signal)
- MOSI (SPI signal)
- MISO (SPI signal)

Using 1 byte SPI commAnds, you can activate the SE8R01 data FIFOs or the register mAp during all modes of operation.

7.1 Features

- Special SPI commAnds for quick access to the most frequently used features
- 0-10Mbps 4-wire SPI
- 8 bit commAnd set
- Easily configurable register mAp
- Full three level FIFO for both TX and RX direction

7.2 Functional description

The SPI is a standard SPI with a Maximum data rate of 10Mbps.

7.3 SPI operation

This section describes the SPI commAnds and timing.

7.3.1 SPI commAnds

The SPI commAnds are shown in Table 8.1. Every new commAnd must be started by a high to low transition on CSN.

The STATUS register is serially shifted out on the MISO pin simultaneously to the SPI commAnd word shifting to the MOSI pin.

The serial shifting SPI commAnds is in the following formAt:

<**CommAnd word:** MSBit to LSBit (one byte)>

<**Data bytes:** LSByte to MSByte, MSBit in each byte first>

See Figure 8.1 and Figure 8.2 for timing informAtion.

CommAnd	CommAnd word (binary)	#Data bytes	Operation

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R_RESISTER	000A AAAA	1 to 5 LSByte first	Read commAnd and status registers. AAAAA=5 bit register mAp address
W_RESISTER	001A AAAA	1 to 5 LSByte first	Write commAnd and status registers. AAAAA=5 bit register mAp address Executable in power down or standby modes only.
R_TX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1-32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed
REUSE_TX_PL	1110 0011	0	Used for a PTX operation Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission.
R_RX_PL_WID	0110 0000	1	Read RX payload width for the top R_RX_PAYLOAD in the RX FIFO. Note: Flush RX FIFO if the read value is larger than 32 bytes.
W_ACK_PAYLOAD	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in – first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_ NO_ACK	1011 0000	1 to 32 LSByte first	Used in TX mode. Disables AUTOACK on this specific packet specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

Table 8.1CommAnd set for the RF transceiver SPI

The W_REGISTER and R_REGISTER commAnds operate on single or multi-byte registers. When accessing multi-byte registers read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register. The content of the status register is always read to MISO after a high to low transition on CSN.

Note: The 3 bit pipe informAtion in the STATUS register is updated during the IRQ high to low transition. The pipe informAtion is unreliable if the STATUS register is read during an IRQ high to low transition.

7.3.2 SPI timing

SPI operation and timing is shown in Figure 8.1 to Figure 8.3 and in Table 8.3 to Table 8.8. SE8R01must be in a standby or power down mode before writing to the configuration registers.

In Figure 8.1 to Figure 8.3 the following abbreviations are used:

Abbreviation	Description
Cn	SPI commAnd bit
Sn	STATUS register bit
Dn	Data Bit (**Note:** LSByte to MSByte, MSBit in each byte first)

Table 8.2 Abbreviations used in Figure 8.1. to Figure 8.2.

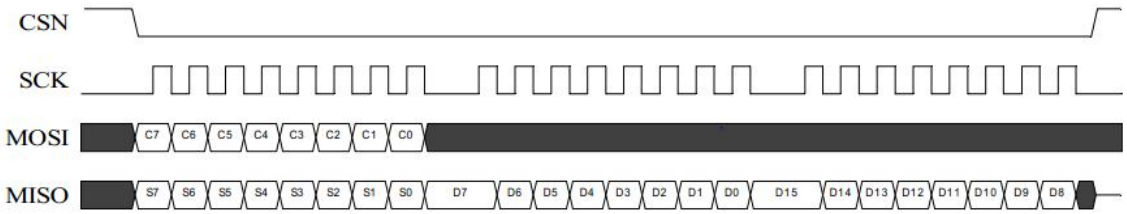


Figure 8.1 SPI read operation

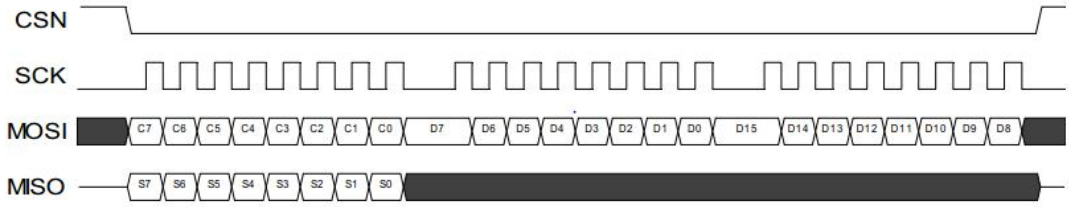


Figure 8.2SPI write operation

7.4 Data FIFO

The data FIFOs store transmitted payloads (TX FIFO) or received payloads that are ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and PRX mode. The following FIFOs are present in the RF transceiver:

- TX three level, 32 byte FIFO
- RX three level, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commAnds. A TX FIFO in PRX can store payloads for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in – first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO using the FLUSH_TX commAnd.

The RX FIFO in PRX can contain payloads from up to three different PTX devices and a TX FIFO in PTX can have up to three payloads stored.

You can write to the TX FIFO using these three commAnds; W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commAnds provide access to the TX_PLD register.

The RX FIFO can be read by the commAnd R_RX_PAYLOAD in PTX and PRX mode. This commAnd provides access to the RX_PLD register.

The payload in TX FIFO in a PTX is not removed if the mAX_RT IRQ is asserted.

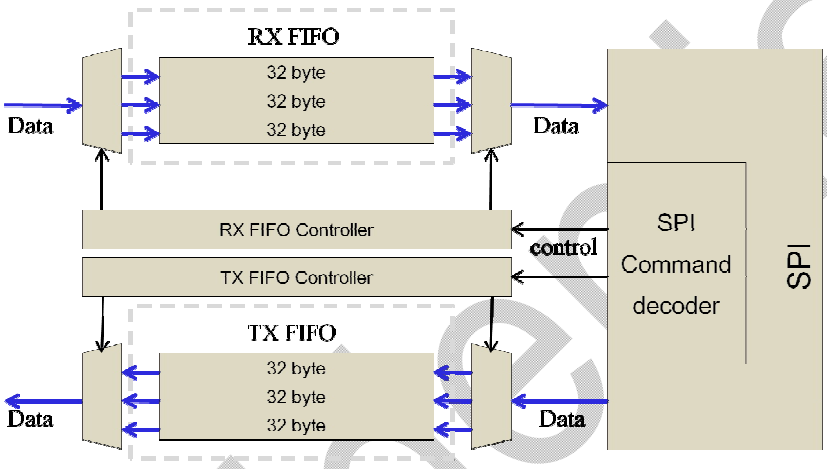


Figure 8.5 FIFO (RX and TX) block diagram

You can read if the TX and RX FIFO are full or empty in the FIFO_STATUS register.

7.5 Interrupt

The SE8R01 has an active low interrupt (IRQ) pin. The IRQ pin is activated when TX_DS IRQ, RX_DR IRQ or mAX_RT IRQ are set high by the state mAchine in the STATUS register. The IRQ pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mAsk in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the mASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

Note: The 3 bit pipe informAtion in the STATUS register is updated during the IRQ high to low transition. The pipe informAtion is unreliable if the STATUS register is read during an IRQ high to low transition.

8 Register mAp

You can configure and control the radio by accessing the register mAp through the SPI.

8.1 Register mAp table

All undefined bits in the table below are redundant. They are read out as ‘0’.

Note:Addresses 18 to 1B are reserved for test purpose, alteringthem mAkes the chip mAlfunction.

8.1.1 CONFIG (RW)Address: 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	mASK_RX_DR	mASK_TX_DS	mASK_mAX_RT	EN_CRC	CRCO	PWR_UP	PRIM_RX
0	0	0	0	1	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
6	0	mASK_RX_DR	mAsk interrupt caused by RX_DR	
			0	Reflect RX_DR as active low interrupt on the IRQ pin
			1	Interruptnot reflected on the IRQ pin
5	0	mASK_TX_DS	mAsk interrupt caused by TX_DS	
			0	Reflect TX_DS as active low interrupt on the IRQ pin
			1	Interrupt not reflected on the IRQpin
4	0	mASK_mAX_RT	mAsk interrupt caused by mAX_RT	
			0	Reflect mAX_RT as active low interrupt on the IRQ pin
			1	Interrupt not reflected on the IRQ pin
3	1	EN_CRC	Enable CRC. Forced high if one of the bits in the EN_AA is high	
			0	Disable CRC
			1	Enable CRC
2	0	CRCO	CRC encoding scheme	
			0	1 byte
			1	2 byte
1	0	PWR_UP	Power up control	
			0	POWER DOWN
			1	POWER UP
0	0	PRIM_RX	RX/TX control	
			0	PTX
			1	PRX

8.1.2 EN_AA (RW) Address: 01h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed		ENAA_P5	ENAA_P4	ENAA_P3	ENAA_P2	ENAA_P1	ENAA_P0
0		1	1	1	1	1	1
RW		RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only 0 allowed	
			0	Keep the current value

			1	Reset to default values
6	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5	1	ENAA_P5	Enable auto acknowledgement data pipe 5	
			0	Disable
			1	Enable
4	1	ENAA_P4	Enable auto acknowledgement data pipe 4	
			0	Disable
			1	Enable
3	1	ENAA_P3	Enable auto acknowledgement data pipe 3	
			0	Disable
			1	Enable
2	1	ENAA_P2	Enable auto acknowledgement data pipe 2	
			0	Disable
			1	Enable
1	1	ENAA_P1	Enable auto acknowledgement data pipe 1	
			0	Disable
			1	Enable
0	1	ENAA_P0	Enable auto acknowledgement data pipe 0	
			0	Disable
			1	Enable

8.1.3 EN_RXADDR (RW) Address: 02h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed		ERX_P5	ERX_P4	ERX_P3	ERX_P2	ERX_P1	ERX_P0
0		0	0	0	0	1	1
RW		RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7:6	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5	0	ERX_P5	Enable data pipe 5	
			0	Disable
			1	Enable
4	0	ERX_P4	Enable data pipe 4	
			0	Disable

			1	Enable
3	0	ERX_P3	Enable data pipe 3	
			0	Disable
			1	Enable
2	0	ERX_P2	Enable data pipe 2	
			0	Disable
			1	Enable
1	1	ERX_P1	Enable data pipe 1	
			0	Disable
			1	Enable
0	1	ERX_P0	Enable data pipe 0	
			0	Disable
			1	Enable

8.1.4 SETUP_AW (RW) Address: 03h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						SETUP_AW	
0						2'b11	
RW						RW	

Description of Word

Bit	Value	Symbol	Description	
7:2	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
1:0	2'b11	SETUP_AW	Setup of Address Widths (common for all data pipes)	
			2'b11	5 bytes
			2'b10	4 bytes
			2'b01	Illegal
			2'b00	Illegal

8.1.5 SETUP_RETR (RW) Address: 04h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ARD				ARC			
4'b0				4'b11			
RW				RW			

Description of Word

Bit	Value	Symbol	Description	
7:2	4'b0	ARD	Auto Retransmit Delay	
			4'hf	Wait 3840μS
			…	…
			4'h1	Wait 256μS
			4'h0	Wait 0μS
3:0	4'b11	ARC	Auto Retransmit Count	
			4'hf	Up to 15 Re-Transmit on fail of AA
			…	…
			4'h1	Up to 1 Re-Transmit on fail of AA
			4'h0	Re-Transmit disabled

8.1.6 RF_CH (RW) Address: 05h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg_Rf_ch							
8'b2							
RW							

Description of Word

Bit	Value	Symbol	Description
8:0	2	Reg_Rf_ch	Sets the frequency channel SE8R01 operates on

8.1.7 RF_SETUP (RW) Address: 06h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONT_WAVE	PA_PWR[3]	RF_DR_LOW	Reserved	RF_DR_HIGH	PA_PWR		
0	1	0	0	1	3'b010		
RW	RW	RW	RW	RW	RW		

Description of Word

Bit	Value	Symbol	Description	
7	0	CONT_WAVE	Enables continuous carrier transmit when high	
			0	Disable
			1	Enable

6	1	PA_PWR[3]	PA power select bit 3	
5	0	RF_DR_LOW	See RF_DR_HIGH for encoding.	
4	0	reserved	Reserved	
3	1	RF_DR_HIGH	Select between the high speed data rates. This bit is donot care if RF_DR_LOW is set.Encoding: [RF_DR_LOW, RF_DR_HIGH]:	
			11	500Kbps
			10	reserved
			01	2Mbps
			00	1Mbps
2:0	3'b010	PA_PWR[2:0]	PA power control, PA_PWR[3:0] with pa_voltage of RF_IVGEN in bank1	
			PA_PWR[3:0] / Pa_voltage(bank1 of RF_IVGEN)	
			1111 / 0	Output 6 dbm, 40mA
			1000 / 0	Output 5 dbm
			0111 / 1	Output 4 dbm, 25mA
			0011 / 0	Output 0 dbm, 18.5mA
			0001 / 0	Output -6 dbm
			0001 / 1	Output -12 dbm
			0000 / 0	Output -16 dbm
			0000 / 1	Output -43 dbm

8.1.8 STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	RX_DR	TX_DS	mAX_RT	RX_P_NO			TX_FULL
0	0	0	0	3'b111			0
R	RW	RW	RW	R			R

Description of Word

Bit	Value	Symbol	Description	
7	0	BANK	Register BANK status	
			1	Register R/W is to register BANK1
			0	Register R/W is to register BANK0
6	0	RX_DR	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO Write 1 to clear bit.	
5	0	TX_DS	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK isactivated, this bit is set high only when ACK is received. Write 1 to clear bit.	

4	0	mAX_RT	Maximum number of TX retransmits interrupt, Write 1 to clear bit. If mAX_RT is asserted it must be cleared to enable further communication.	
3:1	3'b111	RX_P_NO	Data pipe number for the payload available for reading from RX_FIFO	
			111	RX FIFO Empty
			110	Not Used
			000-101	Data Pipe Number
0	0	TX_FULL	TX FIFO full flag	
			0	Available locations in TX FIFO
			1	TX FIFO full

8.1.9 OBSERVE_TX (RW) Address: 08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLOS_CNT				ARC_CNT			
4'h0				4'h0			
R				R			

Description of Word

Bit	Value	Symbol	Description
7:4	4'h0	PLOS_CNT	Count lost packets. The counter is overflow protected to 15, and discontinues at Max until reset. The counter is reset by writing to RF_CH.
3:0	4'h0	ARC_CNT	Count retransmitted packets. The counter is reset when transmission of a new packet starts.

8.1.10 RPD ® Address: 09h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
sig_dbm_est							
8'h0							
R							

Description of Word

Bit	Value	Symbol	Description	
7:0	0	sig_dbm_est	estimAted in-band signal level in dBm, should support -100 ~ +10 dBm,	
			11000000	-64 dBm

8.1.11 RX_ADDR_P0 (RW) Address: 0Ah

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
RX_ADDR_P0							

8’h70							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
RX_ADDR_P0							
8’h41							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
RX_ADDR_P0							
8’h88							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RX_ADDR_P0							
8’h20							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P0							
8’h46							
RW							

Description of Word

Bit	Value	Symbol	Description
39:0	40’7041882046	RX_ADDR_P0	Receive address data pipe 0. 5 Bytes Maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)

8.1.12 RX_ADDR_P1 (RW) Address: 0Bh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P1							
8’Hc2							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8’hc2	RX_ADDR_P1	Receive address data pipe 2. Only LSB. MSBytes are equAl to RX_ADDR_P0[39:8]

8.1.13 RX_ADDR_P2 (RW) Address: 0Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P2							

8’Hc3
RW

Description of Word

Bit	Value	Symbol	Description
7:0	8’hc3	RX_ADDR_P2	Receive address data pipe 2. Only LSB. MSBytes are equAl to RX_ADDR_P0[39:8]

8.1.14 RX_ADDR_P3 (RW) Address: 0Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P3							
8’Hc4							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8’hc4	RX_ADDR_P3	Receive address data pipe 3. Only LSB. MSBytes are equAl to RX_ADDR_P0[39:8]

8.1.15 RX_ADDR_P4 (RW) Address: 0Eh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P4							
8’Hc5							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8’hc5	RX_ADDR_P4	Receive address data pipe 4. Only LSB. MSBytes are equAl to RX_ADDR_P0[39:8]

8.1.16 RX_ADDR_P5 (RW) Address: 0Fh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P5							
8’Hc6							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc6	RX_ADDR_P5	Receive address data pipe 5. Only LSB. MSBytes are equAl to RX_ADDR_P0[39:8]

8.1.17 TX_ADDR(RW) Address: 10h

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
TX_ADDR							
8'h70							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
TX_ADDR							
8'h41							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
TX_ADDR							
8'h88							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TX_ADDR							
8'h20							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_ADDR							
8'h46							
RW							

Description of Word

Bit	Value	Symbol	Description
39:0	40'h704 1882046	TX_ADDR	Transmit address. Used for a PTX device only. (LSByte is written first)Set RX_ADDR_P0 equAl to this address to handle automAtic acknowledge if this is a PTX device with Protocol engine enabled.

8.1.18 RX_PW_P0 (RW) Address: 11h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P0					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P0	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

8.1.19 RX_PW_P1 (RW) Address: 12h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P1					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P1	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

8.1.20 RX_PW_P2 (RW) Address: 13h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P2					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value

			1	Reset to default values
5:0	0	RX_PW_P2	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

8.1.21 RX_PW_P3 (RW) Address: 14h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P3					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P3	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

8.1.22 RX_PW_P4 (RW) Address: 15h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P4					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P4	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes)	
			32	32 bytes

			…	…
			1	1 byte
			0	Pipe not used

8.1.23 RX_PW_P5 (RW) Address: 16h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P4					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P5	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

8.1.24 FIFO_STATUS (RW) Address: 17h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TX_REUSE_PL	TX_FULL	TX_EMPTY	Reserved		RX_FULL	RX_EMPTY
0	0	0	1	0		0	1
R	R	R	R	R		R	R

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only '0' allowed	
			0	Keep the current value
			1	Reset to default values
6	0	TX_REUSE_PL	TX REUSE flag.	
			1	Tx data reused
			0	Tx data not reused
5	0	TX_FULL	TX FIFO full flag.	

			1	TX FIFO full
			0	Available locations in TX FIFO
4	1	TX_EMPTY	TX FIFO empty flag.	
			1	TX FIFO empty
			0	Data in TX FIFO
3:2	2'b00	Reserved	Only '00' allowed	
			0	Keep the current value
			1	Reset to default values
1	0	RX_FULL	RX FIFO full flag.	
			1	RX FIFO full
			0	Available locations in RX FIFO
0	1	RX_EMPTY	RX FIFO empty flag.	
			1	RX FIFO empty
			0	Data in RX FIFO

8.1.25 DYNPD (RW) Address: 1Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		DPL_P5	DPL_P4	DPL_P3	DPL_P2	DPL_P1	DPL_P0
0		0	0	0	0	0	0
RW		RW	RW	RW	RW	RW	RW

Description of Word

Bit	**Value**	**Symbol**	**Description**	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5	0	DPL_P5	Enable dynamic payload length data pipe 5. (Requires EN_DPL)	
4	0	DPL_P4	Enable dynamic payload length data pipe 4. (Requires EN_DPL)	
3	0	DPL_P3	Enable dynamic payload length data pipe 3. (Requires EN_DPL)	
2	0	DPL_P2	Enable dynamic payload length data pipe 2. (Requires EN_DPL)	
1	0	DPL_P1	Enable dynamic payload length data pipe 1. (Requires EN_DPL)	
0	0	DPL_P0	Enable dynamic payload length data pipe 0. (Requires EN_DPL)	

8.1.26 FEATURE (RW) Address: 1Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					EN_DPL	EN_ACK_PAY	EN_DYN_ACK
0					0	0	0

RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7:3	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
2	0	EN_DPL	Enables Dynamic Payload Length	
1	0	EN_ACK_PAY	Enables Payload with ACK	
0	0	EN_DYN_ACK	Enables the W_TX_PAYLOAD_NOACK commAnd	

8.1.27 SETUP_VALUE (RW) Address: 1Eh

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit32
REG_LNA_WAIT							
8'h00							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit24
REG_MBG_WAIT							
8'h10							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
RX_TM_CNT							
8'h80							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TX_SETUP_VALUE							
8'h32							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_SETUP_VALUE							
8'h28							
RW							

Description of Word

Bit	Value	Symbol	Description
39:32	8'h00	REG_LNA_WA	Lna wait counter

		IT	8'hff	255 cycle
			…	…
			1	1 cycle
			0	0 cycle
31:24	8'h10	REG_MBG_WAIT	mAin bandgap wait counter	
			8'hff	255us
			…	…
			1	1 us
			0	0 us
23:16	8'h80	RX_TM_CNT	Rx timeout counter.	
			8'hff	255us
			…	…
			1	1 us
			0	0 us
15:8	8'h32	TX_SETUP_VALUE	TX_SETUP time, the time between Standby to TX mode	
			8'hff	255us
			…	…
			1	1 us
			0	0 us
7:0	8'h28	RX_SETUP_VALUE	RX_SETUP time, the time between Standby to RX mode	
			8'hff	255us
			…	…
			1	1 us
			0	0 us

8.1.28 PRE_GURD (RW) Address: 1Fh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CE_REG	SPARE_REG[6:0]						
0	0						

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAIL_CTL			GRD_EN	GRD_CNT			
1			1	4'h2			
RW			RW	RW			

Description of Word

Bit	Value	Symbol	Description
15	0	CE_REG	CE=CE_PAD&(~CE_REG)，when CE pad connected to power， CE_REG can be used

			to control CE	
14:8	0	SPARE_REG	Reserved register	
7:5	1	TAIL_CTL	Number of repeat bit after the CRC	
			7	7 repeat tail
			…	…
			1	1 repeat tail
			0	0 No repeat tail
4	1	GRD_EN	Pre-GuArd enable	
3:0	4'h2	GRD_CNT	Number of Pre-GuArd bit before preamble	
			4'hf	16 bit pre_guArd
			…	…
			1	2 bit pre_guArd
			0	1 bit pre_guArd

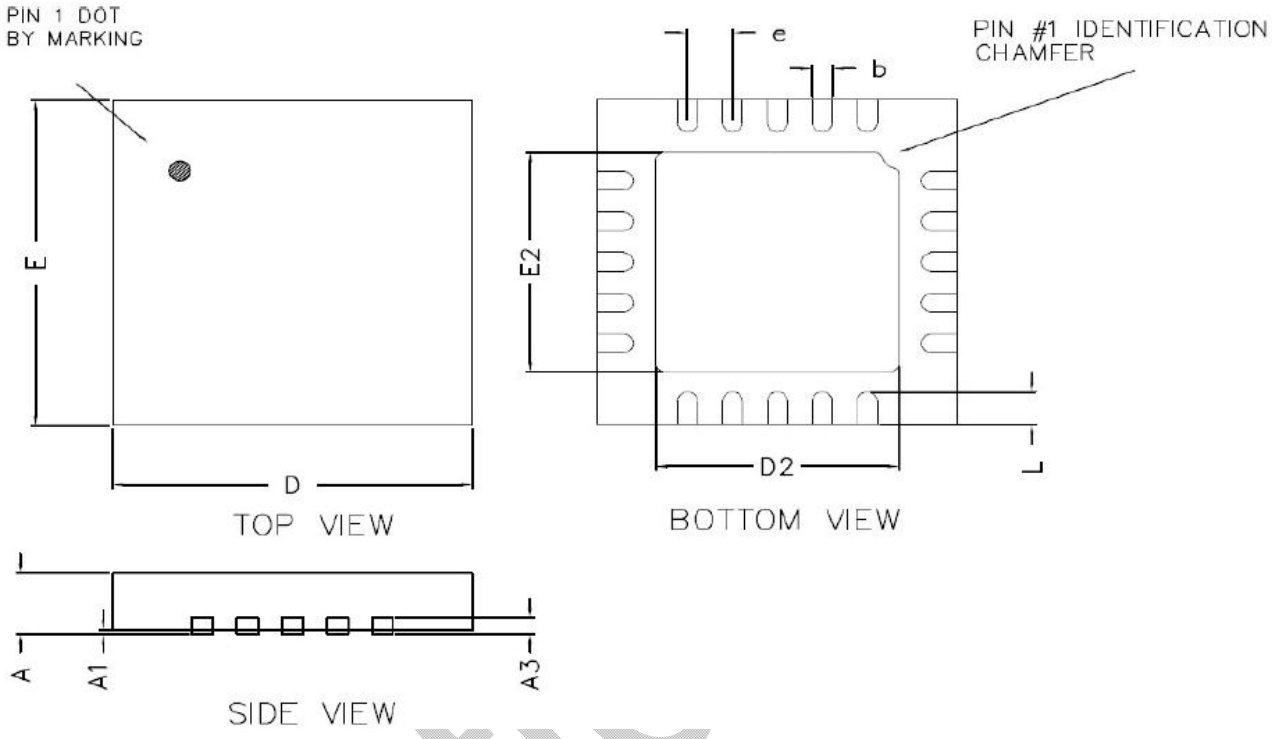
9 Glossary of Terms

Term	Description
ACK	Acknowledgement
ACS	Adjacent Channel Selectivity
AGC	AutomAtic Gain Control

ART	Auto Re-Transmit
CD	Carrier Detect
CE	Chip Enable
CLK	Clock
CRC	Cyclic Redundancy Check
CSN	Chip Select NOT
PE	Protocol engine
GFSK	Gaussian Frequency Shift Keying
IM	Intermodulation
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LSByte	Least Significant Byte
Mbps	Megabit per second
MCU	Microcontroller Unit
MISO	mAster In Slave Out
MOSI	mAster Out Slave In
MSB	Most Significant Bit
MSByte	Most Significant Byte
PCB	Printed Circuit Board
PID	Packet Identity Bits
PLD	Payload
PRX	PrimAry RX
PTX	PrimAry TX
PWR_DWN	Power Down
PWR_UP	Power Up
RoHS	Restriction of use of Certain Hazardous Substances
RPD	Received Power Detector
RX	Receive
RX_DR	Receive Data Ready
SPI	Serial Peripheral Interface
TX	Transmit
TX_DS	Transmit Data Sent

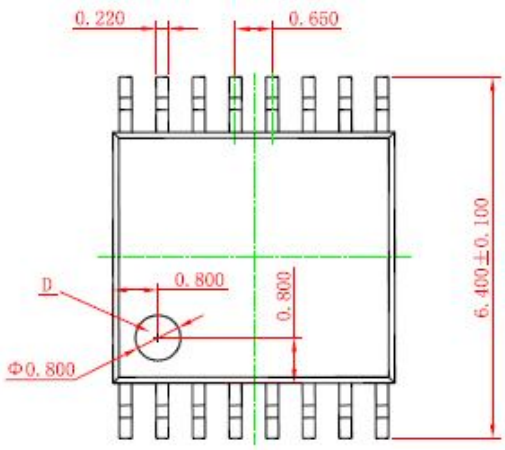
10 Package InformAtion

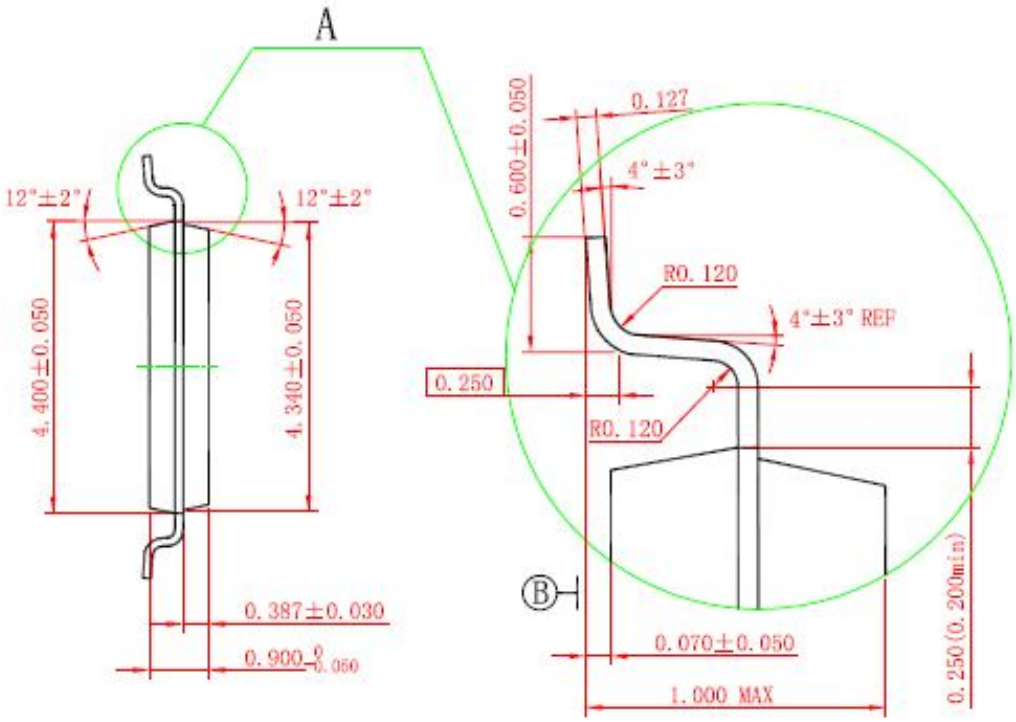
10.1.1 Uses the QFN20 4x4 package, with mAtt tin plating.



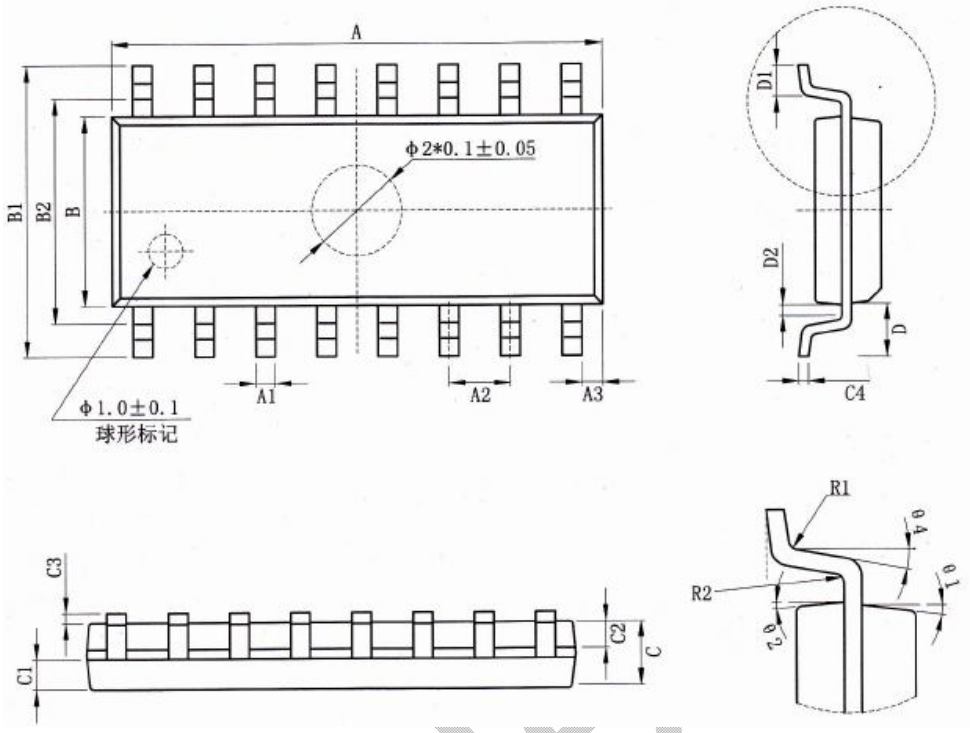
Parameter	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	-	0.05	mm
A3		0.20 REF		mm
D	3.95	4.00	4.05	mm
E	3.95	4.00	4.05	mm
B	0.18	0.23	0.30	mm
L	0.30	0.40	0.50	mm
D2	2.55	2.70	2.80	mm
E2	2.55	2.70	2.80	mm
E		0.50 REF		mm

10.1.2 Uses the Tssop16 package, with mAtt tin plating.





10.1.3 Uses the Sop16 package, with mAtt tin plating.



标注 \ 尺寸	最小(mm)	最大(mm)	标注 \ 尺寸	最小(mm)	最大(mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.35	1.55	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.10	0.25			

Contact Information

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