TLV742P 200-mA, Small Size, Low-Dropout Linear Voltage Regulator

1 Features

- Input Voltage Range From 2 V to 5.5 V
- Fixed-Output Voltage Combinations Possible From 0.85 V to 5 V in 50-mV Steps[(1)]
- 0.5% Typical Accuracy
- High PSRR:
  - 55 dB at 1 MHz
- I_Q When Enabled: 25 µA
- I_Q When Disabled: 1 µA
- Active Output Discharge
- Thermal Shutdown and Overcurrent Protection
- Package:
  - 1-mm × 1-mm DQN (X2SON)

2 Applications

- Point of Sale
- Camera and Machine Vision Modules
- Gaming and Toys
- Building Automation and Video Surveillance
- TVs and Set-Top Boxes

3 Description

The TLV742P series of low-dropout linear voltage regulators (LDOs) are optimized to providing excellent performance by supporting a wide output voltage range. The LDOs can directly regulate a single cell Li-ion battery input-to-output voltage as low as 0.85 V. If used to post-regulate a DC-DC converter output, the high PSRR of 55 dB at 1 MHz suppresses ripple to provide a stable low-noise, well-regulated V_{OUT}.

The TLV742P has an active output discharge feature that helps ensure the output is kept low while the system is disabled, in standby mode, or in sleep mode. Additionally, overcurrent protection is present to protect the device in the event of an output short along with thermal shutdown to prevent overheating.

The TLV742P series of voltage regulators are available in a 1 mm × 1 mm X2SON package to minimize PCB area.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV742P	X2SON (4)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

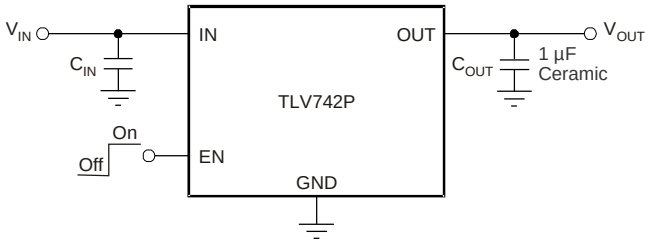


Table of Contents

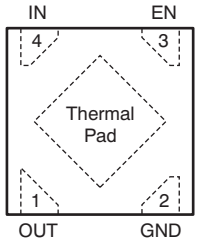
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2017	*	Initial release.

5 Pin Configuration and Functions

DQN Package
4-Pin X2SON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. For TLV742P, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
GND	2	—	Ground pin
IN	4	I	Input pin. For good transient performance, place a small 1-μF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Requirements* for more details.
OUT	1	O	Regulated output voltage pin. A small 1-μF ceramic capacitor is required from this pin to ground to ensure stability. See *Input and Output Capacitor Requirements* for more details.
Thermal pad	—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6	V
	EN	–0.3	6	V
	OUT	–0.3	6	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Operating junction, T_J		–55	150	°C
Storage, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to GND pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)(1)	±2000	V
		Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV742P DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	152	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	117.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	117	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	99.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

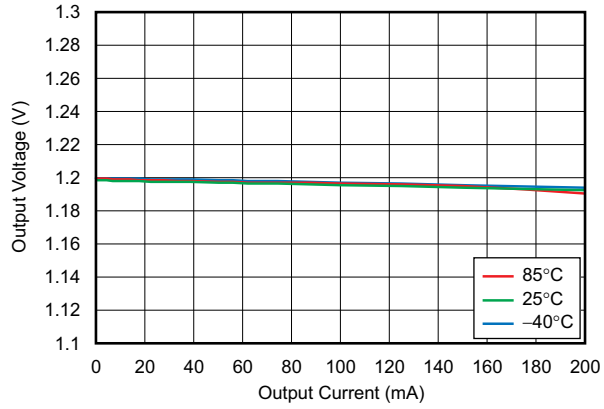
at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 0.47 µF, and T_J = –40°C to +85°C. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2		5.5	V
V_{OUT}	Output voltage range				0.85		5	V
	DC output accuracy					0.5%		
		V_{OUT} ≥ 0.85 V			–1.5%		1.5%	
$\Delta V_{O(\Delta VI)}$	Line regulation					1	5	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA				10	20	mV
$V_{(DO)}$	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$	2 V < V_{OUT} ≤ 2.4 V	I_{OUT} = 30 mA		65		mV
				I_{OUT} = 150 mA		325	360	mV
			2.4 V < V_{OUT} ≤ 2.8 V	I_{OUT} = 30 mA		50		mV
				I_{OUT} = 150 mA		250	300	mV
			2.8 V < V_{OUT} ≤ 3.3 V	I_{OUT} = 30 mA		45		mV
				I_{OUT} = 150 mA		220	270	mV
			3.3 V < V_{OUT} ≤ 5 V	I_{OUT} = 30 mA		40		mV
				I_{OUT} = 150 mA		200	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$			240	300	450	mA
$I_{(GND)}$	Ground pin current	I_{OUT} = 0 mA				25	50	µA
$I_{(EN)}$	EN pin current	V_{EN} = 5.5 V				0.01		µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V 2 V ≤ V_{IN} ≤ 4.5 V				1		µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)				0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)				0.9		V_{IN}	V
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V V_{OUT} = 2.8 V I_{OUT} = 30 mA		f = 100 Hz		70		dB
				f = 10 kHz		55		
				f = 1 MHz		55		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V V_{OUT} = 1.8 V I_{OUT} = 10 mA				45		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1 µF I_{OUT} = 150 mA				100		µs
$R_{PULLDOWN}$	Pulldown resistance (TLV742P only)					120		Ω
T_J	Operating junction temperature				–40		125	°C

(1) Start-up time = time from EN assertion to 0.98 × V_{OUT}.

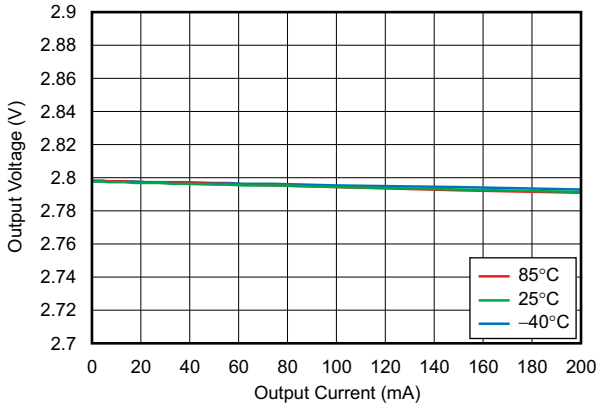
6.6 Typical Characteristics

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



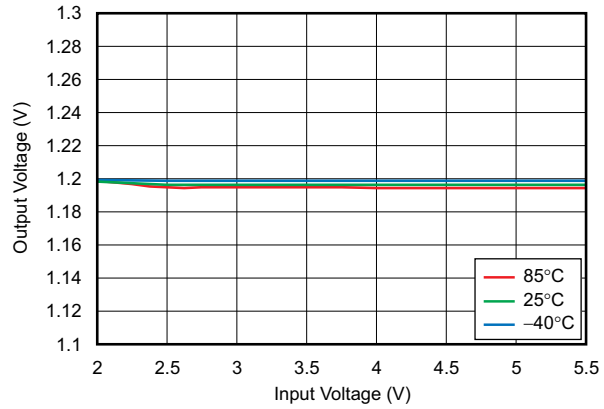
V_{OUT} = 1.2 V

Figure 1. Load Regulation



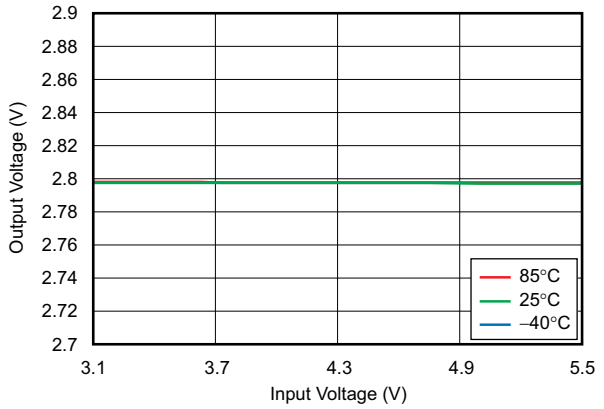
V_{OUT} = 2.8 V

Figure 2. Load Regulation



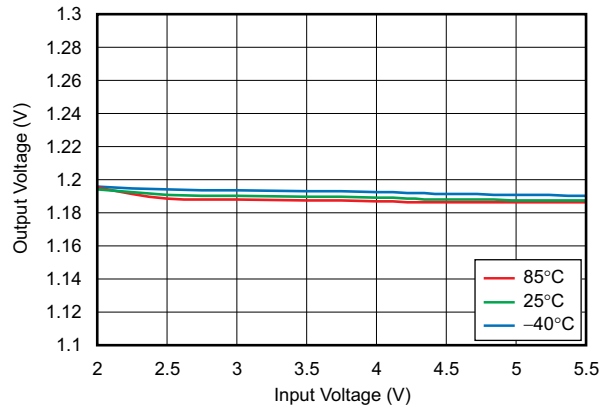
V_{OUT} = 1.2 V, I_{OUT} = 10 mA

Figure 3. Line Regulation



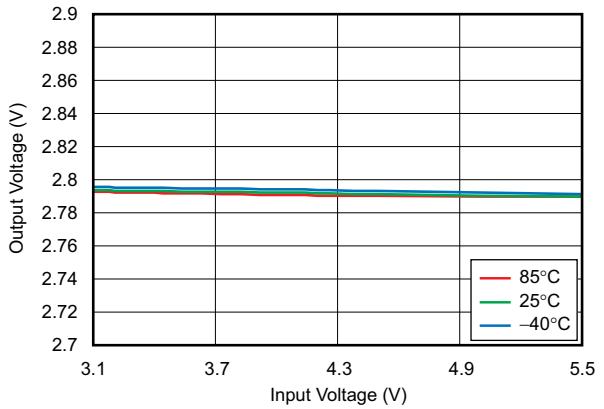
V_{OUT} = 2.8 V, I_{OUT} = 10 mA

Figure 4. Line Regulation



V_{OUT} = 1.2 V, I_{OUT} = 150 mA

Figure 5. Line Regulation

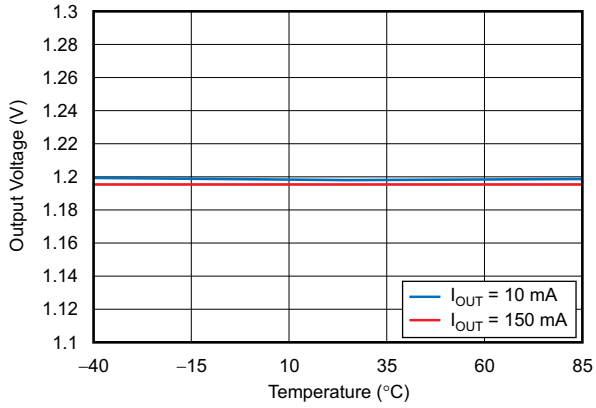


V_{OUT} = 2.8 V, I_{OUT} = 150 mA

Figure 6. Line Regulation

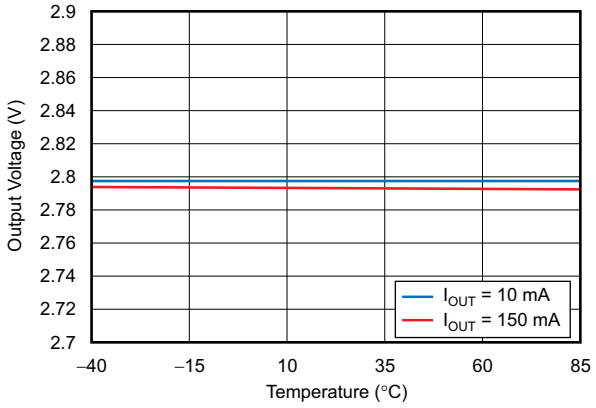
Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



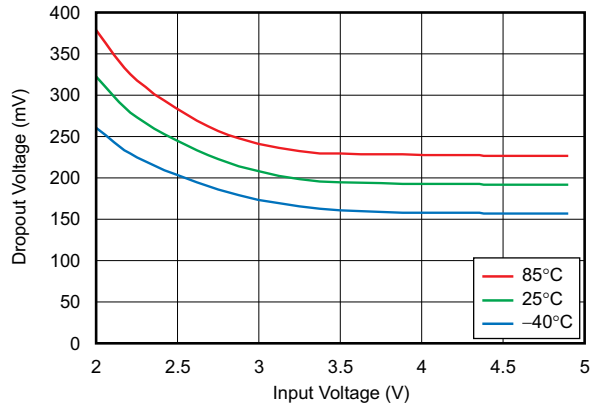
V_{OUT} = 1.2 V

Figure 7. Output Voltage vs Temperature



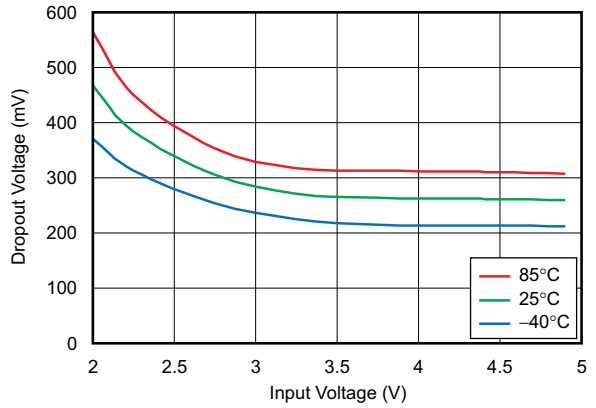
V_{OUT} = 2.8 V

Figure 8. Output Voltage vs Temperature



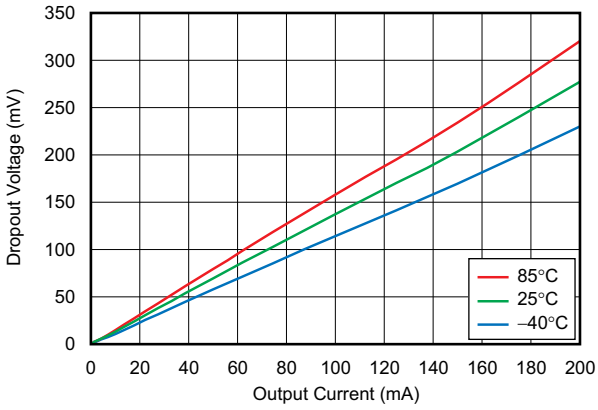
I_{OUT} = 150 mA

Figure 9. Dropout Voltage vs Input Voltage



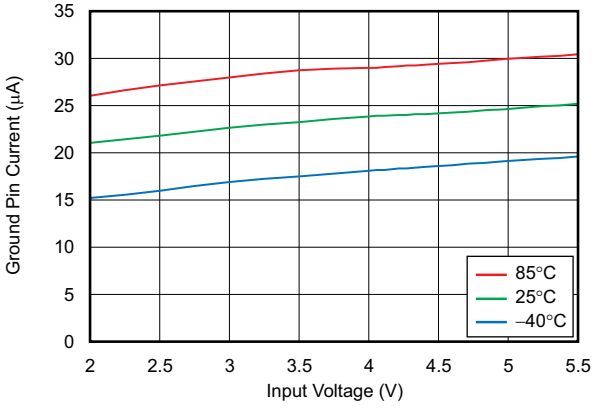
I_{OUT} = 200 mA

Figure 10. Dropout Voltage vs Input Voltage



V_{OUT} = 2.8 V

Figure 11. Dropout Voltage vs Output Current

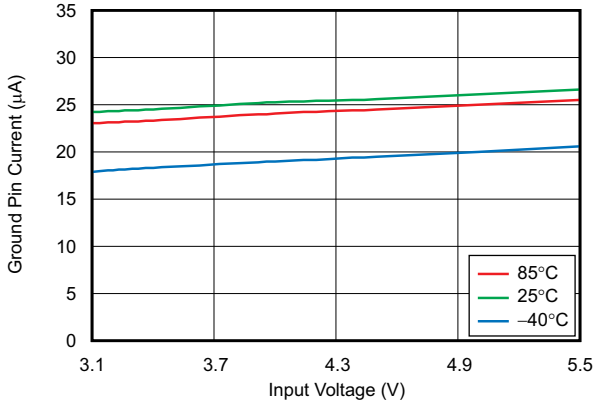


V_{OUT} = 1.2 V, I_{OUT} = 0 mA

Figure 12. Ground Pin Current vs Input Voltage

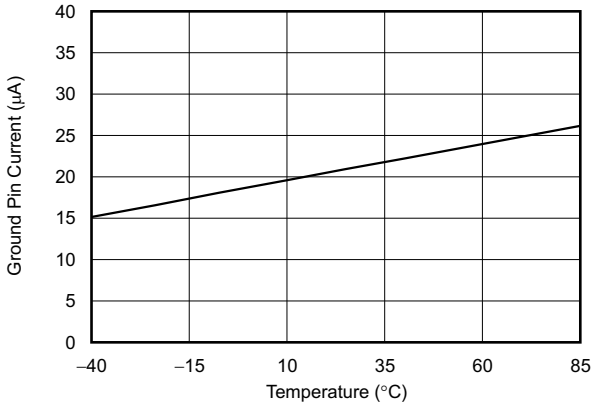
Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



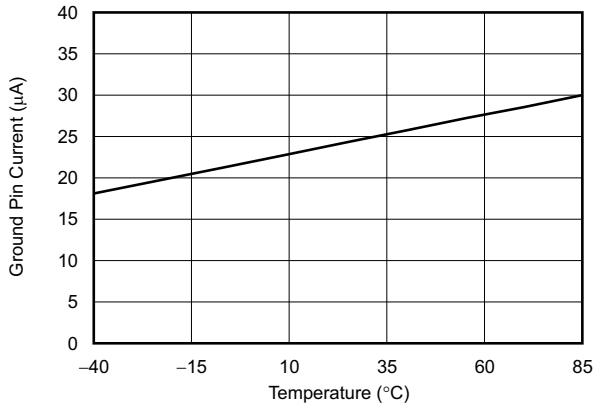
V_{OUT} = 2.8 V, I_{OUT} = 0 mA

Figure 13. Ground Pin Current vs Input Voltage



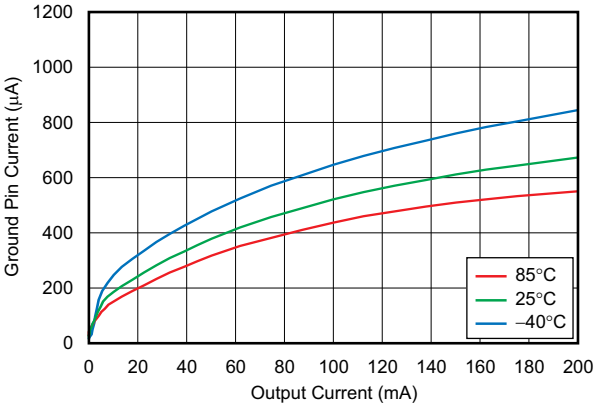
V_{OUT} = 1.2 V, I_{OUT} = 0 mA

Figure 14. Ground Pin Current vs Temperature



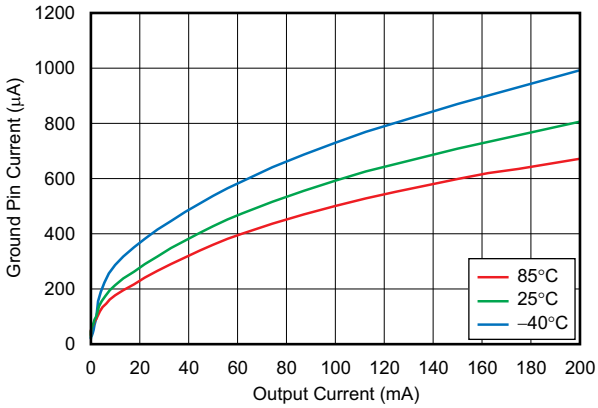
V_{OUT} = 2.8 V, I_{OUT} = 0 mA

Figure 15. Ground Pin Current vs Temperature



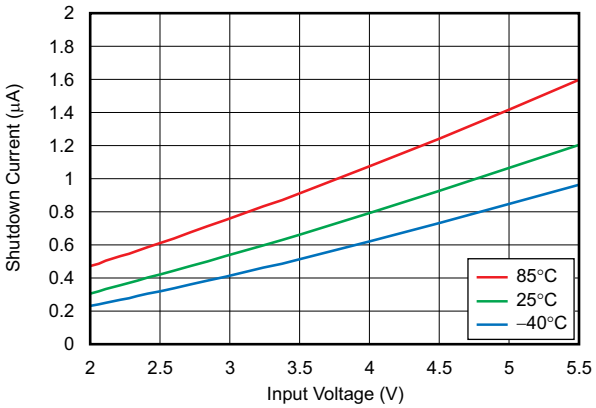
V_{OUT} = 1.2 V

Figure 16. Ground Pin Current vs Output Current



V_{OUT} = 2.8 V

Figure 17. Ground Pin Current vs Output Current

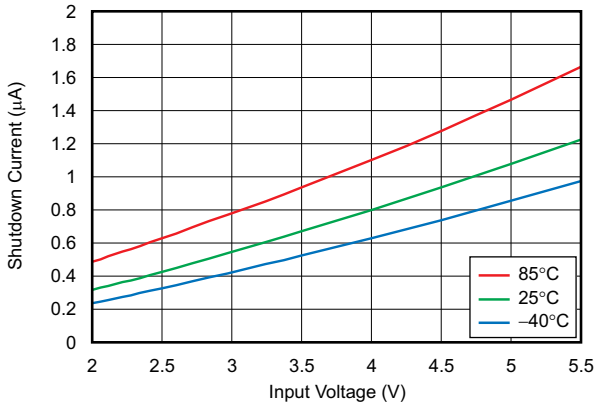


V_{OUT} = 1.2 V

Figure 18. Shutdown Current vs Input Voltage

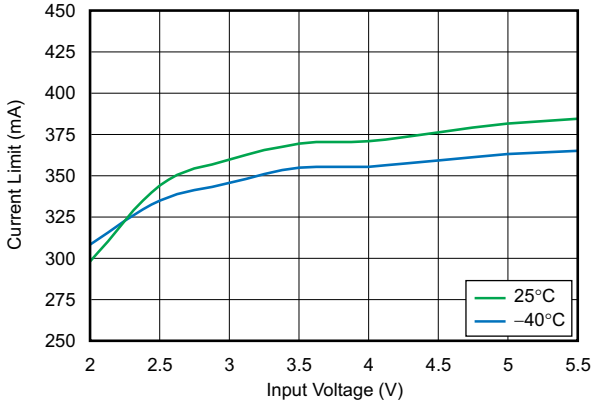
Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



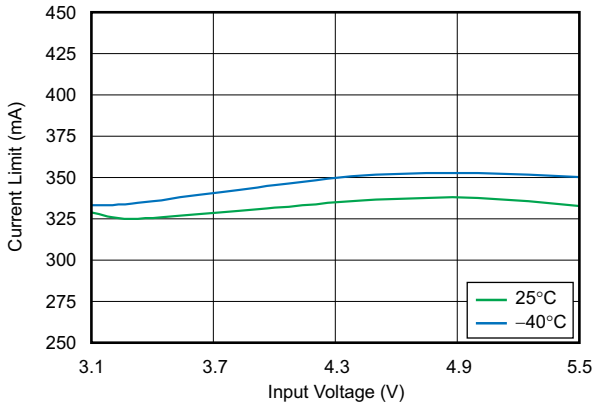
V_{OUT} = 2.8 V

Figure 19. Shutdown Current vs Input Voltage



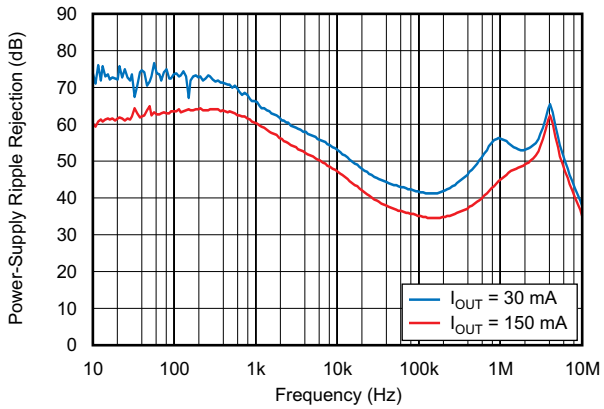
V_{OUT} = 1.2 V

Figure 20. Current Limit vs Input Voltage



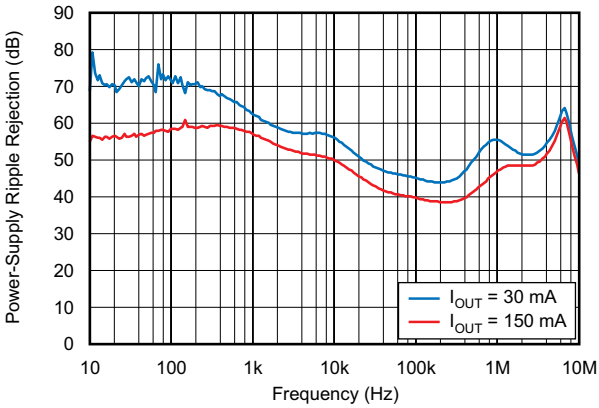
V_{OUT} = 2.8 V

Figure 21. Current Limit vs Input Voltage



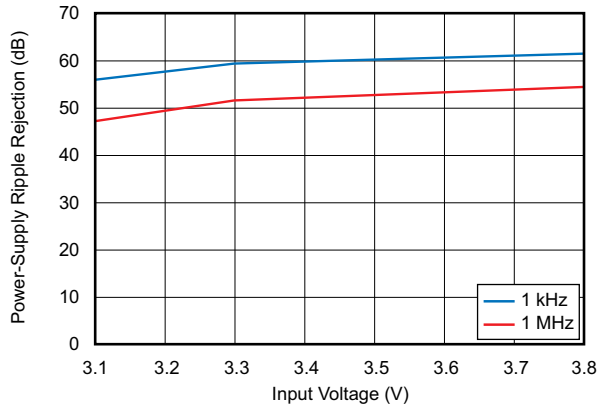
V_{OUT} = 1.2 V

Figure 22. Power-Supply Ripple Rejection vs Frequency



V_{OUT} = 2.8 V

Figure 23. Power-Supply Ripple Rejection vs Frequency

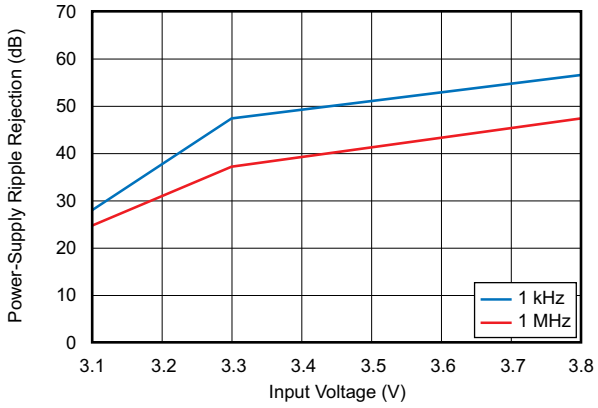


V_{OUT} = 2.8 V, I_{OUT} = 30 mA

Figure 24. Power-Supply Ripple Rejection vs Input Voltage

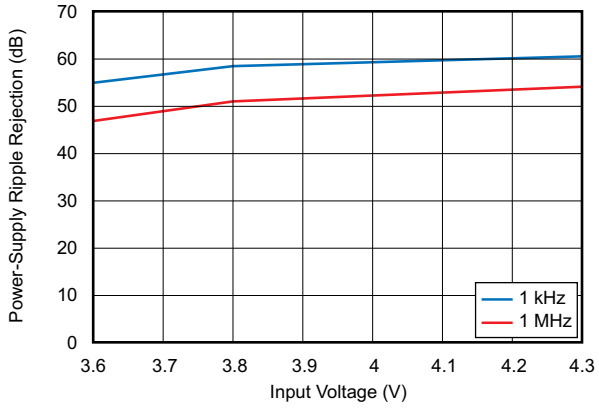
Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



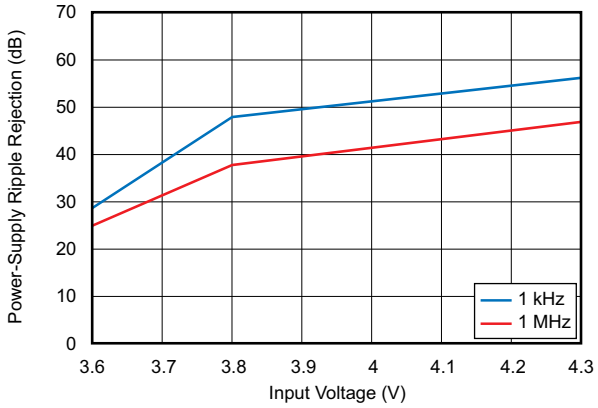
V_{OUT} = 2.8 V, I_{OUT} = 150 mA

Figure 25. Power-Supply Ripple Rejection vs Input Voltage



V_{OUT} = 3.3 V, I_{OUT} = 30 mA

Figure 26. Power-Supply Ripple Rejection vs Input Voltage



V_{OUT} = 3.3 V, I_{OUT} = 150 mA

Figure 27. Power-Supply Ripple Rejection vs Input Voltage

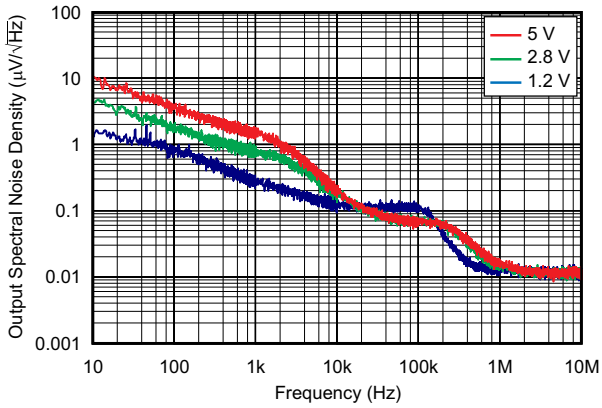
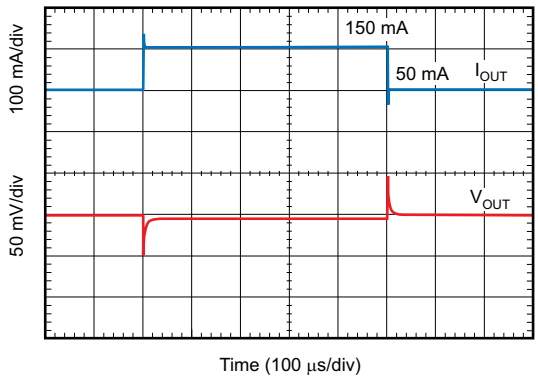
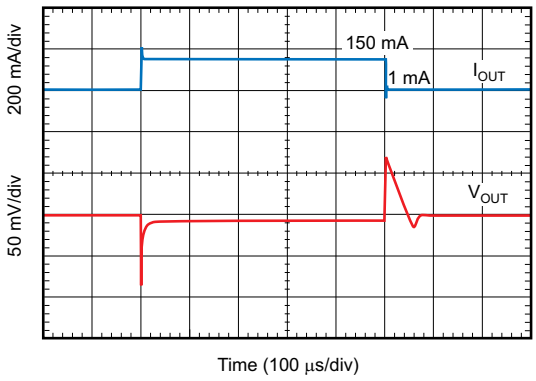


Figure 28. Output Spectral Noise Density vs Frequency



V_{OUT} = 1.2 V

Figure 29. Load Transient Response

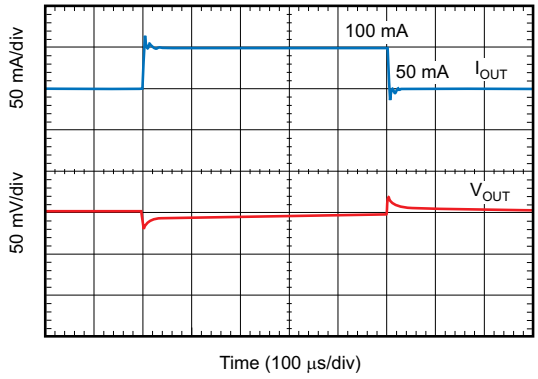


V_{OUT} = 1.2 V

Figure 30. Load Transient Response

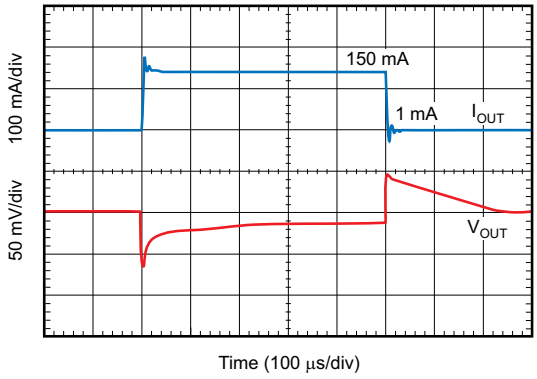
Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



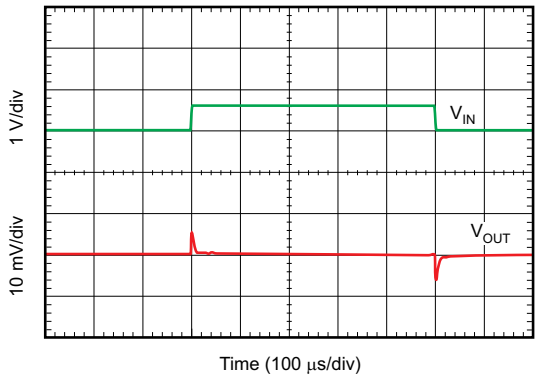
V_{OUT} = 2.8 V

Figure 31. Load Transient Response



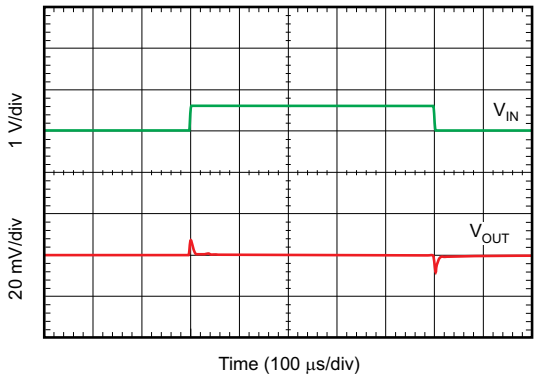
V_{OUT} = 2.8 V

Figure 32. Load Transient Response



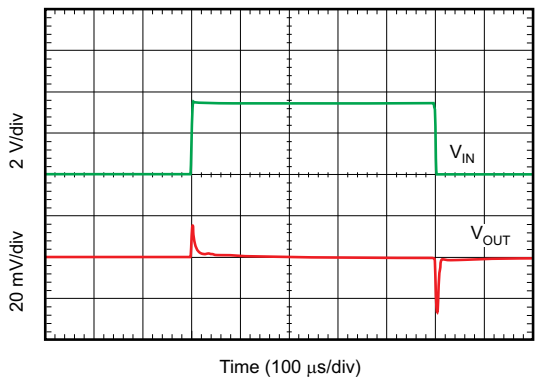
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

Figure 33. Line Transient Response



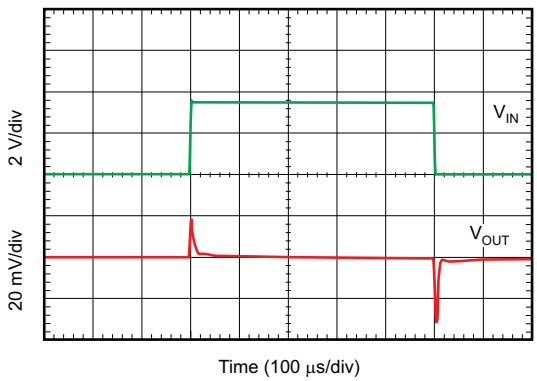
V_{OUT} = 1.2 V, I_{OUT} = 200 mA

Figure 34. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 150 mA

Figure 35. Line Transient Response

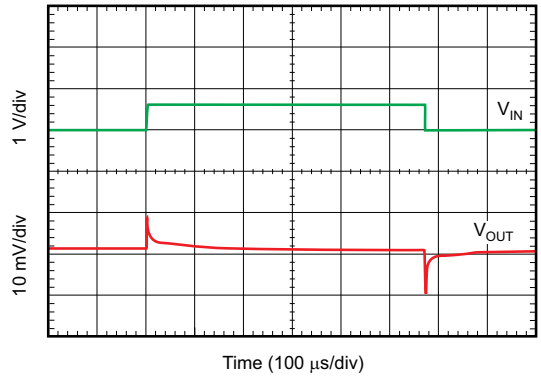


V_{OUT} = 1.2 V, I_{OUT} = 200 mA

Figure 36. Line Transient Response

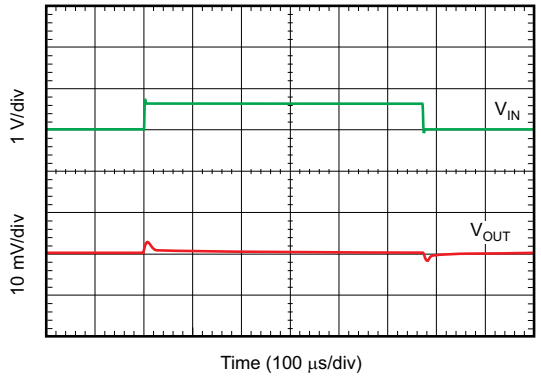
Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



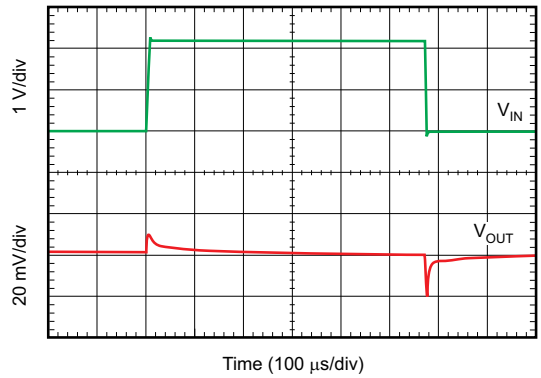
V_{OUT} = 2.8 V, I_{OUT} = 150 mA

Figure 37. Line Transient Response



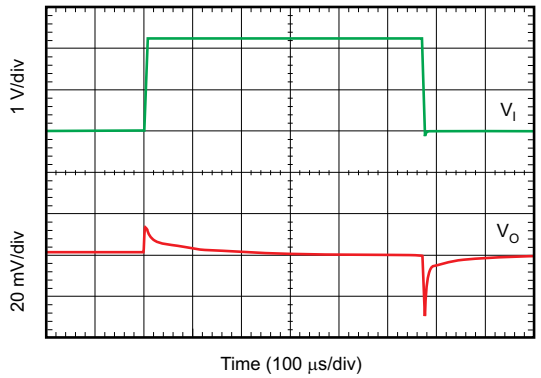
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

Figure 38. Line Transient Response



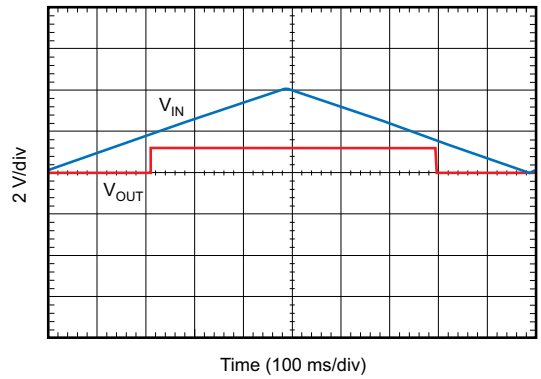
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

Figure 39. Line Transient Response



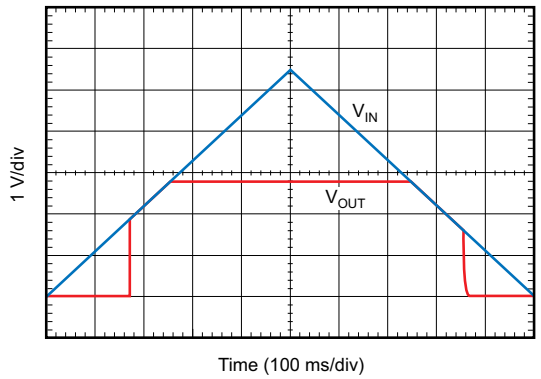
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

Figure 40. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 30 mA

Figure 41. V_{IN} Ramp Up, Ramp Down Response



V_{OUT} = 2.8 V, I_{OUT} = 30 mA

Figure 42. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV742P device belongs to a family of LDOs. This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics [combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom] make this device ideal for portable RF applications.

7.2 Functional Block Diagrams

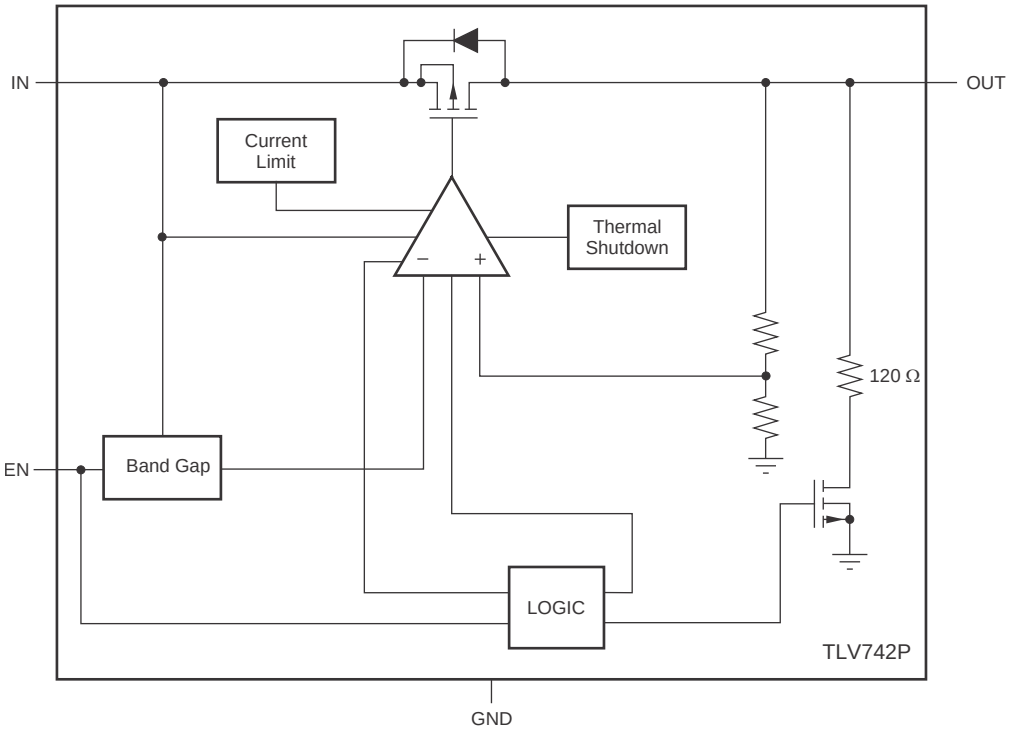


Figure 43. TLV742P Block Diagram

7.3 Feature Description

This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device is –40°C to +125°C.

7.3.1 Internal Current Limit

The internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_L$. The PMOS pass transistor dissipates ($V_{IN} – V_{OUT}$) × I_{LIMIT} until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see *Thermal Information* for more details.

The PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV742P version has internal active pulldown circuitry that discharges the output with a time constant as given by Equation 1:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

7.4 Device Functional Modes

The TLV742P series is specified over the recommended operating conditions (see *Recommended Operating Conditions*). The specifications may not be met when exposed to conditions outside of the recommended operating range.

To turn on the regulator, the EN pin must be driven over 0.9 V. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device typically reduces to 1 µA.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV742P is a LDO with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device series is –40°C to +125°C.

8.2 Typical Application

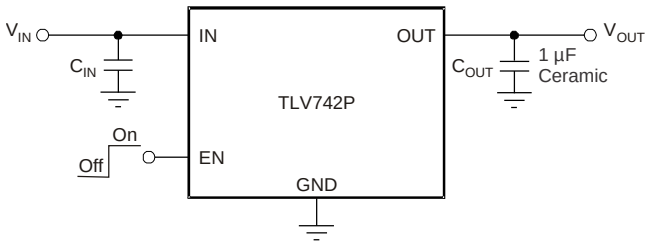


Figure 44. Typical Application Circuit

8.2.1 Design Requirements

Provide an input supply with adequate headroom to meet minimum V_{IN} requirements (as listed in Table 1), compensate for the GND pin current, and to power the load.

Table 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V to 3.6 V
Output voltage	1.2 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Generally, 1-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV742P is designed to be stable with an effective capacitance of 0.1 µF or larger at the output. As a result, the device is stable with capacitors of other dielectric types if the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking bias voltage and temperature derating into consideration. In addition to using less expensive dielectrics, this stability with 0.1-µF effective capacitance enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions is less than 0.1 µF. Maximum ESR must be less than 200 mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be required if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2-Ω, a 0.1-µF input capacitor may be required to ensure stability.

8.2.2.2 Dropout Voltage

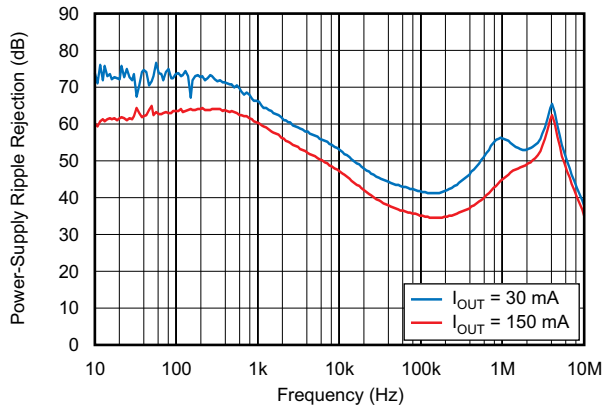
The TLV742P series of LDOs use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions similar to a resistor in dropout.

PSRR and transient response degrade when (V_{IN} – V_{OUT}) approaches dropout.

8.2.2.3 Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves



V_{OUT} = 1.2 V

Figure 45. Power-Supply Ripple Rejection vs Frequency

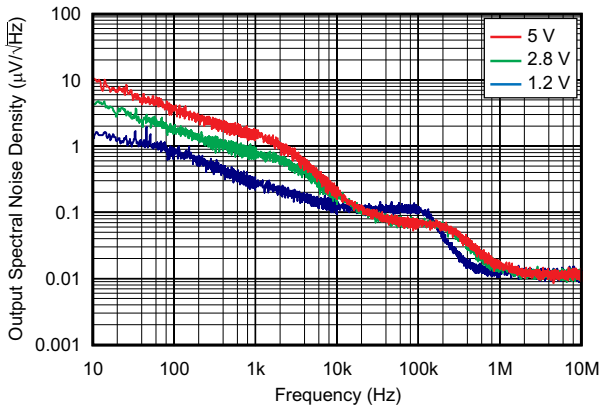
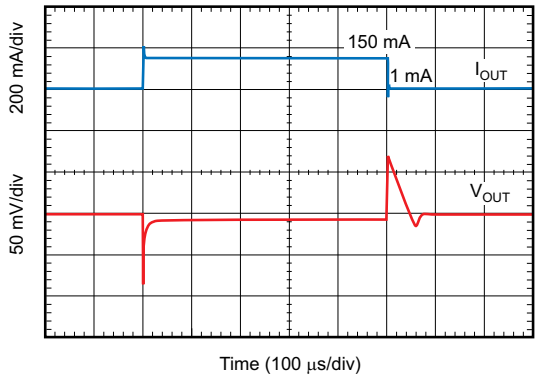
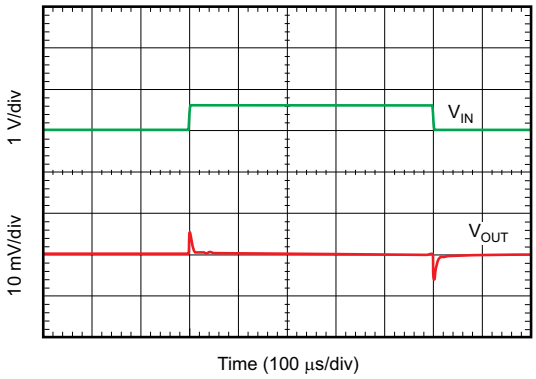


Figure 46. Output Spectral Noise Density vs Frequency



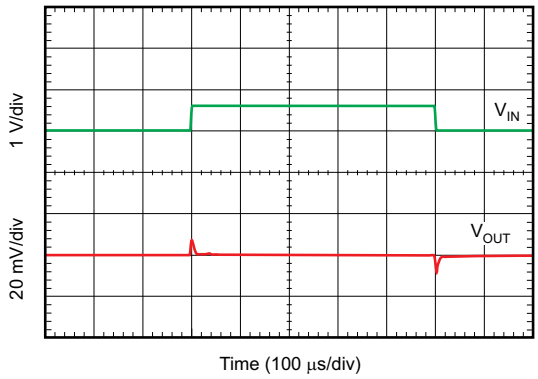
V_{OUT} = 1.2 V

Figure 47. Load Transient Response



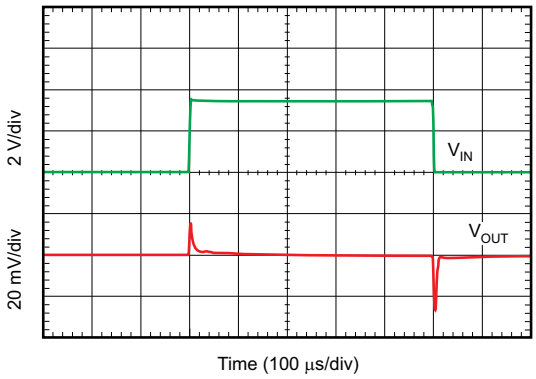
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

Figure 48. Line Transient Response



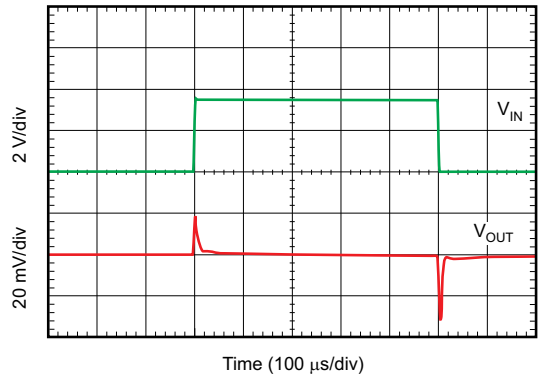
V_{OUT} = 1.2 V, I_{OUT} = 200 mA

Figure 49. Line Transient Response



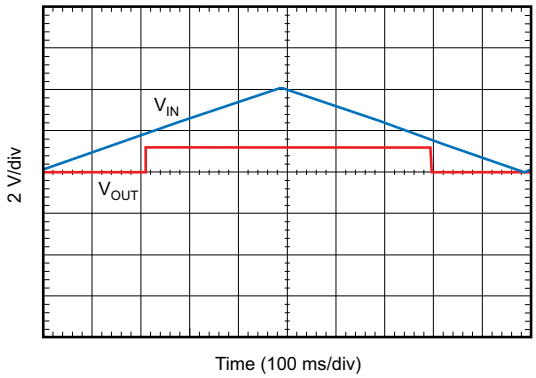
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

Figure 50. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 200 mA

Figure 51. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 30 mA

Figure 52. V_{IN} Ramp Up, Ramp Down Response

8.3 Do's and Don'ts

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 1-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2 V and 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well-regulated (see Figure 33 through Figure 40). If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device, as shown in Figure 53. Connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors can degrade PSRR performance.

10.1.2 Package Mounting

Solder pad footprint recommendations are available from the TI website at www.ti.com. The recommended land pattern for the DQN (X2SON-4) package is provided in the *Mechanical, Packaging, and Orderable Information* section.

10.2 Layout Example

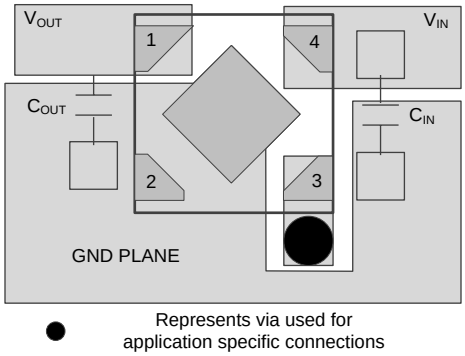


Figure 53. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enables again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, which protects the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the LDO is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the LDO into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are shown in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers improves heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV742P. *TLV70728EVM-612* details the design kits and evaluation modules for TLV70728EVM-612.

The EVM can be requested at the Texas Instruments website through the TLV742P product folder or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Ordering Information(1)

PRODUCT	V_{OUT}(2)
TLV742**xx(x)***Pyyyz*	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V, 285 = 2.85 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is package quantity. Use ***R*** for reel (3000 pieces), and ***T*** for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.85 V to 5 V in 50-mV increments are available. Contact factory for details and availability.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV74211PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8H	Samples
TLV74212PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8G	Samples
TLV74215PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8F	Samples
TLV74218PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8E	Samples
TLV74225PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS	Samples
TLV74227PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8D	Samples
TLV74228PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8C	Samples
TLV74229PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8B	Samples
TLV74230PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT	Samples
TLV74233PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

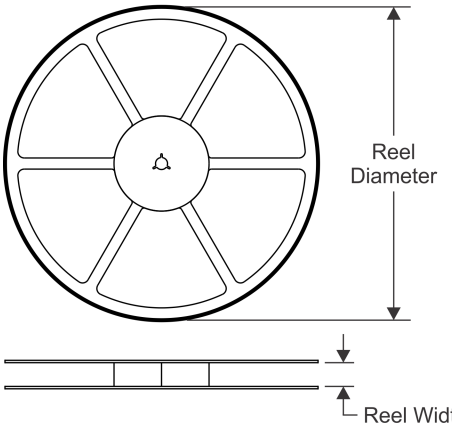
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

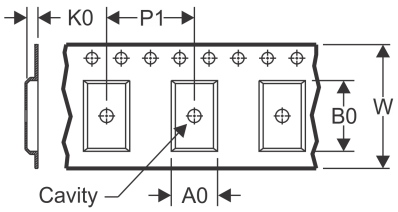
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

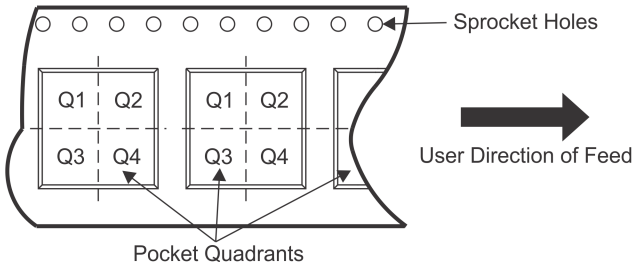


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

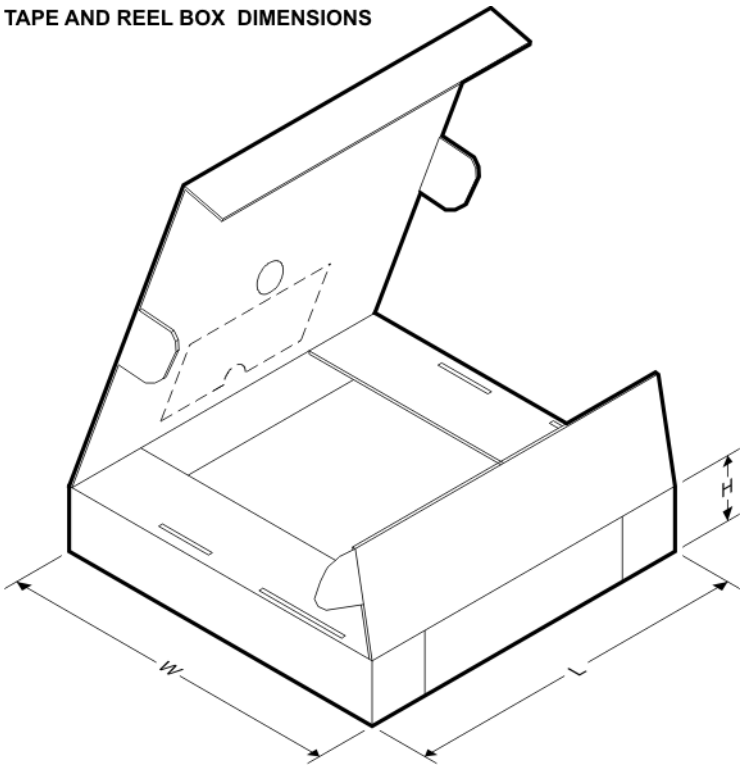
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74211PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74212PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74215PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74218PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74225PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74227PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74228PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74229PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74230PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74233PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74211PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74212PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74215PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74218PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74225PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74227PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74228PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74229PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74230PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74233PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

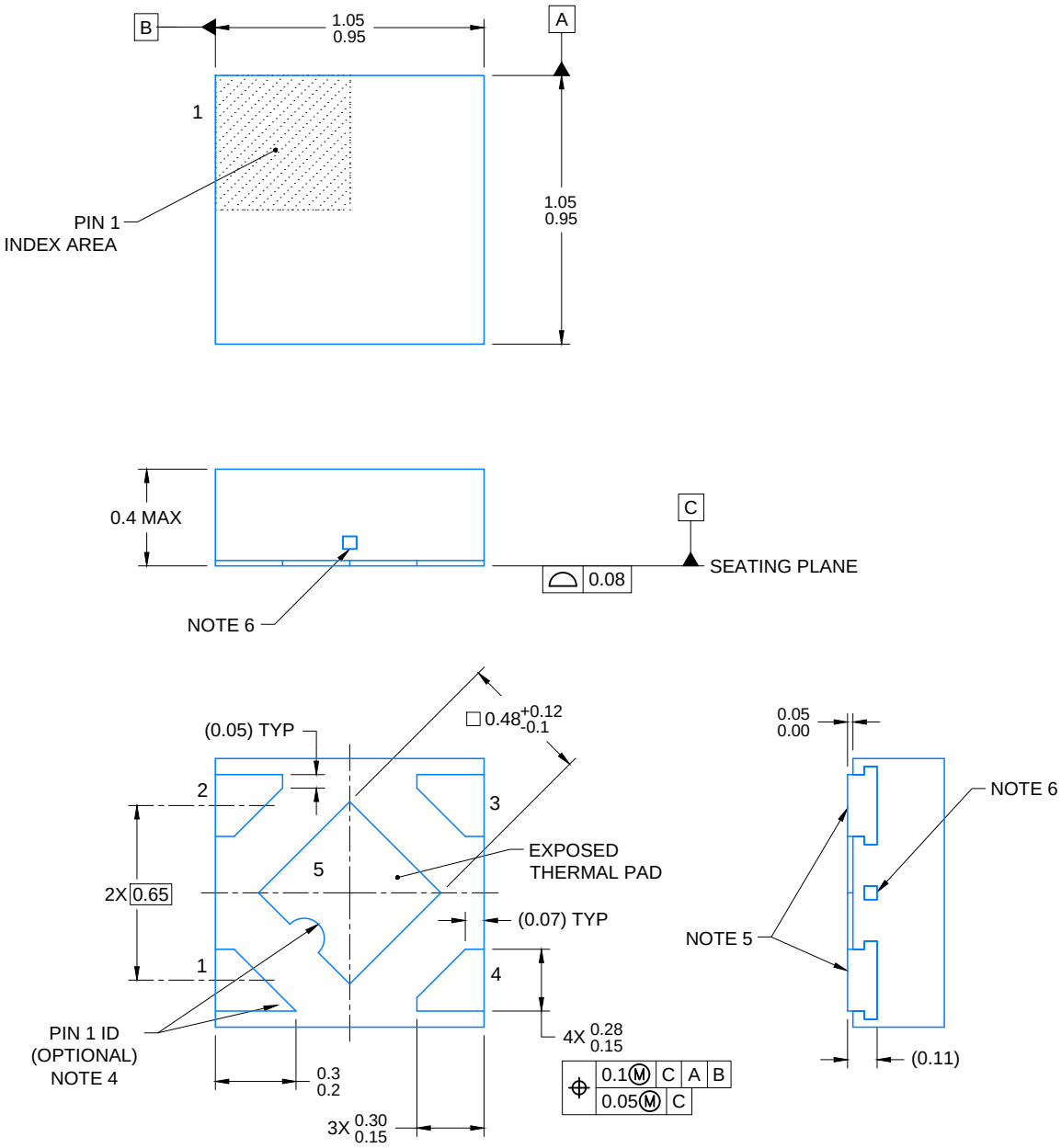
4210367/F

PACKAGE OUTLINE

DQN0004A

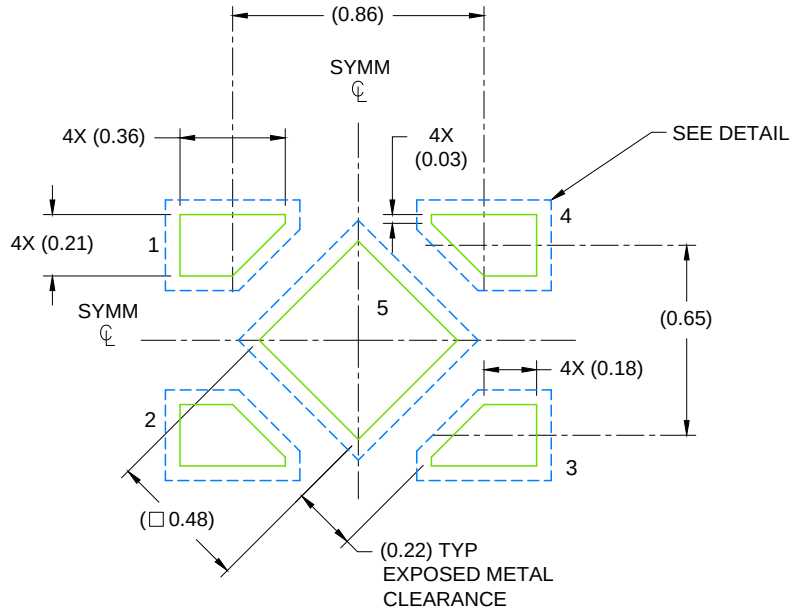
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



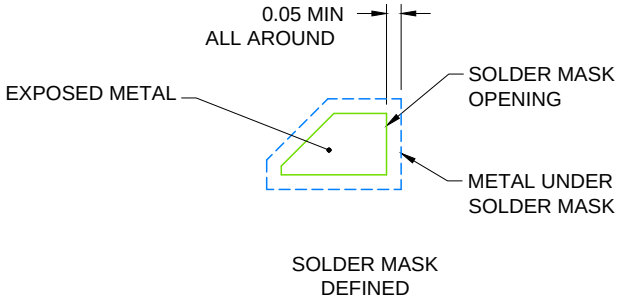
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

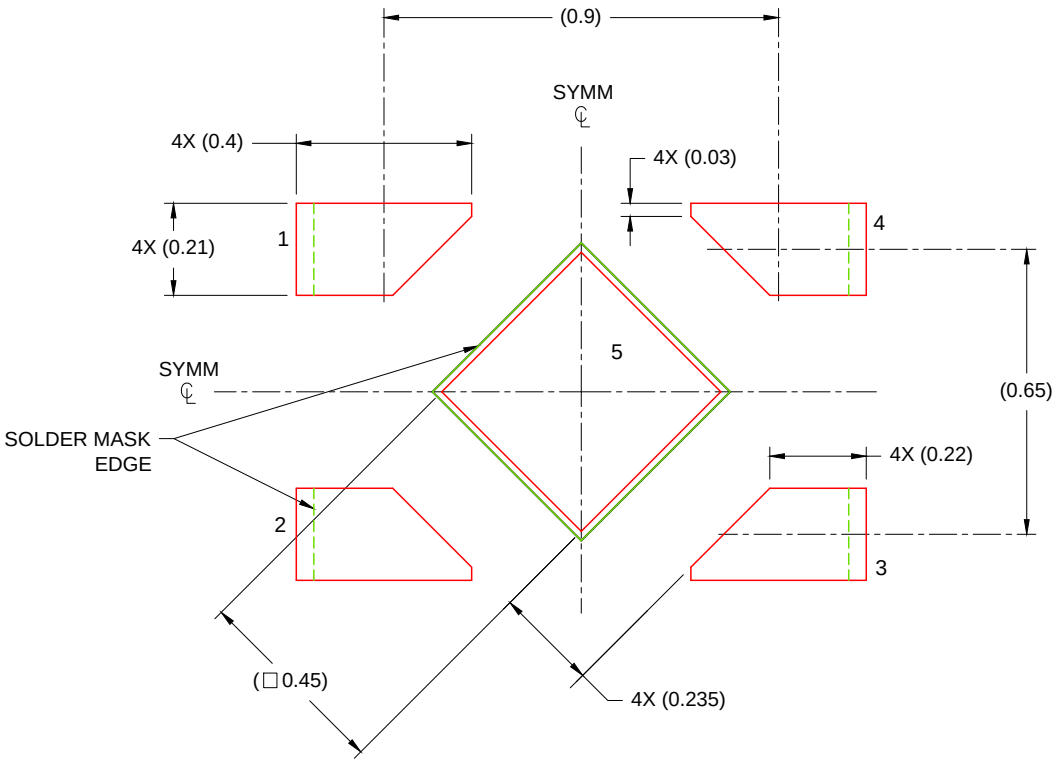


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265