



## Data Sheet

## $\pi$ 140U/ $\pi$ 141U/ $\pi$ 142U

### FEATURES

Ultra low power consumption (150Kbps):

0.55mA/Channel

High data rate:  $\pi$ 14xAxx: 600Mbps  
 $\pi$ 14xExx: 200Mbps  
 $\pi$ 14xMxx: 10Mbps  
 $\pi$ 14xUxx: 150kbps

High common-mode transient immunity: 150 kV/ $\mu$ s typical

High robustness to radiated and conducted noise

Isolation voltages:

$\pi$ 14xx3x: AC 3000Vrms

$\pi$ 14xx6x: AC 6000Vrms

High ESD rating:

ESDA/JEDEC JS-001-2017

Human body model (HBM)  $\pm$ 8kV, all pins

Safety and regulatory approvals (Pending):

UL certificate number: E494497

3000Vrms/6000Vrms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE certificate number: 40047929

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

V<sub>IORM</sub> = 707V peak/1200V peak

CQC certification per GB4943.1-2011

3 V to 5.5 V level translation

AEC-Q100 qualification

Wide temperature range: -40°C to 125°C

16-lead, RoHS-compliant, SOIC\_N, SOIC\_W and SSOP package

### APPLICATIONS

General-purpose multichannel isolation

Industrial field bus isolation

### GENERAL DESCRIPTION

The  $\pi$ 1xxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using matured standard semiconductor CMOS technology and 2PaiSEMI *iDivider* technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (*iDivider* technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The  $\pi$ 1xxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage

rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

### FUNCTIONAL BLOCK DIAGRAMS

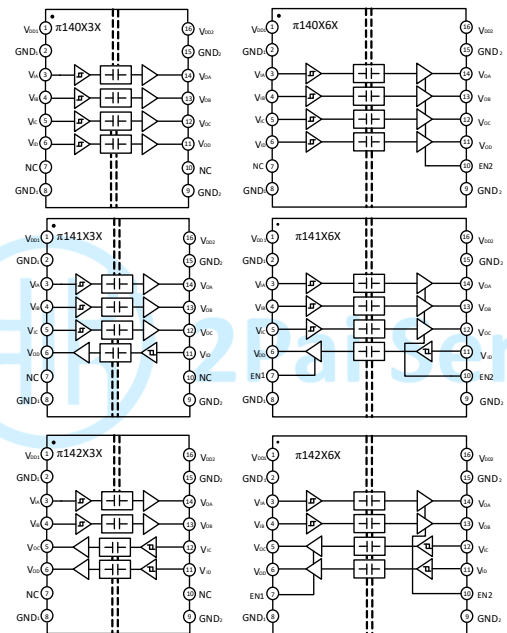


Figure1.  $\pi$ 140xxx/ $\pi$ 141xxx/ $\pi$ 142xxx functional Block Diagram

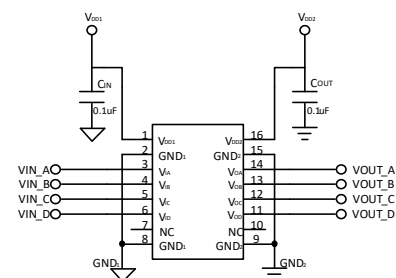
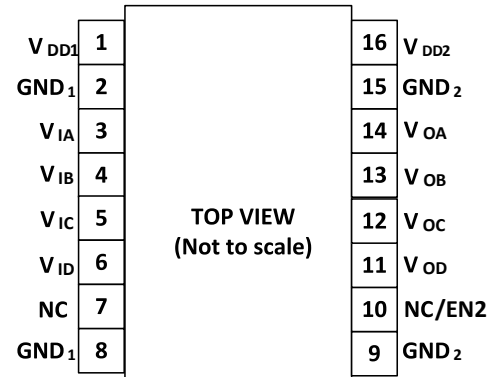


Figure2.  $\pi$ 140x3x Typical Application Circuit

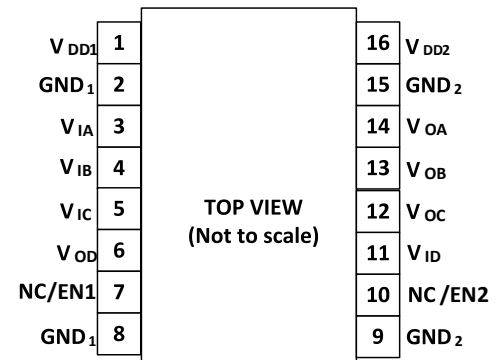
## PIN CONFIGURATIONS AND FUNCTIONS

 $\pi$ 140Uxx Pin Function Descriptions

Pin No.	Name	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>IC</sub>	Logic Input C.
6	V <sub>ID</sub>	Logic Input D.
7	NC	No connect.
8	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC /EN2	No connect for $\pi$ 140U3X. Output enable for $\pi$ 140U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
11	V <sub>OD</sub>	Logic Output D.
12	V <sub>OC</sub>	Logic Output C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
15	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

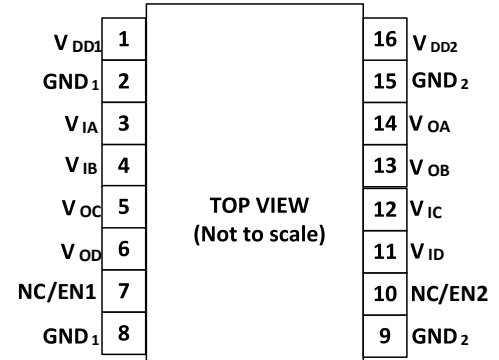
Figure3  $\pi$ 140Uxx Pin Configuration $\pi$ 141Uxx Pin Function Descriptions

Pin No.	Name	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>IC</sub>	Logic Input C.
6	V <sub>OD</sub>	Logic Output D.
7	NC/EN1	No connect for $\pi$ 141U3X. Output enable 1 for $\pi$ 141U6X. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
8	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC/EN2	No connect for $\pi$ 141U3X. Output enable 2 for $\pi$ 141U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
11	V <sub>ID</sub>	Logic Input D.
12	V <sub>OC</sub>	Logic Output C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
15	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

Figure4.  $\pi$ 141Uxx Pin Configuration

$\pi$ 142Uxx Pin Function Descriptions

Pin No.	Name	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>OC</sub>	Logic Output C.
6	V <sub>OD</sub>	Logic Output D.
7	NC/EN1	No connect for $\pi$ 142U3X. Output enable 1 for $\pi$ 142U6X. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
8	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC/EN2	No connect for $\pi$ 142U3X. Output enable 2 for $\pi$ 142U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
11	V <sub>ID</sub>	Logic Input D.
12	V <sub>IC</sub>	Logic Input C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
15	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

Figure 5.  $\pi$ 142Uxx Pin Configuration

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.Table 1. Absolute Maximum Ratings<sup>4</sup>

Parameter	Rating
Supply Voltages (V <sub>DD1</sub> -GND <sub>1</sub> , V <sub>DD2</sub> -GND <sub>2</sub> )	-0.5 V to +7.0 V
Input Voltages (V <sub>IA</sub> , V <sub>IB</sub> ) <sup>1</sup>	-0.5 V to V <sub>DDx</sub> + 0.5 V
Output Voltages (V <sub>OA</sub> , V <sub>OB</sub> ) <sup>1</sup>	-0.5 V to V <sub>DDx</sub> + 0.5 V
Average Output Current per Pin <sup>2</sup> Side 1 Output Current (I <sub>O1</sub> )	-10 mA to +10 mA
Average Output Current per Pin <sup>2</sup> Side 2 Output Current (I <sub>O2</sub> )	-10 mA to +10 mA
Common-Mode Transients Immunity <sup>3</sup>	-150 kV/μs to +150 kV/μs
Storage Temperature (T <sub>ST</sub> ) Range	-65°C to +150°C
Ambient Operating Temperature (T <sub>A</sub> ) Range	-40°C to +125°C

Notes:

<sup>1</sup> V<sub>DDx</sub> is the side voltage power supply V<sub>DD</sub>, where x = 1 or 2.<sup>2</sup> See Figure 6 for the maximum rated current values for various temperatures.<sup>3</sup> See Figure 18 for Common-mode transient immunity (CMTI) measurement.<sup>4</sup> Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## RECOMMENDED OPERATING CONDITIONS

**Table 2. Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DDx}^1$	3		5.5	V
High Level Input Signal Voltage	$V_{IH}$	$0.7 \cdot V_{DDx}^1$		$V_{DDx}^1$	V
Low Level Input Signal Voltage	$V_{IL}$	0		$0.3 \cdot V_{DDx}^1$	V
High Level Output Current	$I_{OH}$	-6			mA
Low Level Output Current	$I_{OL}$			6	mA
Maximum Data Rate		0		150	Kbps
Junction Temperature	$T_J$	-40		150	°C
Ambient Operating Temperature	$T_A$	-40		125	°C

Notes:

<sup>1</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where x = 1 or 2.

## Truth Tables

**Table 3.  $\pi$ 140U3x/ $\pi$ 141U3x/ $\pi$ 142U3x Truth Table**

$V_{ix}$ Input <sup>1</sup>	$V_{DDI}$ State <sup>1</sup>	$V_{DDO}$ State <sup>1</sup>	Default Low $V_{Ox}$ Output <sup>1</sup>	Default High $V_{Ox}$ Output <sup>1</sup>	Test Conditions /Comments
Low	Powered <sup>2</sup>	Powered <sup>2</sup>	Low	Low	Normal operation
High	Powered <sup>2</sup>	Powered <sup>2</sup>	High	High	Normal operation
Open	Powered <sup>2</sup>	Powered <sup>2</sup>	Low	High	Default output
Don't Care <sup>4</sup>	Unpowered <sup>3</sup>	Powered <sup>2</sup>	Low	High	Default output <sup>5</sup>
Don't Care <sup>4</sup>	Powered <sup>2</sup>	Unpowered <sup>3</sup>	High Impedance	High Impedance	

Notes:

<sup>1</sup>  $V_{ix}/V_{Ox}$  are the input/output signals of a given channel (A or B).  $V_{DDI}/V_{DDO}$  are the supply voltages on the input/output signal sides of this given channel.

<sup>2</sup> Powered means  $V_{DDx} \geq 2.9$  V

<sup>3</sup> Unpowered means  $V_{DDx} < 2.3$  V

<sup>4</sup> Input signal ( $V_{ix}$ ) must be in a low state to avoid powering the given  $V_{DDI}$  through its ESD protection circuitry.

<sup>5</sup> If the  $V_{DDI}$  goes into unpowered status, the channel outputs the default logic signal after around 1 $\mu$ s. If the  $V_{DDI}$  goes into powered status, the channel outputs the input status logic signal after around 3 $\mu$ s.

**Table 4.  $\pi$ 140U6x/ $\pi$ 141U6x/ $\pi$ 142U6x Truth Table**

$V_{ix}$ Input <sup>1</sup>	EN1/2 State	$V_{DDI}$ State <sup>1</sup>	$V_{DDO}$ State <sup>1</sup>	Default Low $V_{Ox}$ Output <sup>1</sup>	Default High $V_{Ox}$ Output <sup>1</sup>	Test Conditions /Comments
Low	High or NC	Powered <sup>2</sup>	Powered <sup>2</sup>	Low	Low	Normal operation
High	High or NC	Powered <sup>2</sup>	Powered <sup>2</sup>	High	High	Normal operation
Don't Care <sup>4</sup>	L	Powered <sup>2</sup>	Powered <sup>2</sup>	High Impedance	High Impedance	Disabled
Open	High or NC	Powered <sup>2</sup>	Powered <sup>2</sup>	Low	High	Default output <sup>5</sup>
Don't Care <sup>4</sup>	High or NC	Unpowered <sup>3</sup>	Powered <sup>2</sup>	Low	High	Default output <sup>5</sup>
Don't Care <sup>4</sup>	L	Unpowered <sup>3</sup>	Powered <sup>2</sup>	High Impedance	High Impedance	
Don't Care <sup>4</sup>	Don't Care <sup>4</sup>	Powered <sup>2</sup>	Unpowered <sup>3</sup>	High Impedance	High Impedance	

Notes:

<sup>1</sup>  $V_{ix}/V_{Ox}$  are the input/output signals of a given channel (A or B).  $V_{DDI}/V_{DDO}$  are the supply voltages on the input/output signal sides of this given channel.

<sup>2</sup> Powered means  $V_{DDx} \geq 2.9$  V

<sup>3</sup> Unpowered means  $V_{DDx} < 2.3$  V

<sup>4</sup> Input signal ( $V_{ix}$ ) must be in a low state to avoid powering the given  $V_{DDI}$  through its ESD protection circuitry.

<sup>5</sup>If the  $V_{DDI}$  goes into unpowered status, the channel outputs the default logic signal after around 1us. If the  $V_{DDI}$  goes into powered status, the channel outputs the input status logic signal after around 3us.

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

**Table 5. Switching Specifications**

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			6.5	us	Within pulse width distortion (PWD) limit
Maximum Data Rate		150			Kbps	Within PWD limit
Propagation Delay Time <sup>1,4</sup>	$t_{pHL}, t_{pLH}$		3.0	4.5	us	The different time between 50% input signal to 50% output signal 50% @ $5V_{DC}$ supply
			3.2	4.8	us	@ $3.3V_{DC}$ supply
Pulse Width Distortion <sup>4</sup>	PWD	0	0.02	0.2	us	The max different time between $t_{pHL}$ and $t_{pLH}$ @ $5V_{DC}$ supply. And The value is $ t_{pHL} - t_{pLH} $
		0	0.02	0.2	us	@ $3.3V_{DC}$ supply
Part to Part Propagation Delay Skew <sup>4</sup>	$t_{PSK}$			0.3	us	The max different propagation delay time between any two devices at the same temperature, load and voltage @ $5V_{DC}$ supply
				0.3	us	@ $3.3V_{DC}$ supply
Channel to Channel Propagation Delay Skew <sup>4</sup>	$t_{CSK}$		0	0.2	us	The max amount propagation delay time differs between any two output channels in the single device @ $5V_{DC}$ supply.
			0	0.2	us	@ $3.3V_{DC}$ supply
Output Signal Rise/Fall Time <sup>4</sup>	$t_r/t_f$		1.5		ns	10% to 90% signal terminated $50\Omega$ , See figure15.
Common-Mode Transient Immunity <sup>3</sup>	CMTI	100	150		kV/ $\mu s$	$V_{IN} = V_{DDX}^2$ or 0V, $V_{CM} = 1000$ V
ESD (HBM - Human body model)	ESD		$\pm 8$		kV	All pins

Notes:

<sup>1</sup>  $t_{pLH}$  = low-to-high propagation delay time,  $t_{pHL}$  = high-to-low propagation delay time. See figure 16.

<sup>2</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where x = 1 or 2.

<sup>3</sup> See Figure19 for Common-mode transient immunity (CMTI) measurement.

<sup>4</sup> Output Signal Terminated  $50\Omega$ .

**Table 6. DC Specifications**

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	$V_{IT+}$		$0.6 * V_{DDx}^1$	$0.7 * V_{DDx}^1$	V	
Falling Input Signal Voltage Threshold	$V_{IT-}$	$0.3 * V_{DDx}^1$	$0.4 * V_{DDx}^1$		V	
High Level Output Voltage	$V_{OH}^1$	$V_{DDx} - 0.1$	$V_{DDx}$		V	-20 $\mu A$ output current
		$V_{DDx} - 0.2$	$V_{DDx} - 0.1$		V	-2 mA output current
Low Level Output Voltage	$V_{OL}$		0	0.1	V	20 $\mu A$ output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	$I_{IN}$	-10	0.5	10	$\mu A$	$0 V \leq \text{Signal voltage} \leq V_{DDx}^1$

$V_{DDx}^1$ Undervoltage Rising Threshold	$V_{DDxUV+}$	2.45	2.65	2.9	V
$V_{DDx}^1$ Undervoltage Falling Threshold	$V_{DDxUV-}$	2.3	2.5	2.75	V
$V_{DDx}^1$ Hysteresis	$V_{DDxUVH}$	0.15			V

Notes:

<sup>1</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where  $x = 1$  or  $2$ .**Table 7. Quiescent Supply Current** $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $C_L = 0$  pF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	
$\pi 140U_{xx}$ Quiescent Supply Current @ $5V_{DC}$ Supply	$I_{DD1}(Q)$	307	384	499	$\mu A$	0V Input signal	
	$I_{DD2}(Q)$	1416	1770	2301	$\mu A$	0V Input signal	
	$I_{DD1}(Q)$	122	152	198	$\mu A$	5V Input signal	
	$I_{DD2}(Q)$	1534	1918	2493	$\mu A$	5V Input signal	
	@ $3.3V_{DC}$ Supply	$I_{DD1}(Q)$	226	282	367	$\mu A$	0V Input signal
		$I_{DD2}(Q)$	1392	1740	2262	$\mu A$	0V Input signal
		$I_{DD1}(Q)$	120	150	195	$\mu A$	3.3V Input signal
		$I_{DD2}(Q)$	1517	1896	2465	$\mu A$	3.3V Input signal
$\pi 141U_{xx}$ Quiescent Supply Current @ $5V_{DC}$ Supply	$I_{DD1}(Q)$	584	731	950	$\mu A$	0V Input signal	
	$I_{DD2}(Q)$	1139	1424	1851	$\mu A$	0V Input signal	
	$I_{DD1}(Q)$	475	594	772	$\mu A$	5V Input signal	
	$I_{DD2}(Q)$	1182	1477	1920	$\mu A$	5V Input signal	
	@ $3.3V_{DC}$ Supply	$I_{DD1}(Q)$	517	647	840	$\mu A$	0V Input signal
		$I_{DD2}(Q)$	1101	1376	1789	$\mu A$	0V Input signal
		$I_{DD1}(Q)$	469	587	762	$\mu A$	3.3V Input signal
		$I_{DD2}(Q)$	1168	1460	1898	$\mu A$	3.3V Input signal
$\pi 142U_{xx}$ Quiescent Supply Current @ $5V_{DC}$ Supply	$I_{DD1}(Q)$	862	1077	1400	$\mu A$	0V Input signal	
	$I_{DD2}(Q)$	862	1078	1401	$\mu A$	0V Input signal	
	$I_{DD1}(Q)$	828	1035	1346	$\mu A$	5V Input signal	
	$I_{DD2}(Q)$	829	1036	1347	$\mu A$	5V Input signal	
	@ $3.3V_{DC}$ Supply	$I_{DD1}(Q)$	809	1011	1314	$\mu A$	0V Input signal
		$I_{DD2}(Q)$	810	1012	1316	$\mu A$	0V Input signal
		$I_{DD1}(Q)$	818	1023	1330	$\mu A$	3.3V Input signal
		$I_{DD2}(Q)$	819	1024	1331	$\mu A$	3.3V Input signal

**Table 8. Total Supply Current vs. Data Throughput ( $C_L = 0$  pF)** $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $C_L = 0$  pF, unless otherwise noted.

Parameter	Symbol	2 Kbps			50Kbps			150Kbps			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$\pi 140U_{xx}$ Supply Current @ $5V_{DC}$	$I_{DD1}$		0.26	0.39		0.26	0.39		0.26	0.39	mA	
	$I_{DD2}$		1.84	2.76		1.86	2.79		1.88	2.82		
	@ $3.3V_{DC}$	$I_{DD1}$		0.20	0.30		0.20	0.30		0.20	0.30	mA
		$I_{DD2}$		1.82	2.73		1.82	2.73		1.84	2.76	
$\pi 141U_{xx}$ Supply Current @ $5V_{DC}$	$I_{DD1}$		0.66	0.98		0.66	0.99		0.67	1.00	mA	

	I <sub>DD2</sub>	1.45	2.18	1.46	2.19	1.48	2.22	mA
	I <sub>DD1</sub>	0.61	0.91	0.61	0.92	0.61	0.92	mA
	I <sub>DD2</sub>	1.42	2.13	1.42	2.13	1.43	2.15	mA
$\pi$ 142Uxx Supply Current @5V <sub>DC</sub>	I <sub>DD1</sub>	1.05	1.58	1.06	1.59	1.08	1.62	mA
	I <sub>DD2</sub>	1.05	1.58	1.06	1.59	1.08	1.62	mA
@ 3.3V <sub>DC</sub>	I <sub>DD1</sub>	1.01	1.52	1.02	1.53	1.02	1.53	mA
	I <sub>DD2</sub>	1.01	1.52	1.02	1.53	1.02	1.53	mA

## INSULATION AND SAFETY RELATED SPECIFICATIONS

**Table 9. Insulation Specifications**

Parameter	Symbol	Value		Unit	Test Conditions/Comments
		$\pi$ 14xU3x	$\pi$ 14xU6x		
Rated Dielectric Insulation Voltage		3000	6000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	4	8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	4	8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		11	21	$\mu$ m min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II	II		Material Group (DIN VDE 0110, 1/89, Table 1)

## PACKAGE CHARACTERISTICS

**Table 10. Package Characteristics**

Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		$\pi$ 14xU3x	$\pi$ 14xU6x		
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>	10 <sup>11</sup>	10 <sup>11</sup>	$\Omega$	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>	0.6	0.6	pF	@1MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	$\theta_{JA}$	100	45	$^{\circ}$ C/W	Thermocouple located at center of package underside

Notes:

<sup>1</sup>The device is considered a 2-terminal device; SOIC-16 Pin 1 - Pin 8 (WSOIC-16 Pin 1-Pin8 and SSOP16 Pin 1-Pin8) are shorted together as the one terminal, and SOIC-16 Pin 9- Pin 16 (WSOIC-16 Pin 9-Pin16 and SSOP16 Pin 9-Pin16) are shorted together as the other terminal.

<sup>2</sup>Testing from the input signal pin to ground.

## REGULATORY INFORMATION

See Table 11 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

**Table 11. Regulatory**

Regulatory	$\pi$ 14xU3x	$\pi$ 14xU6x
UL	Recognized under UL 1577 Component Recognition Program <sup>1</sup> Single Protection, 3000 V rms Isolation Voltage File (E494497)	Recognized under UL 1577 Component Recognition Program <sup>1</sup> Single Protection, 6000 V rms Isolation Voltage File (pending)
CSA	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and

	IEC 60950-1, second edition, +A1+A2: Basic insulation at 500Vrms (707Vpeak) Reinforced insulation at 250 V rms (353 V peak) File (pending)	IEC 60950-1, second edition, +A1+A2: Basic insulation at 845Vrms (1200Vpeak) Reinforced insulation at 422V rms (600V peak) File (pending)
<b>VDE</b>	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup> Basic insulation, $V_{IORM} = 707$ V peak, $V_{IOSM} = 4615$ V peak  File (40047929)	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup> Basic insulation, $V_{IORM} = 1200$ Vpeak, $V_{IOSM} = 7000$ V peak  Reinforced insulation, $V_{IORM} = 600$ V peak  File (pending)
<b>CQC</b>	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 250 V rms (353 V peak) File (pending)	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 845V rms (1200V peak) working voltage Reinforced insulation at 422V rms (600V peak) File (pending)

## Notes:

<sup>1</sup> In accordance with UL 1577, each  $\pi$ 140U3x/ $\pi$ 141U3x/ $\pi$ 142U3x is proof tested by applying an insulation test voltage  $\geq 3600$  V rms for 1 sec; each  $\pi$ 140U6x/ $\pi$ 141U6x/ $\pi$ 142U6x is proof tested by applying an insulation test voltage  $\geq 7200$  V rms for 1 sec

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each  $\pi$ 140U3x/ $\pi$ 141U3x/ $\pi$ 142U3x is proof tested by applying an insulation test voltage  $\geq 1326$  V peak for 1 sec (partial discharge detection limit = 5 pC); each  $\pi$ 140U6x/ $\pi$ 141U6x/ $\pi$ 142U6x is proof tested by  $\geq 2250$  V peak for 1 sec. The marking branded on the component designates DIN V VDE V 0884-10 approval.

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The marking on packages denotes DIN V VDE V 0884-10 approval.

**Table 12. VDE Insulation Characteristics**

Description	Test Conditions/Comments	Symbol	Characteristic		Unit
			$\pi$ 14xU3x	$\pi$ 14xU6x	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150$ V rms			I to IV	I to IV	
For Rated Mains Voltage $\leq 300$ V rms			I to III	I to III	
For Rated Mains Voltage $\leq 400$ V rms			I to III	I to III	
Climatic Classification			40/105/21	40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum Working Insulation Voltage		$V_{IORM}$	707	1200	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	1326	2250	V peak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	1061	1800	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC		849	1440	V peak
Highest Allowable Overvoltage		$V_{IOTM}$	4200	8500	V peak



Surge Isolation Voltage Basic	Basic insulation, 1.2 $\mu$ s rise time, 50 $\mu$ s, 50% fall time	$V_{IOSM}$	4615	7000	V peak
Surge Isolation Voltage Reinforced	Reinforced insulation, 1.2 $\mu$ s rise time, 50 $\mu$ s, 50% fall time	$V_{IOSM}$			V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)				
Maximum Junction Temperature		$T_S$	150	150	$^{\circ}$ C
Total Power Dissipation at 25 $^{\circ}$ C		$P_S$	1.56	2.78	W
Insulation Resistance at $T_S$	$V_{IO} = 800$ V	$R_S$	$>10^9$	$>10^9$	$\Omega$

$\pi$ 14xU3x

$\pi$ 14xU6x

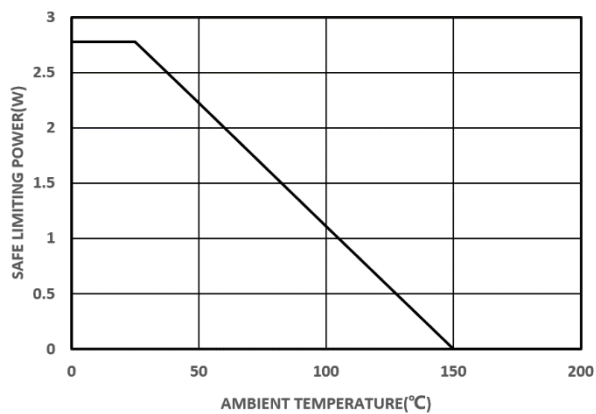
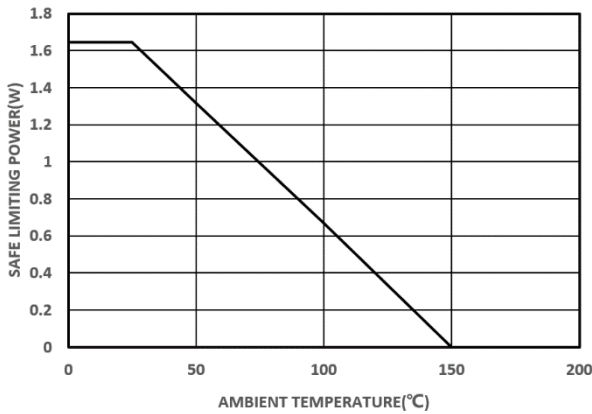


Figure6. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE

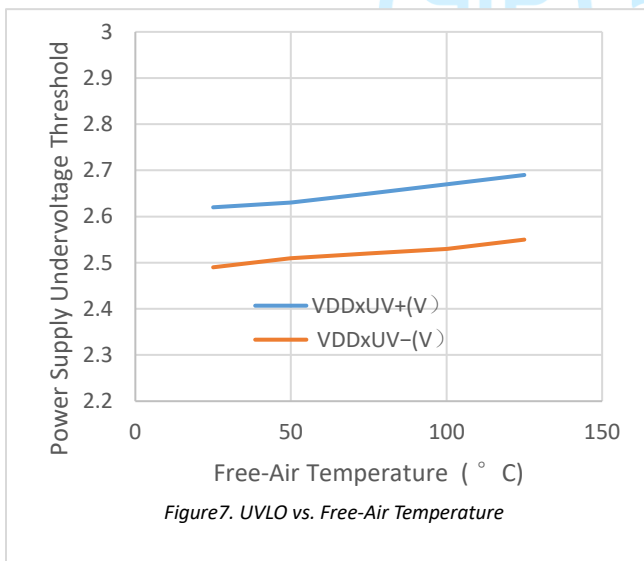


Figure7. UVLO vs. Free-Air Temperature

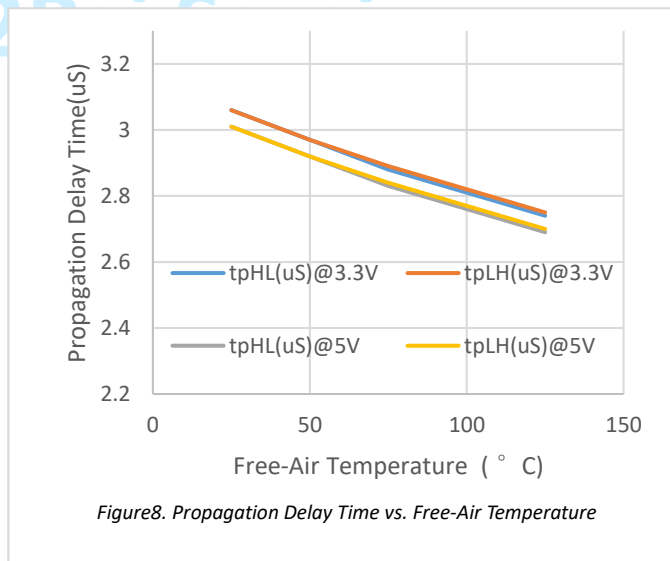


Figure8. Propagation Delay Time vs. Free-Air Temperature

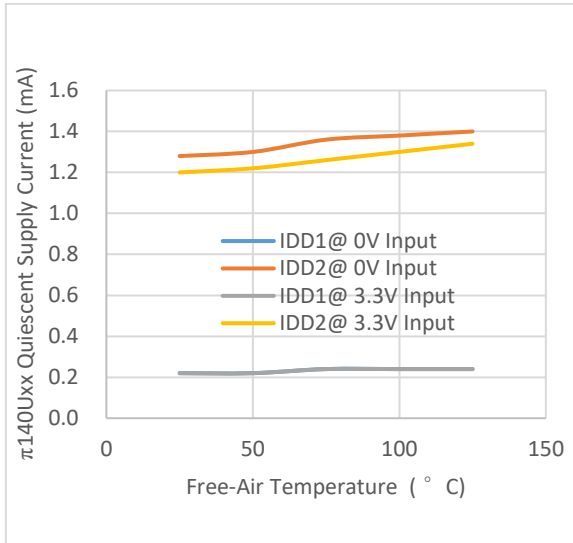


Figure9  $\pi$ 140Uxx Quiescent Supply Current with 3.3V Supply vs.Free-Air Temperature

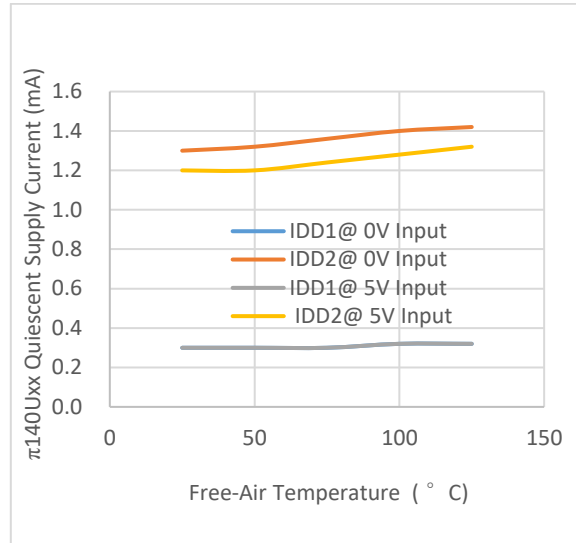


Figure10  $\pi$ 140Uxx Quiescent Supply Current with 5V Supply vs. Free-Air Temperature

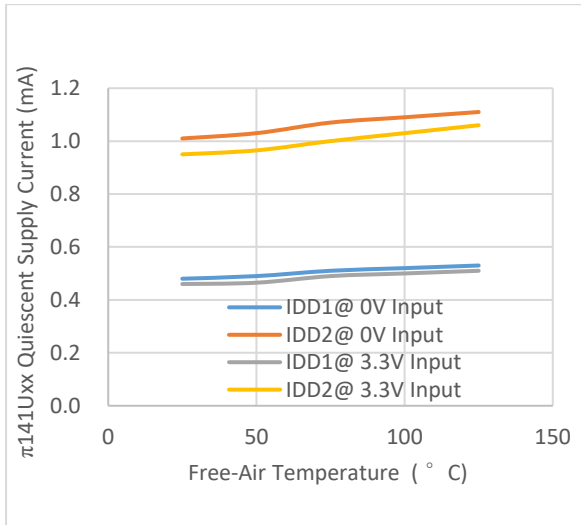


Figure 11  $\pi$ 141Uxx Quiescent Supply Current with 3.3V Supply vs.Free-Air Temperature

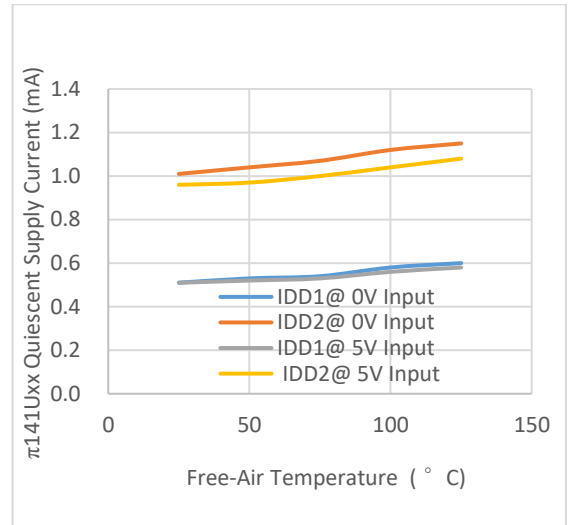


Figure 12  $\pi$ 141Uxx Quiescent Supply Current with 5V Supply vs. Free-Air Temperature

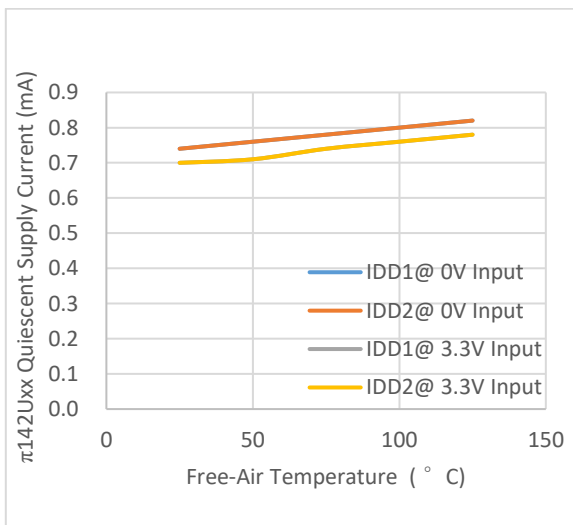


Figure 13  $\pi$ 142Uxx Quiescent Supply Current with 3.3V Supply vs.Free-Air Temperature

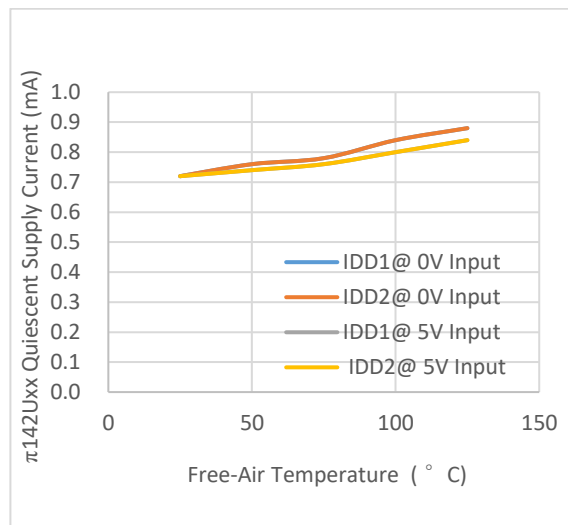


Figure 14  $\pi$ 142Uxx Quiescent Supply Current with 5V Supply vs. Free-Air Temperature

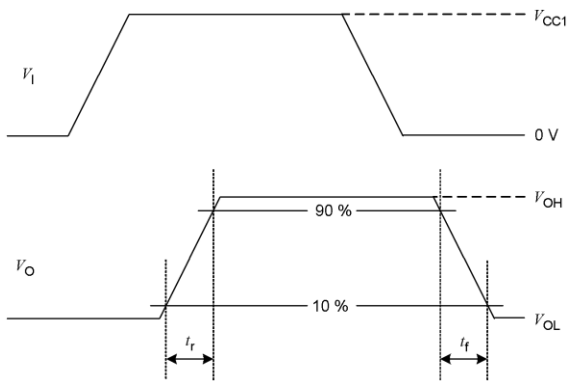


Figure15. Transition time waveform measurement

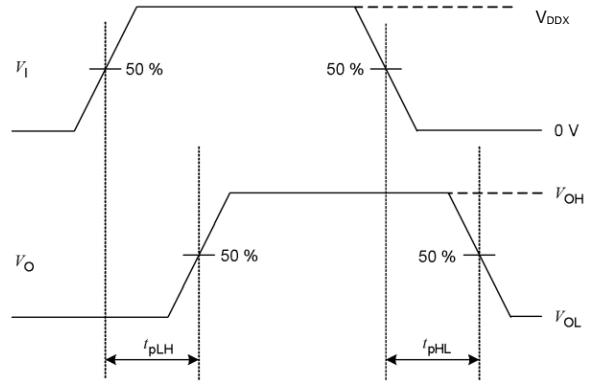


Figure16. Propagation delay time waveform measurement



2Pai Semi

## APPLICATIONS INFORMATION

### OVERVIEW

The  $\pi$ 1xxxx are 2PaiSemi digital isolators product family based on 2PaiSEMI unique **iDivider** technology. Intelligent voltage **Divider** technology (**iDivider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, **iDivider** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using matured standard semiconductor CMOS technology and the innovative **iDivider** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The  $\pi$ 1xxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The  $\pi$ 140Uxx/ $\pi$ 141Uxx/ $\pi$ 142Uxx are the outstanding 150Kbps quad-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic.

The  $\pi$ 140Uxx/ $\pi$ 141Uxx/ $\pi$ 142Uxx have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

### PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between  $V_{DD1}$  and  $GND_1$  and between  $V_{DD2}$  and  $GND_2$ . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1  $\mu$ F and 10  $\mu$ F. To enhance the robustness of a design, the user may also include resistors (50–300  $\Omega$ ) in series with the inputs and outputs if the system is excessively noisy.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

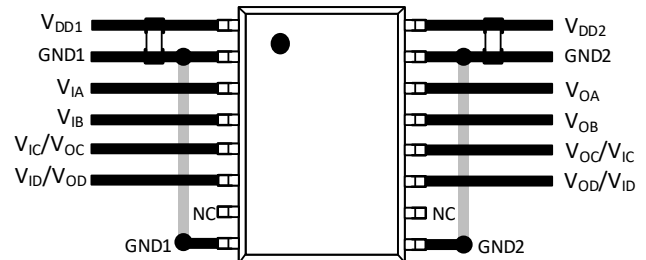


Figure17.Recommended Printed Circuit Board Layout

### CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of  $\pi$ 1xxxx isolator under specified common-mode pulse magnitude ( $V_{CM}$ ) and specified slew rate of the common-mode pulse ( $dV_{CM}/dt$ ) and other specified test or ambient conditions, The common-mode pulse generator ( $G_1$ ) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse ( $V_{CM}$ ) and the maximum common-mode slew rates ( $dV_{CM}/dt$ ) can be applied to  $\pi$ 1xxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground  $GND_1$  and the other side ground  $GND_2$  of  $\pi$ 1xxxx isolator and shall be capable of providing positive transients as well as negative transients.

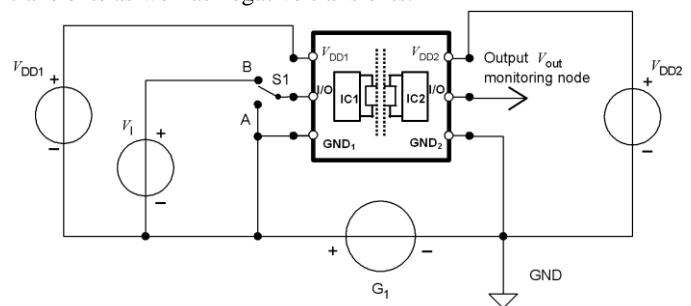


Figure18. Common-mode transient immunity (CMTI) measurement

### OUTLINE DIMENSIONS

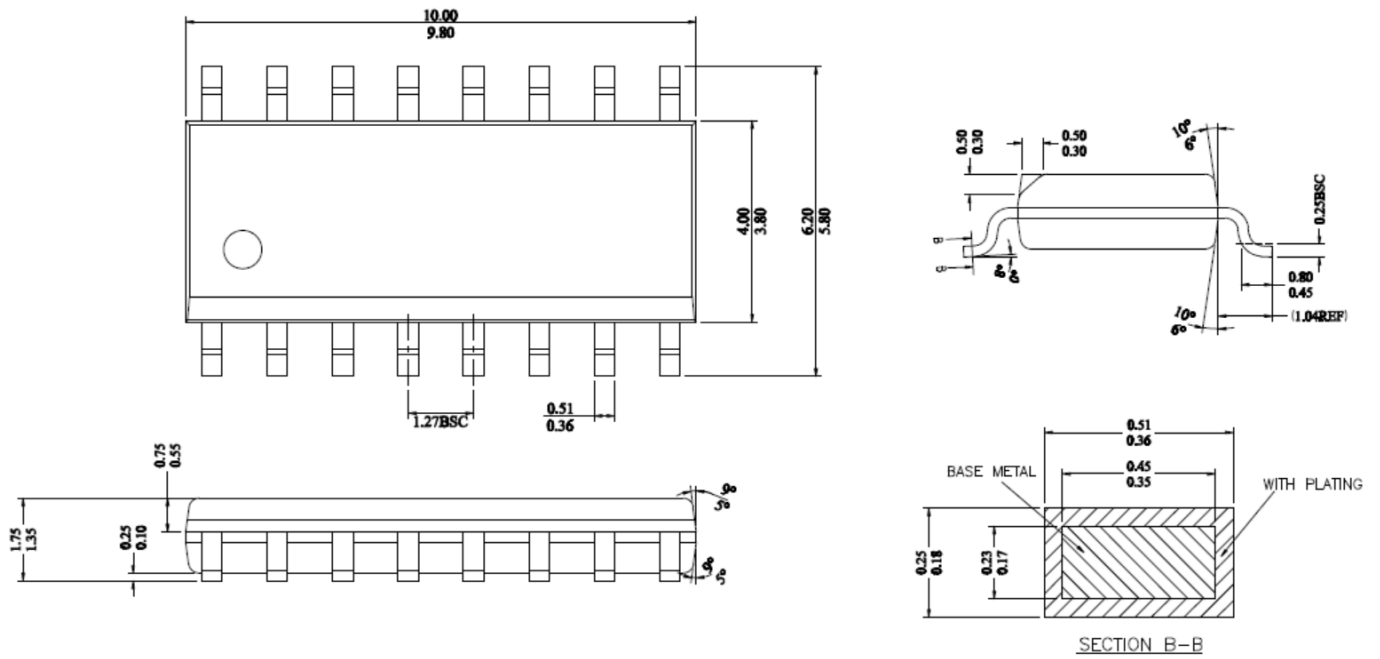


Figure19. 16-Lead Standard Small Outline Package [16-Lead SOIC\_N]

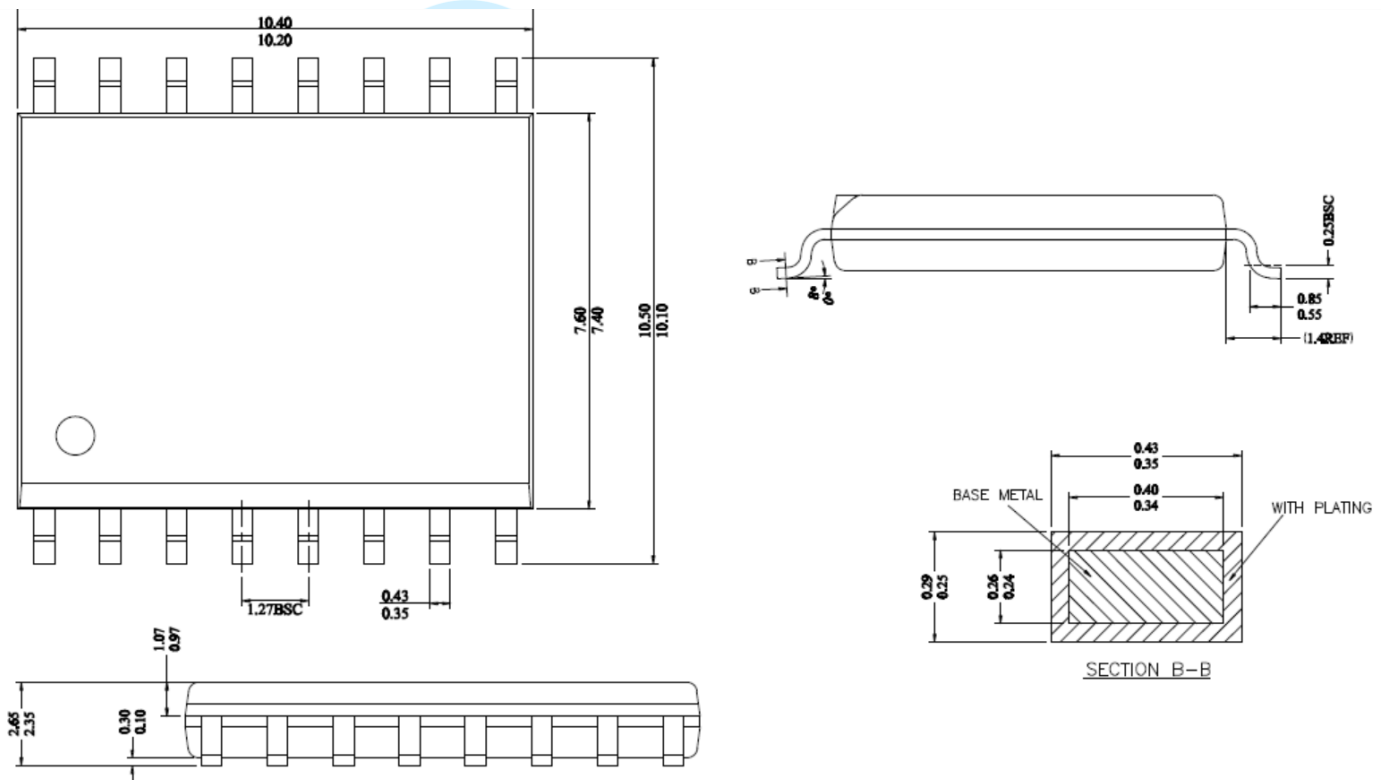
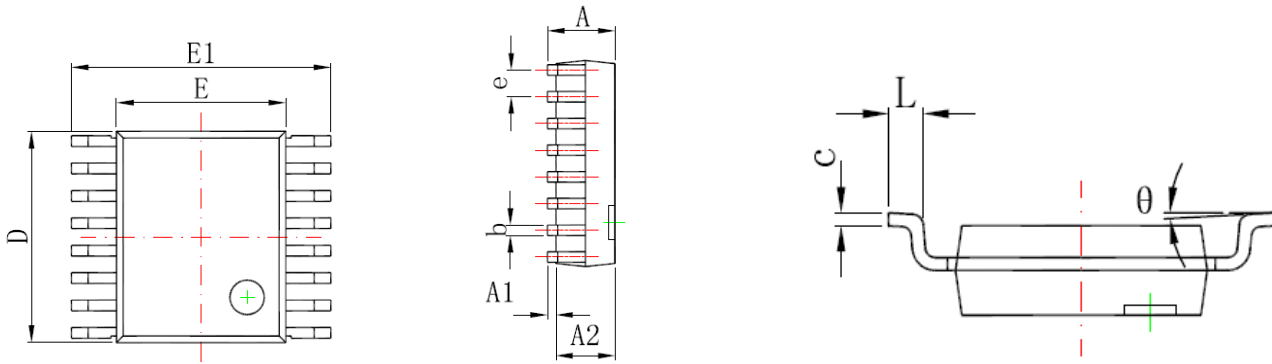


Figure20. 16-Lead Wide Body Outline Package [16-Lead SOIC\_W]

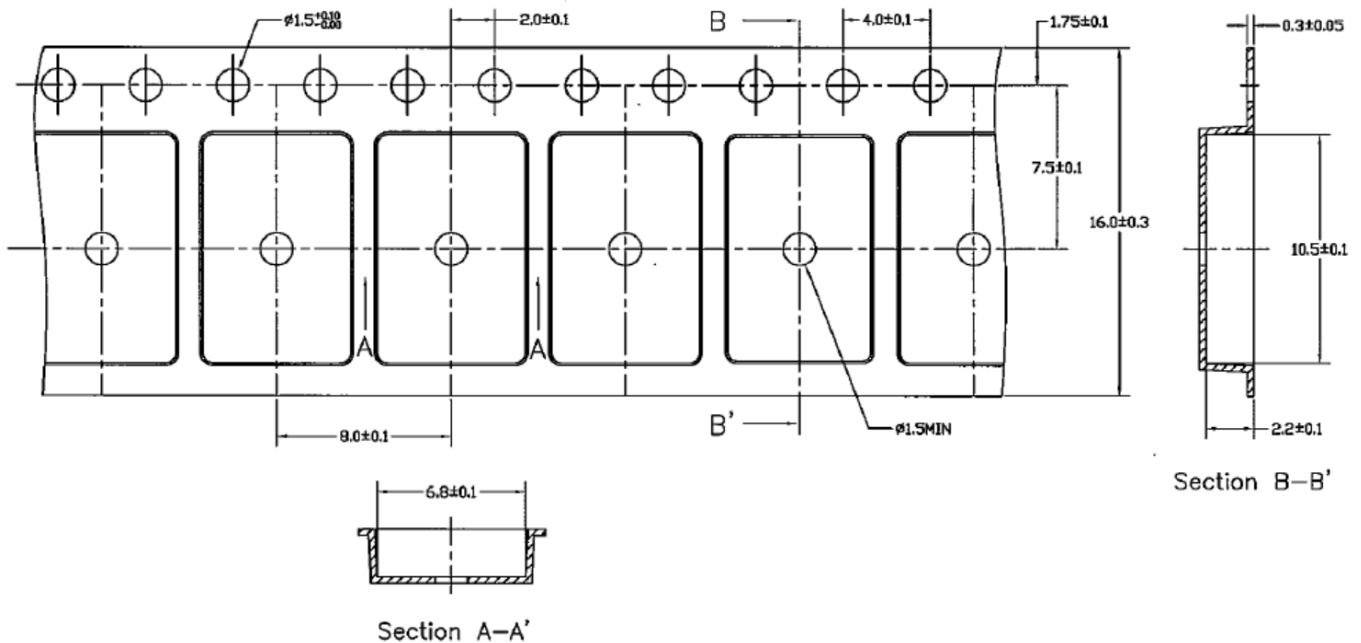


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 (BSC)		0.025 (BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

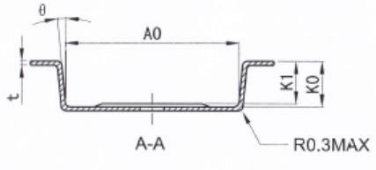
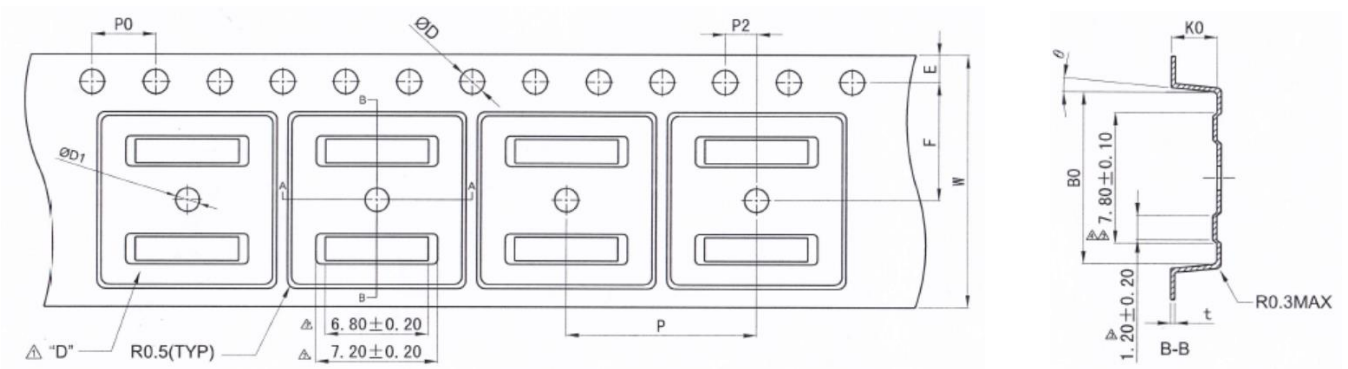
Figure 21. 16-Lead SSOP Outline Package [SSOP16]

## REEL INFORMATION

16-Lead SOIC\_N



16-Lead SOIC\_W

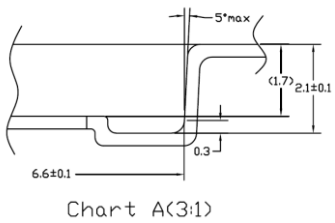
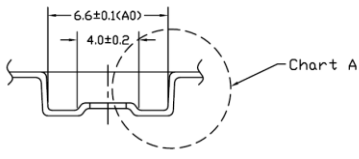
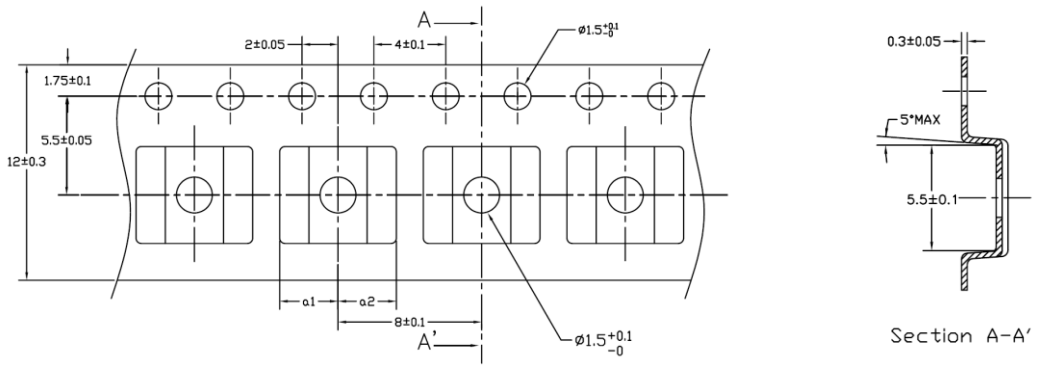


Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP



16-Lead SSOP



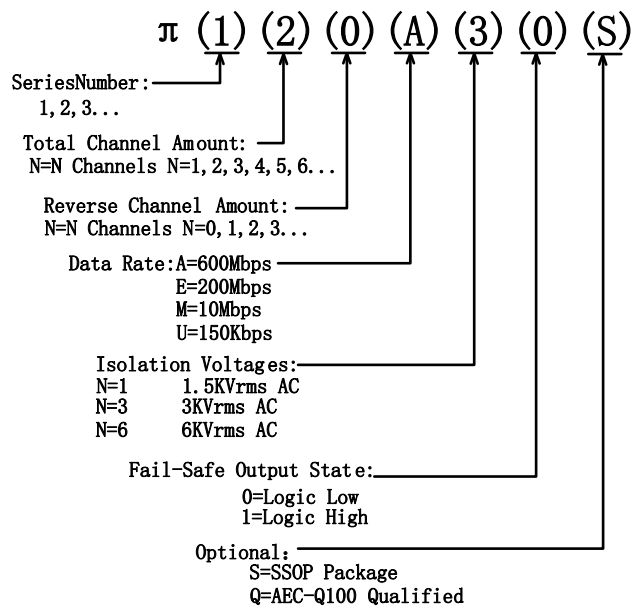
### ORDERING GUIDE

Model Name		Temperature Range	No. of Input s, V <sub>DD1</sub> Side	No. of Inputs , V <sub>DD2</sub> Side	Withstan d Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	Package Option	Quantity
$\pi$ 140U31	Pai140U31	-40°C to +125°C	4	0	3	High	16-Lead SOIC_N	S-16-N	2500 per reel
$\pi$ 140U30	Pai140U30	-40°C to +125°C	4	0	3	Low	16-Lead SOIC_N	S-16-N	2500 per reel
$\pi$ 141U31	Pai141U31	-40°C to +125°C	3	1	3	High	16-Lead SOIC_N	S-16-N	2500 per reel
$\pi$ 141U30	Pai141U30	-40°C to +125°C	3	1	3	Low	16-Lead SOIC_N	S-16-N	2500 per reel
$\pi$ 142U31	Pai142U31	-40°C to +125°C	2	2	3	High	16-Lead SOIC_N	S-16-N	2500 per reel
$\pi$ 142U30	Pai142U30	-40°C to +125°C	2	2	3	Low	16-Lead SOIC_N	S-16-N	2500 per reel
$\pi$ 140U61	Pai140U61	-40°C to +125°C	4	0	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
$\pi$ 140U60	Pai140U60	-40°C to +125°C	4	0	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
$\pi$ 141U61	Pai141U61	-40°C to +125°C	3	1	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
$\pi$ 141U60	Pai141U60	-40°C to +125°C	3	1	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
$\pi$ 142U61	Pai142U61	-40°C to +125°C	2	2	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
$\pi$ 142U60	Pai142U60	-40°C to +125°C	2	2	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
$\pi$ 140U31S	Pai140U31S	-40°C to +125°C	4	0	3	High	16-Lead SSOP	SSOP16	4000 per reel
$\pi$ 140U30S	Pai140U30S	-40°C to +125°C	4	0	3	Low	16-Lead SSOP	SSOP16	4000 per reel
$\pi$ 141U31S	Pai141U31S	-40°C to +125°C	3	1	3	High	16-Lead SSOP	SSOP16	4000 per reel
$\pi$ 141U30S	Pai141U30S	-40°C to +125°C	3	1	3	Low	16-Lead SSOP	SSOP16	4000 per reel
$\pi$ 142U31S	Pai142U31S	-40°C to +125°C	2	2	3	High	16-Lead SSOP	SSOP16	4000 per reel
$\pi$ 142U30S	Pai142U30S	-40°C to +125°C	2	2	3	Low	16-Lead SSOP	SSOP16	4000 per reel

Notes:

<sup>1</sup>  $\pi$ 14xxxxQ special for Auto, qualified for AEC-Q100

### PART NUMBER NAMED RULE



Notes:

Pai14xxxx is equals to  $\pi$ 14xxxx in the customer BOM



## REVISION HISTORY

Revision	Updated	Date	Page	Change Record
1	Victory	2018/09/20	All	Initial version
2	Victory	2018/11/28	P1,P11	Changed $C_{IN}$ , $C_{OUT}$ in Figure2 from 0.1uF to 1uF. Changed the recommended bypass capacitor value from between 0.1 $\mu$ F and 1 $\mu$ F to between 0.1 $\mu$ F and 10 $\mu$ F.
3	Devin	2019/09/08	P1,P7,P11 ,P13,P14, P15	P1: Changed the address from 'Room 19307, Building 8, No.498, GuoShouJing Road' to 'Room 308-309, No.22, Boxia Road'; Changed '(W)SOIC package' to 'SOIC_N, SOIC_W and SSOP package'; Add <b>iDivider</b> technology description in General Description. Changed $C_{IN}$ , $C_{OUT}$ in Figure2 from 1uF to 0.1uF. P7: Add 'and SSOP16 Pin 1-Pin8' and 'and SSOP16 Pin 9-Pin16' in note 1. P11: Add <b>iDivider</b> technology description in overview. P13: Add Figure21. 16-Lead SSOP Outline Package drawing P14: Add 16-Lead SSOP Reel drawing; Updated 16-Lead SOIC_W reel drawing. P15: Add character 'S' and 'Q' in part number named rule; Changed the SOIC_W quantity from '1000 per reel' to '1500 per reel'; Add ' $\pi$ 140U31S、 $\pi$ 140U30S、 $\pi$ 141U31S、 $\pi$ 141U30S、 $\pi$ 142U31S、 $\pi$ 142U30S' in ordering guide

