

## 600V Half Bridge Driver

### PRODUCT SUMMARY

- $V_{\text{OFFSET}}$  600 V max.
- $I_{\text{O+/- (min)}}$  130 mA/270 mA
- $V_{\text{OUT}}$  10 V - 20 V
- $t_{\text{on/off (typ.)}}$  160 ns/220 ns
- **Delay Matching** 60 ns

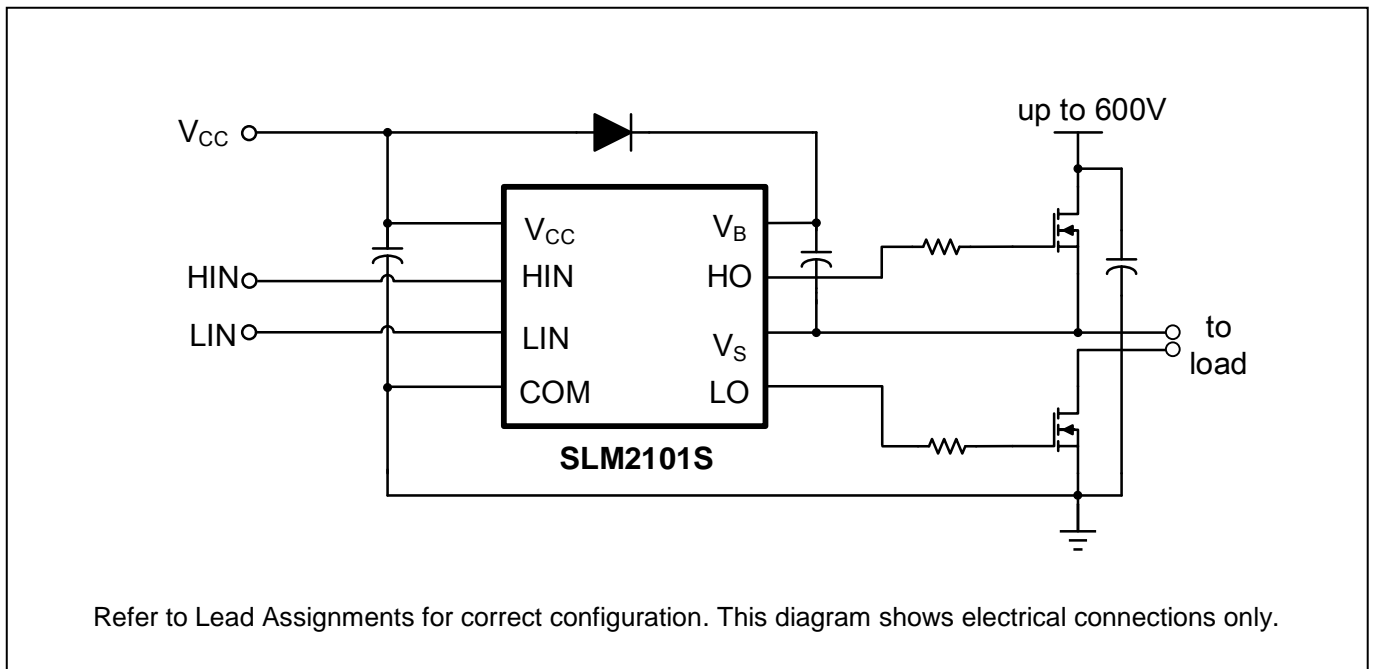
### GENERAL DESCRIPTION

The SLM2101S is a high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

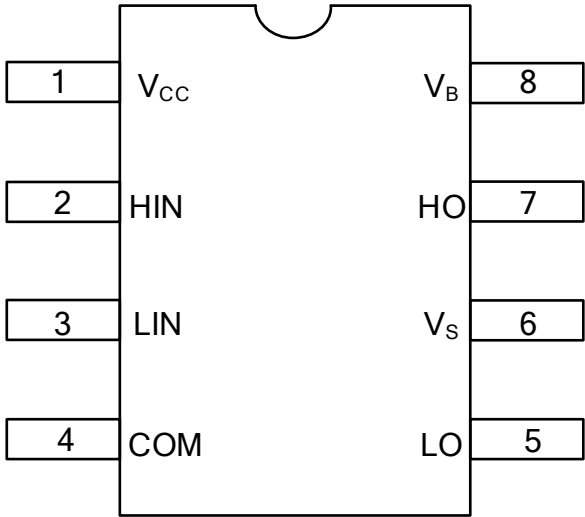
### FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOP8 package

### TYPICAL APPLICATION CIRCUIT



**PIN CONFIGURATION**

Package	Pin Configuration (Top View)
SOP8	

**PIN DESCRIPTION**

No.	Pin	Description
1	V <sub>CC</sub>	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V <sub>S</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>B</sub>	High-side floating supply

**ORDERING INFORMATION**

INDUSTRIAL RANGE: -40°C TO +125°C

Order Part No.	Package	QTY
SLM2101SCA-13GTR	SOP8, Pb-Free	2500/Reel



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating absolute voltage	-0.3	625	V
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	-0.3	25	
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input voltage (HIN & LIN)	-0.3	V <sub>CC</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	---	50	V/ns
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	---	0.625	W
θ <sub>JA</sub>	Thermal resistance, junction to ambient	---	200	°C/W
T <sub>J</sub>	Junction temperature	---	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	---	300	

**Note:** Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage		600	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (HIN & LIN)	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	- 40	125	°C

**Note:** The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at a 15 V differential.

**DYNAMIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ ,  $C_L = 1000\text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0\text{ V}$	---	160	220	ns
$t_{off}$	Turn-off propagation delay	$V_S = 0\text{ V}$	---	220	280	
$t_r$	Turn-on rise time		---	70	170	
$t_f$	Turn-off fall time		---	35	90	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

**STATIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "1" input voltage	$V_{CC} = 10\text{ V to }20\text{ V}$	2.5	---	---	V
$V_{IL}$	Logic "0" input voltage		---	---	0.8	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2\text{ mA}$	---	0.05	0.2	
$V_{OL}$	Low level output voltage, $V_O$		---	0.02	0.1	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN} = 0\text{ V}$	---	60	78	
$I_{QCC}$	Quiescent $V_{CC}$ supply current		---	230	280	
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = 5\text{ V}$	---	8	15	
$I_{IN-}$	Logic "0" input bias current	$V_{IN} = 0\text{ V}$	---	---	5	
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ & $V_{BS}$ supply undervoltage positive going threshold		8	8.9	9.8	V
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ & $V_{BS}$ supply undervoltage negative going threshold		7.4	8.2	9	
$I_{O+}$	Output high short circuit pulsed current	$V_O = 15\text{ V}$ , $V_{IN} = \text{Logic "1"}$ , $PW \leq 10\ \mu\text{s}$	130	290		mA
$I_{O-}$	Output low short circuit pulsed current	$V_O = 0\text{ V}$ , $V_{IN} = \text{Logic "0"}$ , $PW \leq 10\ \mu\text{s}$	270	600		

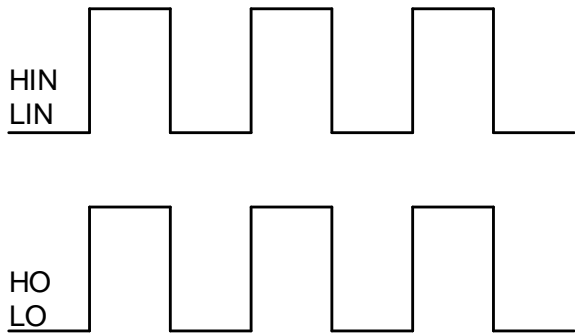


Figure 1. Input/Output Timing Diagram

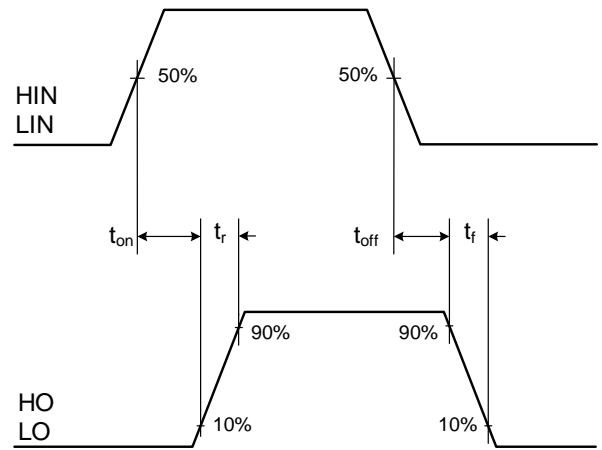


Figure 2. Switching Time Waveform

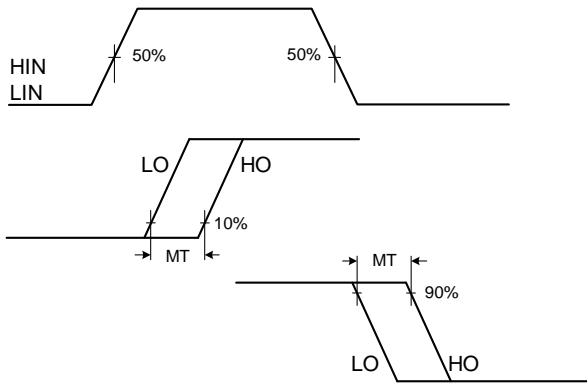


Figure 3. Delay Matching Waveform

**TYPICAL PERFORMANCE CHARACTERISTICS**

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V, and  $T_A$  = 25°C unless otherwise specified.

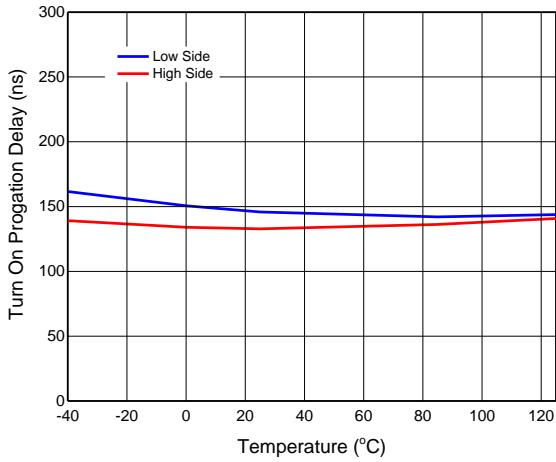


Figure 4. Turn On Delay vs. Temperature

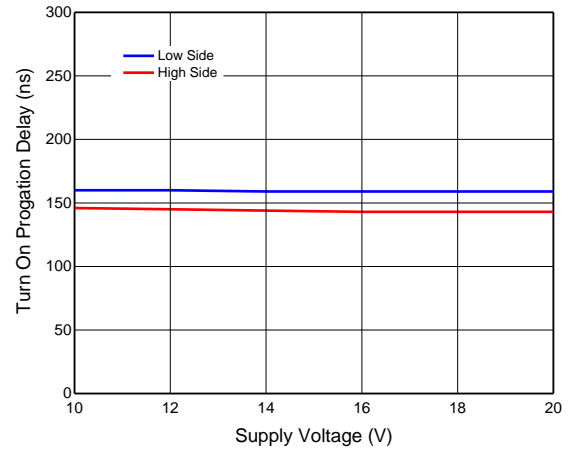


Figure 5. Turn On Delay vs. Supply Voltage

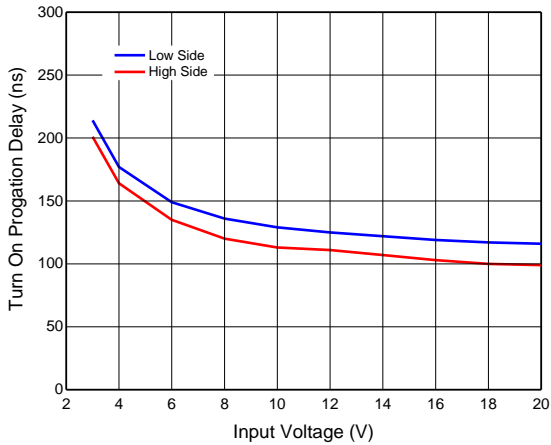


Figure 6. Turn On Delay vs. Input Voltage

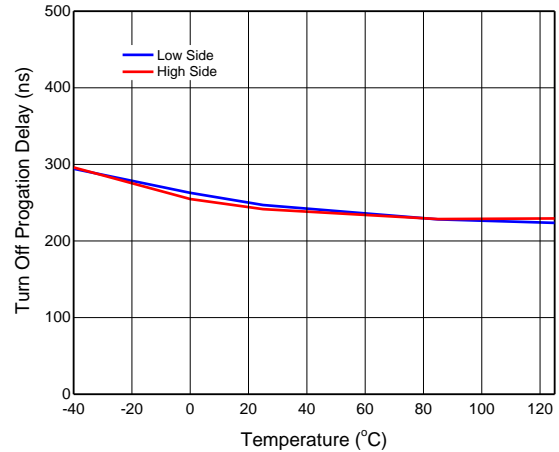


Figure 7. Turn Off Delay vs. Temperature

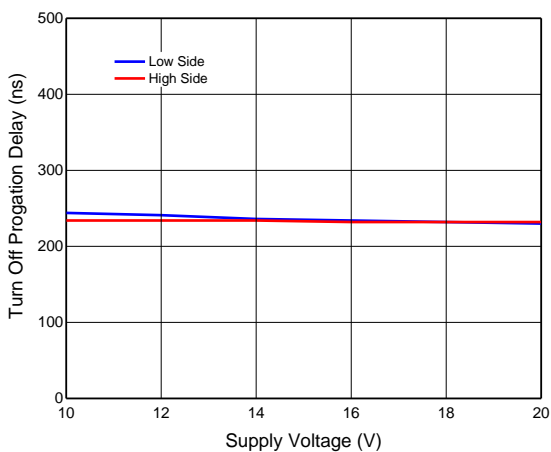


Figure 8. Turn Off Delay vs. Supply Voltage

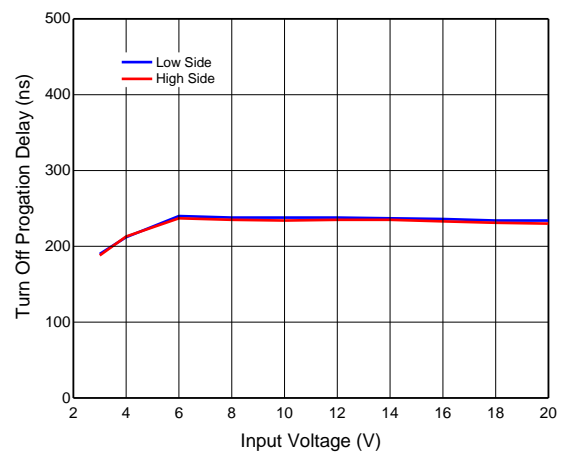


Figure 9. Turn Off Delay vs. Input Voltage

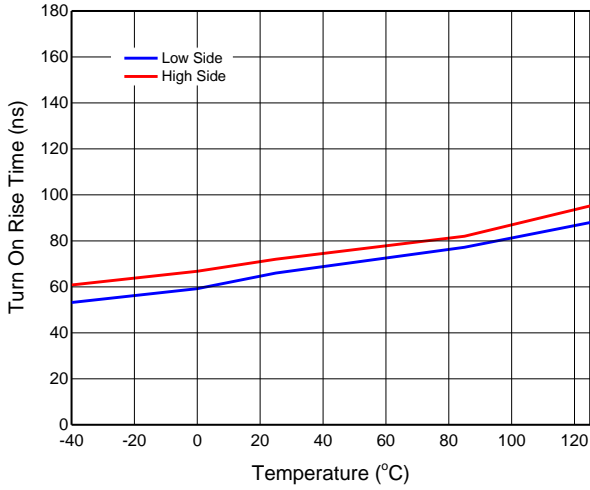


Figure 10. Turn On Rise Time vs. Temperature

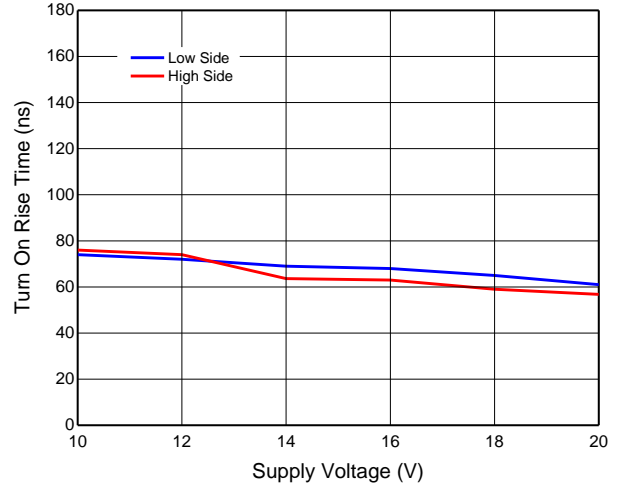


Figure 11. Turn On Rise Time vs. Supply Voltage

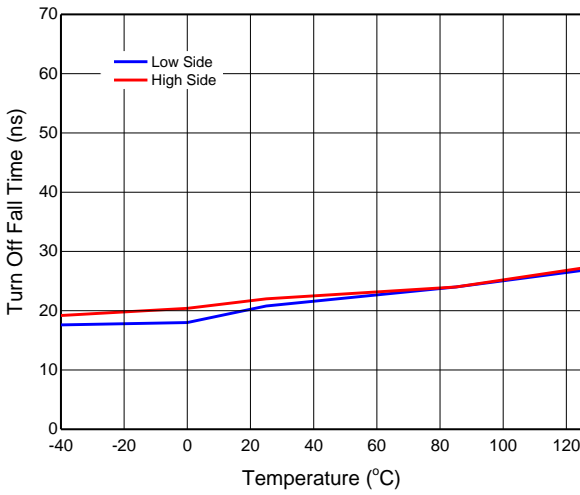


Figure 12. Turn Off Fall Time vs. Temperature

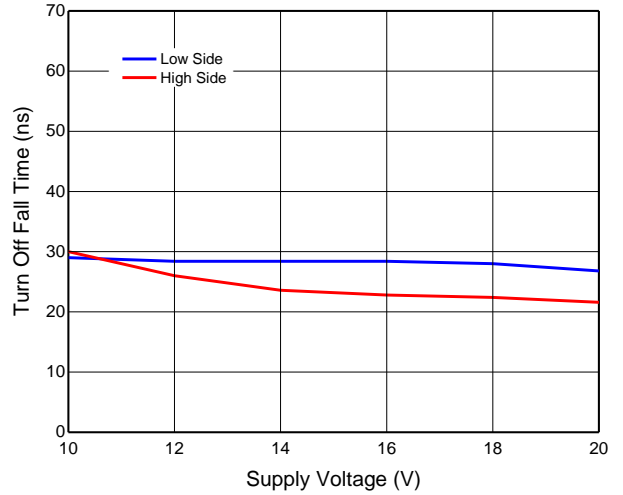


Figure 13. Turn Off Fall Time vs. Supply Voltage

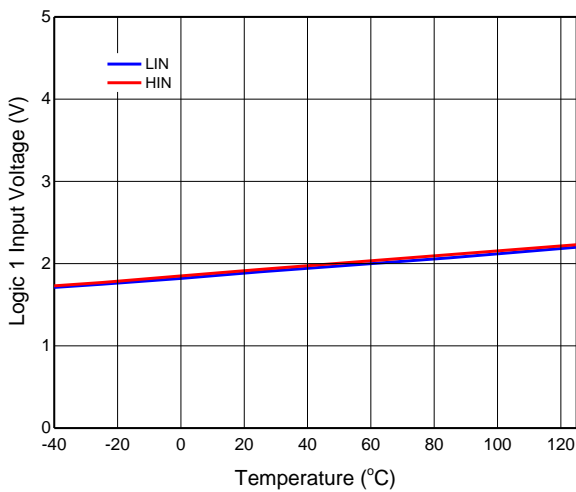


Figure 14. Logic "1" Input Voltage vs. Temperature

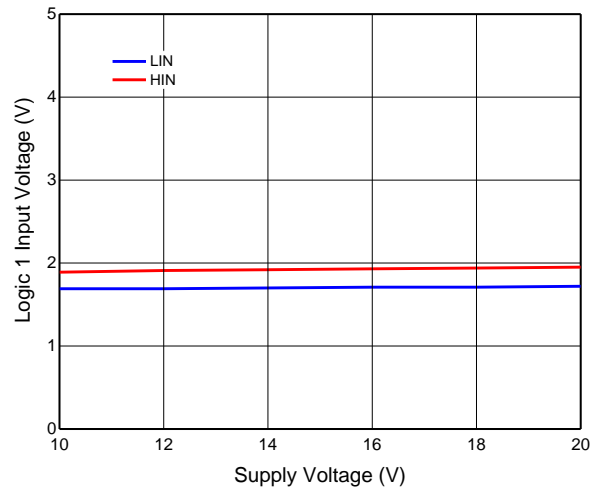


Figure 15. Logic "1" Input Voltage vs. Supply Voltage



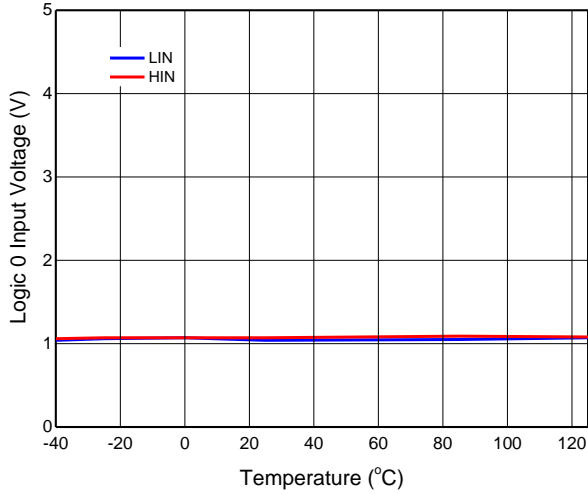


Figure 16. Logic "0" Input Voltage vs. Temperature

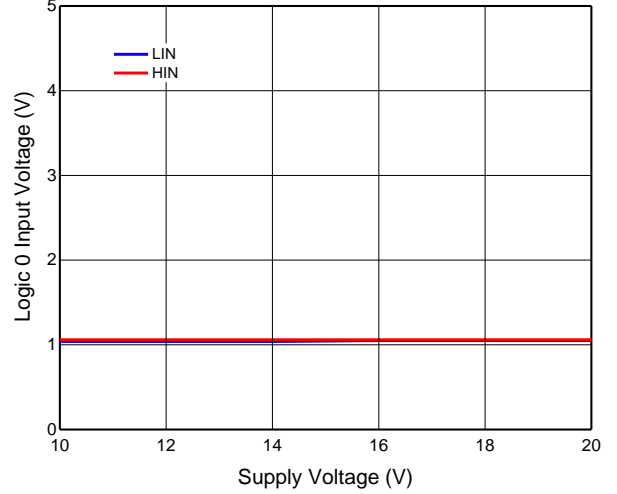


Figure 17. Logic "0" Input Voltage vs. Supply Voltage

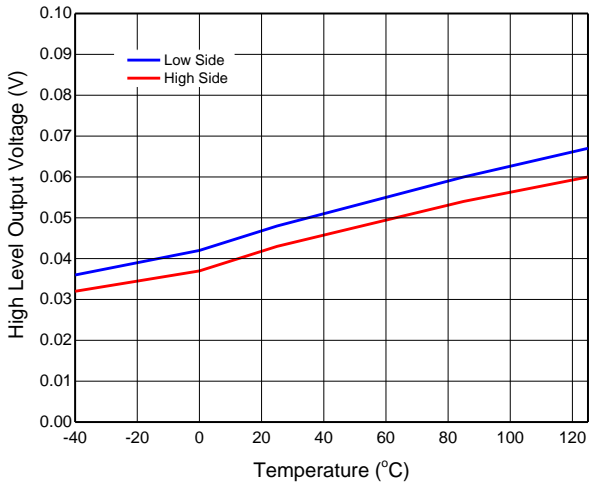


Figure 18. High Level Output vs. Temperature

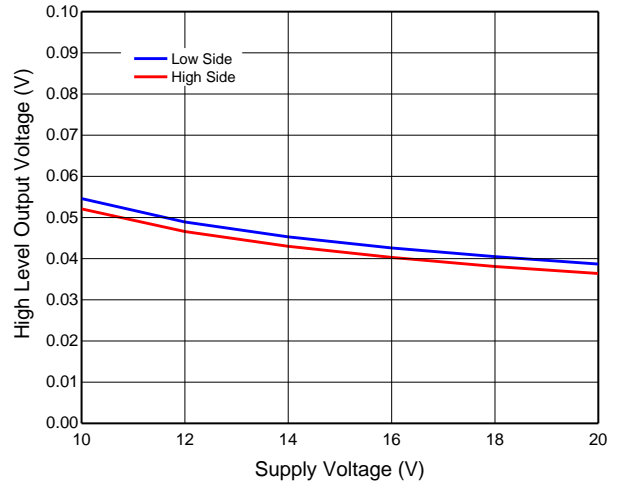


Figure 19. High Level Output vs. Supply Voltage

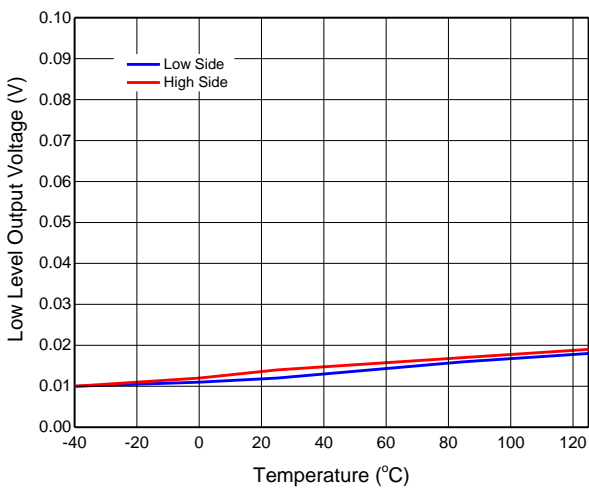


Figure 20. Low Level Output vs. Temperature

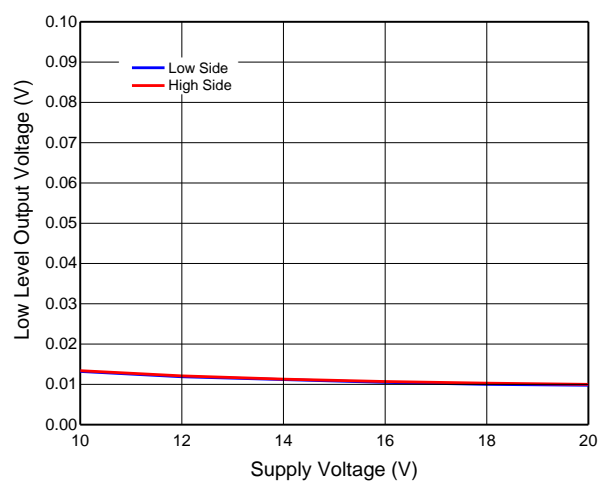


Figure 21. Low Level Output vs. Supply Voltage

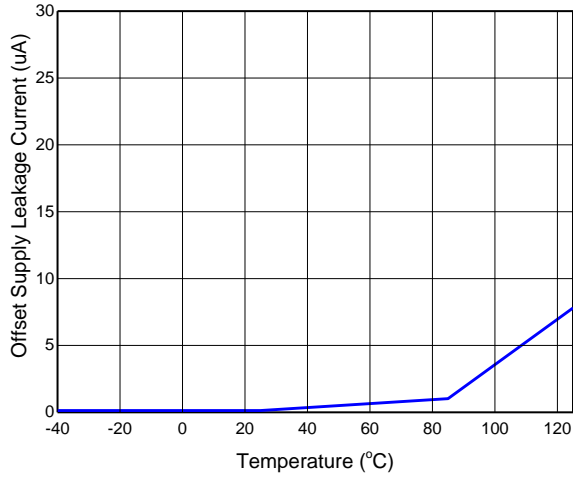


Figure 22. Offset Supply Current vs. Temperature

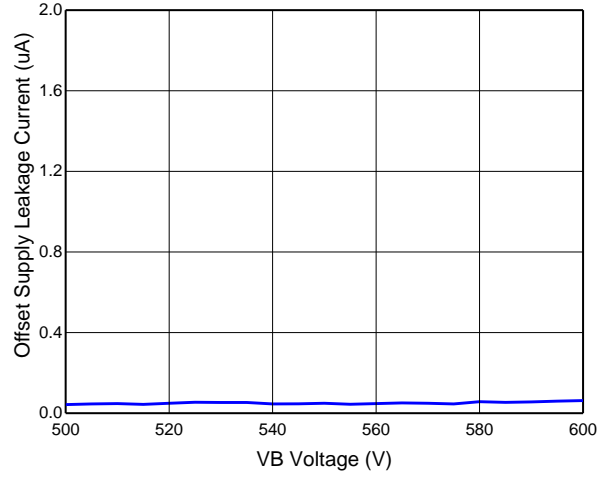


Figure 23. Offset Supply Current vs. VB Voltage

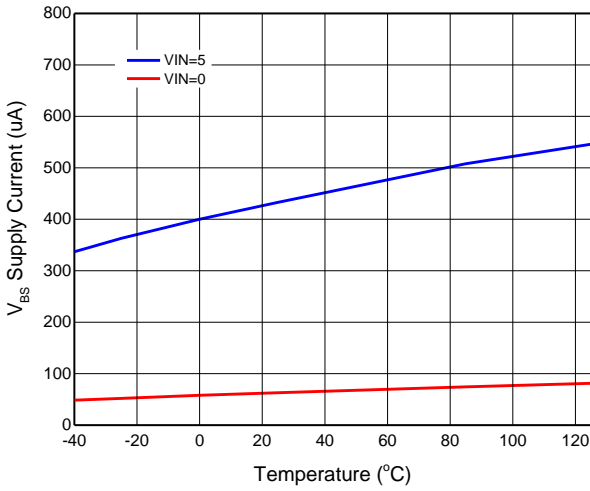


Figure 24. V<sub>BS</sub> Supply Current vs. Temperature

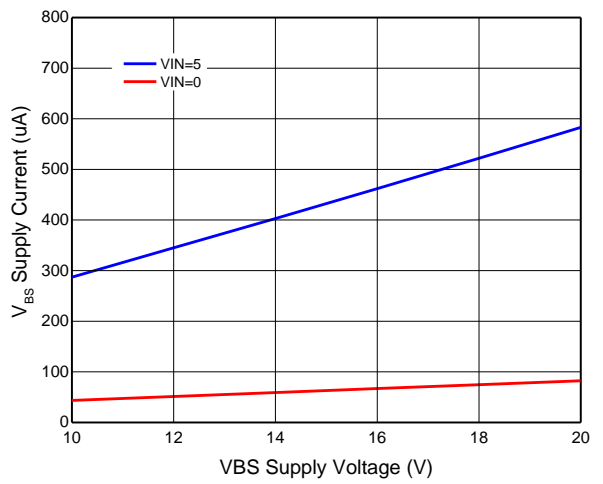


Figure 25. V<sub>BS</sub> Supply Current vs. Supply Voltage

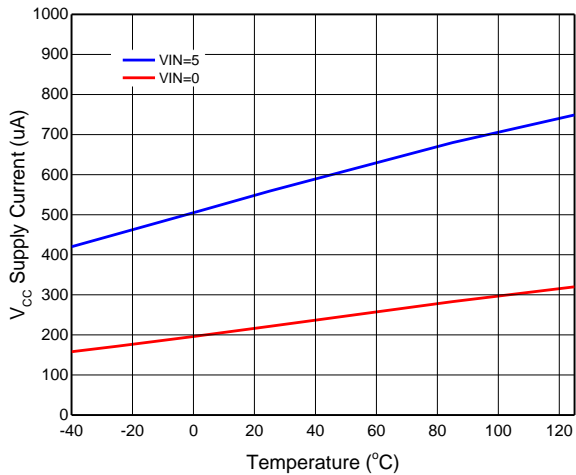


Figure 26. V<sub>CC</sub> Supply Current vs. Temperature

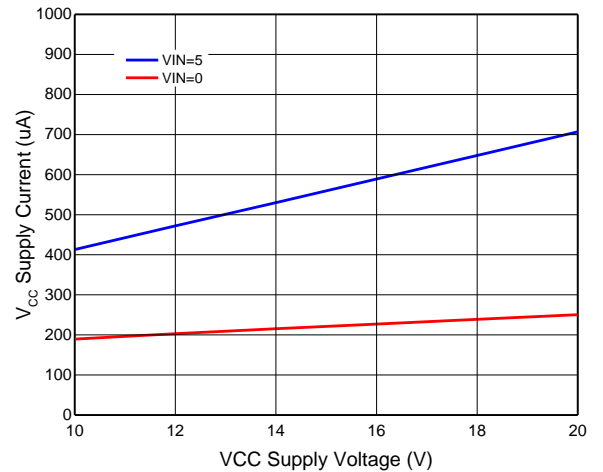


Figure 27. V<sub>CC</sub> Supply Current vs. Supply Voltage

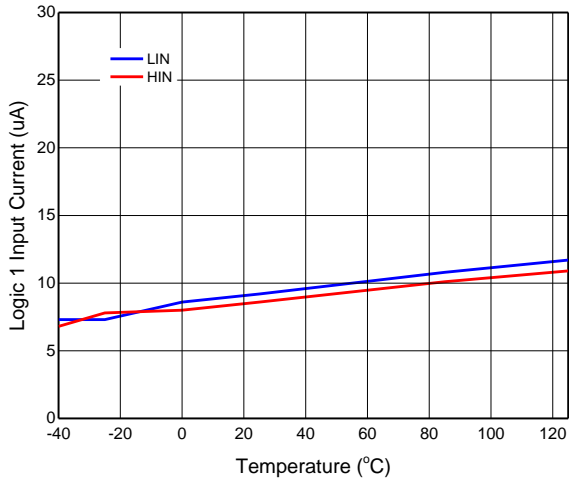


Figure 28. Logic "1" Input Current vs. Temperature

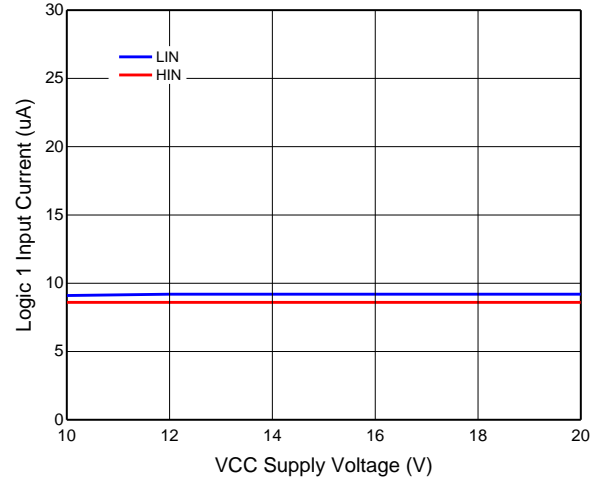


Figure 29. Logic "1" Input Current vs. Supply Voltage

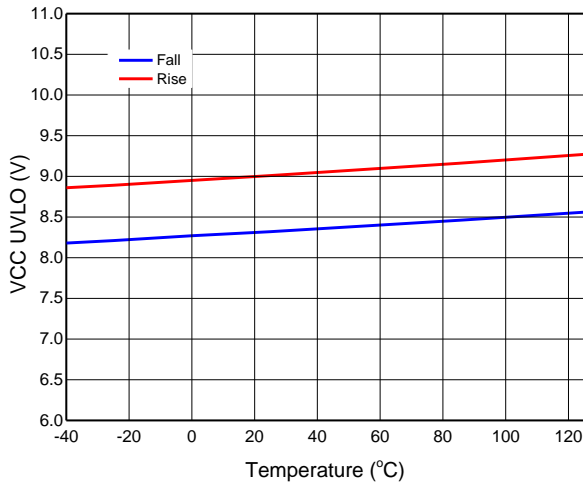


Figure 30. VCC UVLO Threshold vs. Temperature

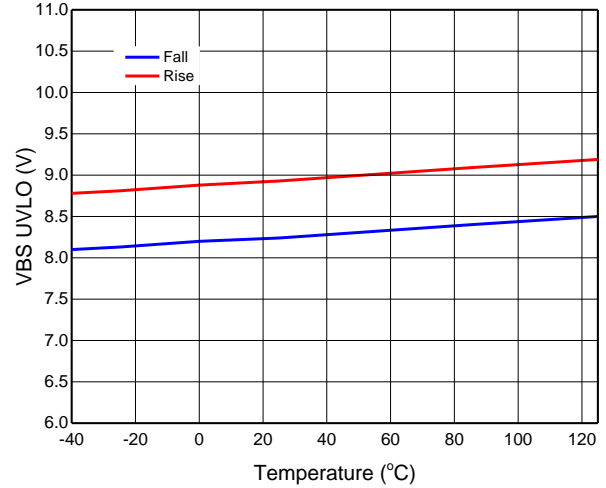


Figure 31. VBS UVLO Threshold vs. Temperature

**PACKAGE CASE OUTLINES**

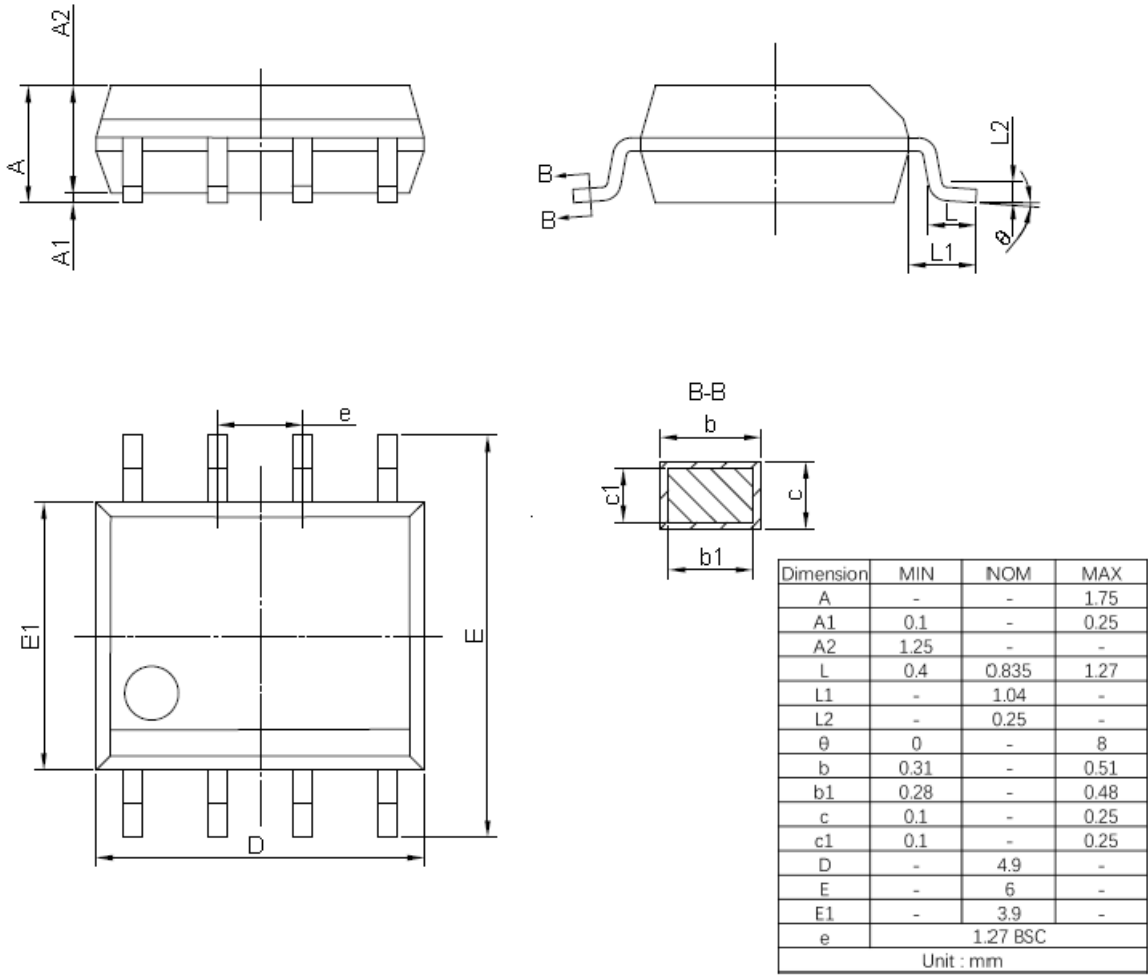


Figure 32. SOP8 Outline Dimensions

**REVISION HISTORY**

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
<b>Rev 1.0 datasheet, 2019-8-29</b>	
Whole document	new company logo released
Page 1	Removed "Fig 1. "
<b>Rev 1.1 datasheet, 2019-10-21</b>	
Page 1	Change "high side and low side driver" to "half-bridge driver"
Page 1	Change "independent" to "dependent"
<b>Rev 1.2 datasheet, 2020-5-15</b>	
Page 5	I <sub>QBS</sub> and I <sub>QCC</sub> change
<b>Rev 1.3 datasheet, 2020-9-23</b>	
Page 5	V <sub>OH</sub> and V <sub>OL</sub> test condition change I <sub>IN+</sub> parameter change
<b>Rev 1.4 datasheet, 2021-10-29</b>	
Whole datasheet	Update the Logo and format
Page 1	Remove the DIP 8 package
Page 2	Remove the SLM2101SCA-GT, SLM2101SDA-GT in the ordering information.
Page 5	Update the V <sub>OH</sub> , V <sub>OL</sub> and I <sub>QCC</sub> in the static electrical characteristics table
<b>Rev 1.5 datasheet, 2022-12-19</b>	
Whole datasheet	Change package name from SOIC-8 to SOP8 and update the package case outlines