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NOTICE

1. Advance agreement will be needed before changing any contents of the specification herein.
2. Provided that the information herein is subject to change, only revised pages shall be reissued.
3. When the product described herein includes Regulated Products subject to The Wassenaar Arrangement etc., they may not be exported without authorization from the appropriate governmental authorities.
4. The contents of this specification including all figures and illustrations are proprietary information (copyright or know-how) of Seiko Instruments Inc. It is strictly prohibited to copy all or part of these specifications to third parties without permission.
5. The products described herein are not designed to be radiation-proof.
6. In the case that the products described herein are used as part of any devices or equipment which might influence any one of the human body, human life and property, such as physical exercise equipment, medical equipment or vehicles, please let us know that.

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Contents

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Quality Specifications

This book of specifications applies to the product with which Seiko Instruments Inc.(hereinafter referred to as SII) supplies the customer. This book of specifications specifies product standard of the supplied IC and items regarding quality assurance and others.

1. Quality standard

1 - 1. Test specifications for reliability recognition.

Test specifications are shown in an attached "RELIABILITY TEST DATA".

1 - 2. Condition

SII assures above mentioned LTFR in which units are assembled in standard package of SII. The customer may evaluate the units based upon customer's criteria and if any discrepancy comes up, both parties should discuss the solution.

2. Disposition of disqualified lots and defective products.

2 - 1. Disposition of disqualified lots.

If any lot is judged to be disqualified and both parties agree that the defect shall be attributed to the IC of SII after examining samples and data, it is a rule that the customer returns the troubled lot to SII and SII supplies substitutes to the customer without delay. In case of abnormality such as occurrence of disqualifications in subsequent lots at the customer, both parties decide how to handle the problem after discussing the matter without any delay.

A lot also must consist of ICs from the same wafer or the wafers produced at the same time under the same condition. A lot in which the number of parts is short for packing can be combined with another lot.

2 - 2. Analysis and disposition of defective products .

SII carries out failure analysis of defectives by request, and clarifies the cause of the defect and notifies the customer of the result. Failure analysis after assembling ICs on a circuit board shall be performed by the customer in principle. If the analysis makes it evident that the responsibility is attributed to SII, SII plans a corrective action , in which supplying substitute is the maximum compensation, SII puts this into practice without delay.

2 - 3. Adjustment of measurement system.

In case that the specifications and electrical characteristics of the IC are different and it becomes necessary to adjust the measurement system of the customer and SII, following three steps are performed.

1) SII supplies the customer the minimum n=10 pcs of ICs with data.

2) The customer performs the measurements of the same characteristic and puts the data in shape and returns the ICs to SII with the data.
3) Both the parties adjust the measurement system based upon the result of 1) and 2). Both the parties discuss and decide the details.

3. Change of Specification

In case of changing the specifications upon requests of both parties a prior written form is required in principle. Depending upon the contents of the change both parties discuss and decide how to proceed. When it is presumed that the change of design, material, or process may affect the characteristics of the IC, SII shall notify the customer of the change and send the quality assurance data and samples, etc., to get the customer's prior consent. If a trouble occurs regarding the items not referred to in this book, both parties shall discuss and decide.

4. Period of quality assurance

Period of quality assurance shall extend for one year hereafter every time the customer accepts the products delivered by SII after the contract of these specifications.

5. Electrostatic breakdown protection

The product has a built-in input protection circuit to prevent damage to the device under most conditions. However in order to protect the ICs from breakdown due to high static electricity or high voltage which exceed the performance of the circuit, the following procedures are recommended to avoid accidental circuit damage.

1) Soldering irons, testing equipment, machines and tools should be at the same reference (ground) potential as the devices.
2) Unit should not be inserted into a socket or taken out from a socket while power is applied.
3) Any signal voltage should not be applied to input terminals while power is off.
4) All unused input terminals should be tied to ground terminal or power supply terminal unless they are pull-up or pull-down.
5) High voltage which exceeds power supply voltage should not be applied to any terminal.

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6. Product Liability

1) SII agrees to indemnify and hold Buyer harmless from any claim and suit (hereinafter referred to as Claims) asserted by any third party against Buyer alleging that Buyer's products into which the Product supplied by SII to Buyer has been incorporated caused bodily injury to or death of any person or property or any other damage, provided that it shall be clearly shown by Buyer that;

a) the Claims were caused solely and exclusively by a defect in the Product;

and

b) the Claims would have not been caused unless the Product had been incorporated into the Buyer's products.

Notwithstanding anything to the contrary contained in this Section, SII's liability to Buyer in connection with the Claims shall be limited to the selling price of the Product from SII to Buyer.

2) Notwithstanding the foregoing, Buyer and SII may jointly resolve the Claims by mutual agreement.

3) SII and Buyer agree to endeavor to determine matters not provided in this Section and resolve any dispute or difference among them arising out of this Section by discussions to be held in good faith.

7. Others

In the event that any trouble which is not referred to in this book of specifications should occur and when it becomes necessary to revise the standards, one party is requested to notify the other and both parties discuss to revise and carry it out.

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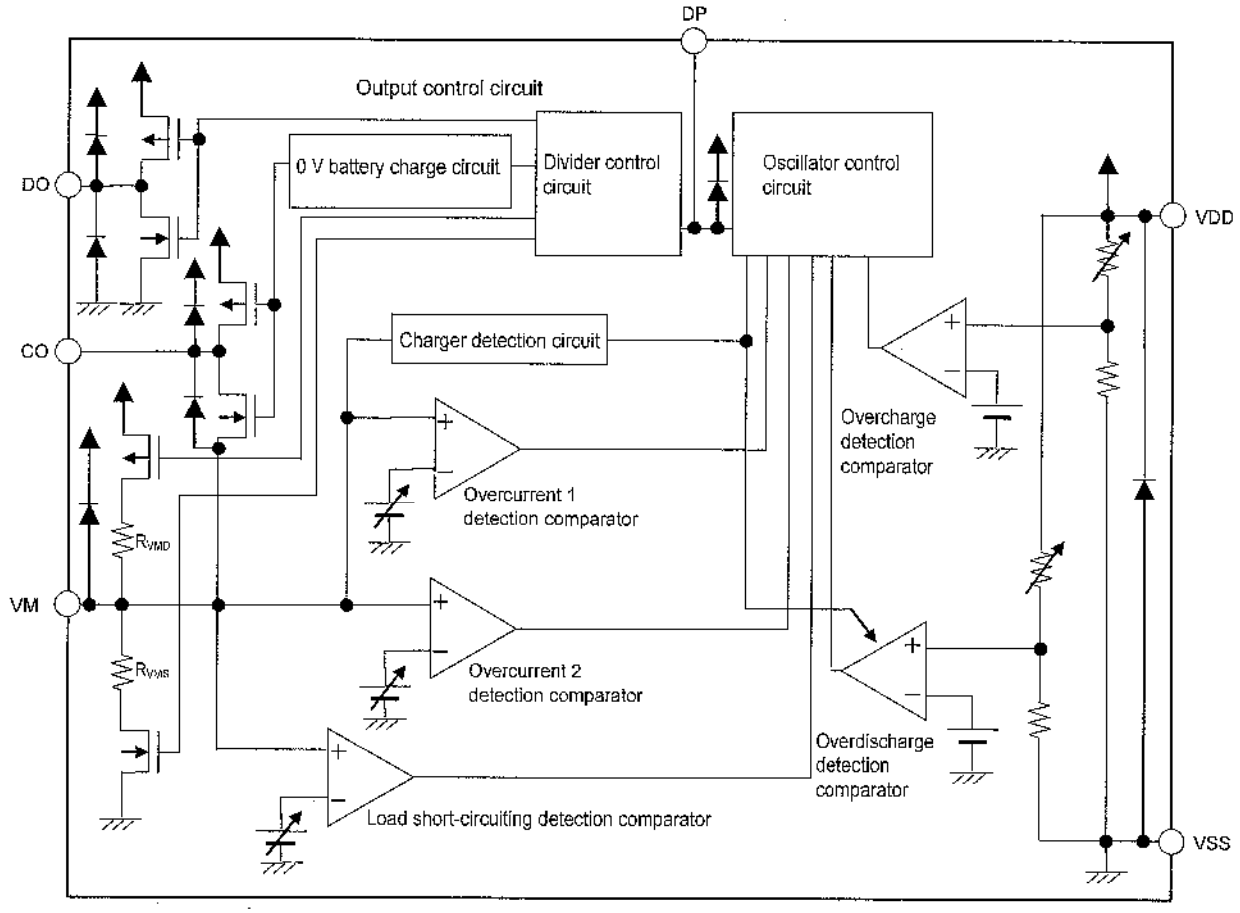
S-8261ACVMD-G4VT2U
Product Standards

This book of Product Standards consists of the following items.

1. Block Diagram



Remark All the diodes shown in the figure are parasitic diodes.

Figure 1

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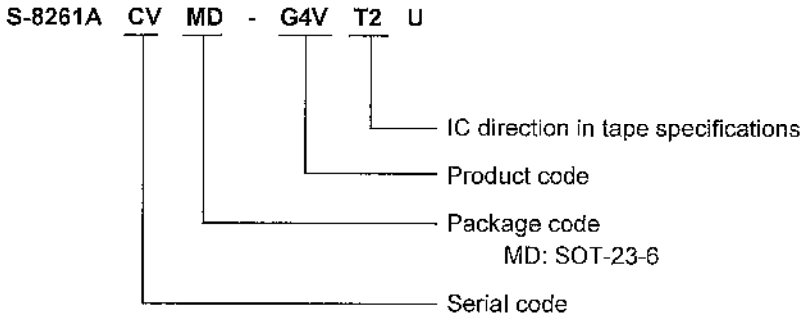
2. Product Name Structure



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3. Pin Configuration

SOT-23-6
Top view

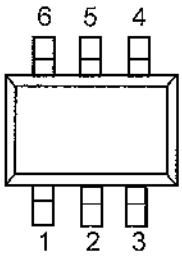

Figure 2

Table 1

Pin No.	Symbol	Description
1	DO	FET gate control pin for discharge (CMOS output)
2	VM	Voltage detection pin between VM and VSS (Overcurrent detection pin)
3	CO	FET gate control pin for charge (CMOS output)
4	DP	Test pin for delay time measurement
5	VDD	Positive power input pin
6	VSS	Negative power input pin

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4. Absolute Maximum Ratings

Table 2

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied pin	Absolute Maximum Rating	Unit
Input voltage between VDD and VSS	V_{DS}	VDD	V_{SS} −0.3 to V_{SS} +12	V
Input pin voltage for VM	V_{VM}	VM	V_{DD} −28 to V_{DD} +0.3	V
Output pin voltage for CO	V_{CO}	CO	V_{VM} −0.3 to V_{DD}+0.3	V
Output pin voltage for DO	V_{DO}	DO	V_{SS} −0.3 to V_{DD} +0.3	V
Power dissipation	P_D	—	250 (When not mounted on board)	mW
			650*1	mW
Operating ambient temperature	T_{opr}	—	−40 to +85	°C
Storage temperature	T_{stg}	—	−55 to +125	°C

*1. When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

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5. Electrical Characteristics

5-1. Except Detection Delay Time (25°C)

Table 3

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage	V_{CU}	—	V_{CU} −0.025	V_{CU} =4.375	V_{CU} +0.025	V	1	1
		Ta = −5°C to 55°C*1	V_{CU} −0.030	V_{CU} =4.375	V_{CU} +0.030	V	1	1
Overcharge hysteresis voltage	V_{HC}	—	V_{HC} −0.025	V_{HC} =0.20	V_{HC} +0.025	V	1	1
Overdischarge detection voltage	V_{DL}	—	V_{DL} −0.050	V_{DL} =2.80	V_{DL} +0.050	V	2	2
Overdischarge hysteresis voltage	V_{HD}	—	V_{HD} −0.050	V_{HD} =0.2	V_{HD} +0.050	V	2	2
Overcurrent 1 detection voltage	V_{IOV1}	—	V_{IOV1} −0.015	V_{IOV1} =0.15	V_{IOV1} +0.015	V	3	2
Overcurrent 2 detection voltage	V_{IOV2}	—	0.4	0.5	0.6	V	3	2
Load short-circuiting detection voltage	V_{SHORT}	—	0.9	1.2	1.5	V	3	2
Charger detection voltage	V_{CHA}	—	−1.0	−0.7	−0.4	V	4	2
INPUT VOLTAGE, OPERATION VOLTAGE								
Operation voltage between VDD and VSS	V_{DSOP1}	Internal circuit operating voltage	1.5	—	8	V	—	—
Operation voltage between VDD and VM	V_{DSOP2}	Internal circuit operating voltage	1.5	—	28	V	—	—
CURRENT CONSUMPTION								
Current consumption in normal operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V	1.0	3.5	7.0	μA	5	2
Current consumption at power down	I_{PDN}	V_{DD} = V_{VM} = 1.5 V	—	—	0.1	μA	5	2
OUTPUT RESISTANCE								
CO pin resistance "H"	R_{COH}	V_{CO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V	2.5	5	10	kΩ	7	4
CO pin resistance "L"	R_{COL}	V_{CO} = 0.5 V, V_{DD} = 4.5 V, V_{VM} = 0 V	2.5	5	10	kΩ	7	4
DO pin resistance "H"	R_{DOH}	V_{DO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V	2.5	5	10	kΩ	8	4
DO pin resistance "L"	R_{DOL}	V_{DO} = 0.5 V, V_{DD} = V_{VM} = 1.8 V	2.5	5	10	kΩ	8	4
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	100	300	900	kΩ	6	3
Internal resistance between VM and VSS	R_{VMS}	V_{DD} = 3.5 V, V_{VM} = 1.0 V	10	20	40	kΩ	6	3
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge "available"	1.2	—	—	V	11	2

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

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5-2. Except Detection Delay Time (−40°C to +85°C[*1])

Table 4

(Ta = −40°C to +85°C[*1] unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage	V_{CU}	—	V_{CU} −0.055	V_{CU} =4.375	V_{CU} +0.040	V	1	1
Overcharge hysteresis voltage	V_{HC}	—	V_{HC} −0.025	V_{HC} =0.20	V_{HC} +0.025	V	1	1
Overdischarge detection voltage	V_{DL}	—	V_{DL} −0.080	V_{DL} =2.80	V_{DL} +0.080	V	2	2
Overdischarge hysteresis voltage	V_{HD}	—	V_{HD} −0.050	V_{HD} =0.2	V_{HD} +0.050	V	2	2
Overcurrent 1 detection voltage	V_{IOV1}	—	V_{IOV1} −0.021	V_{IOV1} =0.15	V_{IOV1} +0.021	V	3	2
Overcurrent 2 detection voltage	V_{IOV2}	—	0.37	0.5	0.63	V	3	2
Load short-circuiting detection voltage	V_{SHORT}	—	0.7	1.2	1.7	V	3	2
Charger detection voltage	V_{CHA}	—	−1.2	−0.7	−0.2	V	4	2
INPUT VOLTAGE, OPERATION VOLTAGE								
Operation voltage between VDD and VSS	V_{DSOP1}	Internal circuit operating voltage	1.5	—	8	V	—	—
Operation voltage between VDD and VM	V_{DSOP2}	Internal circuit operating voltage	1.5	—	28	V	—	—
CURRENT CONSUMPTION								
Current consumption in normal operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V	0.7	3.5	8.0	μA	5	2
Current consumption at power down	I_{PDN}	V_{DD} = V_{VM} = 1.5 V	—	—	0.1	μA	5	2
OUTPUT RESISTANCE								
CO pin resistance "H"	R_{COH}	V_{CO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V	1.2	5	15	kΩ	7	4
CO pin resistance "L"	R_{COL}	V_{CO} = 0.5 V, V_{DD} = 4.5 V, V_{VM} = 0 V	1.2	5	15	kΩ	7	4
DO pin resistance "H"	R_{DOH}	V_{DO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V	1.2	5	15	kΩ	8	4
DO pin resistance "L"	R_{DOL}	V_{DO} = 0.5 V, V_{DD} = V_{VM} = 1.8 V	1.2	5	15	kΩ	8	4
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	78	300	1310	kΩ	6	3
Internal resistance between VM and VSS	R_{VMS}	V_{DD} = 3.5 V, V_{VM} = 1.0 V	7.2	20	44	kΩ	6	3
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge "available"	1.7	—	—	V	11	2

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

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5-3. Detection Delay Time

Table 5

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t_{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t_{DL}	—	115	144	173	ms	9	5
Overcurrent 1 detection delay time	t_{IOV1}	—	7.2	9	11	ms	10	5
Overcurrent 2 detection delay time	t_{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t_{SHORT}	—	220	320	380	µs	10	5
DELAY TIME (Ta = −40°C to +85°C) *1								
Overcharge detection delay time	t_{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t_{DL}	—	80	144	245	ms	9	5
Overcurrent 1 detection delay time	t_{IOV1}	—	5	9	15	ms	10	5
Overcurrent 2 detection delay time	t_{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t_{SHORT}	—	150	320	540	µs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

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6. Test Circuits

Caution **Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.**

(1) Test Condition 1, Test Circuit 1

(Overcharge Detection Voltage, Overcharge Hysteresis Voltage)

The overcharge detection voltage (V_{CU}) is defined as the voltage between VDD and VSS at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.5 V. The overcharge hysteresis voltage (V_{HC}) is then defined as the difference between the overcharge detection voltage (V_{CU}) and the voltage between VDD and VSS at which V_{CO} goes from "L" to "H" when the voltage V1 is gradually decreased.

(2) Test Condition 2, Test Circuit 2

(Overdischarge Detection Voltage, Overdischarge Hysteresis Voltage)

The overdischarge detection voltage (V_{DL}) is defined as the voltage between VDD and VSS at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = 3.5 V and V2 = 0 V. The overdischarge hysteresis voltage (V_{HD}) is then defined as the difference between the overdischarge detection voltage (V_{DL}) and the voltage between VDD and VSS at which V_{DO} goes from "L" to "H" when the voltage V1 is gradually increased.

(3) Test Condition 3, Test Circuit 2

(Overcurrent 1 Detection Voltage, Overcurrent 2 Detection Voltage, Load Short-Circuiting Detection Voltage)

The overcurrent 1 detection voltage (V_{IOV1}) is defined as the voltage between VM and VSS whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of the overcurrent 1 detection delay time when the voltage V2 is increased rapidly (within 10 μs) from the starting condition V1 = 3.5 V and V2 = 0 V.

The overcurrent 2 detection voltage (V_{IOV2}) is defined as the voltage between VM and VSS whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of the overcurrent 2 detection delay time when the voltage V2 is increased rapidly (within 10 μs) from the starting condition V1 = 3.5 V and V2 = 0 V.

The load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage between VM and VSS whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of the load short-circuiting detection delay time when the voltage V2 is increased rapidly (within 10 μs) from the starting condition V1 = 3.5 V and V2 = 0 V.

(4) Test Condition 4, Test Circuit 2

(Charger Detection Voltage, Abnormal Charge Current Detection Voltage)

The charger detection voltage (V_{CHA}) is defined as the voltage between VM and VSS at which V_{DO} goes from "L" to "H" when the voltage V2 is gradually decreased from 0 V after the voltage V1 is gradually increased from the starting condition of V1 = 1.8 V and V2 = 0 V until the voltage V1 becomes V1 = V_{DL} + (V_{HD} / 2).

The charger detection voltage can be measured only in the product whose overdischarge hysteresis $V_{HD} \neq 0$.

Set V1 = 3.5 V and V2 = 0 V. Decrease V2 from 0 V gradually. The voltage between VM and VSS when V_{CO} goes from "H" to "L" is the abnormal charge current detection voltage. The abnormal charge current detection voltage has the same value as the charger detection voltage (V_{CHA}).

(5) Test Condition 5, Test Circuit 2

(Normal Operation Current Consumption, Power-Down Current Consumption)

The operating current consumption (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 3.5 V and V2 = 0 V (Normal status).

The power-down current consumption (I_{PDN}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = V2 = 1.5 V (Overdischarge status).

(6) Test Condition 6, Test Circuit 3

(Internal Resistance between VM and VDD, Internal Resistance between VM and VSS)

The resistance between VM and VDD (R_{VMD}) is the internal resistance between VM and VDD under the set conditions of V1 = 1.8 V and V2 = 0 V.

The resistance between VM and VSS (R_{VMS}) is the internal resistance between VM and VSS under the set conditions of V1 = 3.5 V and V2 = 1.0 V.

(7) Test Condition 7, Test Circuit 4

(CO Pin Resistance "H", CO Pin Resistance "L")

The CO pin resistance "H" (R_{COH}) is the resistance the CO pin under the set condition of V1 = 3.5 V, V2 = 0 V and V3 = 3.0 V.

The CO pin resistance "L" (R_{COL}) is the resistance the CO pin under the set condition of V1 = 4.5 V, V2 = 0 V and V3 = 0.5 V.

(8) Test Condition 8, Test Circuit 4

(DO Pin Resistance "H", DO Pin Resistance "L")

The DO pin resistance "H" (R_{DOH}) is the resistance the DO pin under the set condition of V1 = 3.5 V, V2 = 0 V and V4 = 3.0 V.

The DO pin resistance "L" (R_{DOL}) is the resistance the DO pin under the set condition of V1 = 1.8 V, V2 = 0 V and V4 = 0.5 V.

(9) Test Condition 9, Test Circuit 5

(Overcharge Detection Delay Time, Overdischarge Detection Delay Time)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the voltage V1 momentarily increases (within 10 μs) from the overcharge detection voltage (V_{CU}) − 0.2 V to the overcharge detection voltage (V_{CU}) + 0.2 V under the set condition of V2 = 0 V.

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the voltage V1 momentarily decreases (within 10 μs) from the overdischarge detection voltage (V_{DL}) +0.2 V to the overdischarge detection voltage (V_{DL}) − 0.2 V under the set condition of V2 = 0 V.

(10) Test Condition 10, Test Circuit 5

(Overcurrent 1 Detection Delay Time, Overcurrent 2 Detection Delay Time, Load Short-circuiting Detection Delay Time, Abnormal Charge Current Detection Delay Time)

The overcurrent 1 detection delay time (t_{IOV1}) is the time needed for V_{DO} to go "L" after the voltage V2 momentarily increases (within 10 μs) from 0 V to 0.35 V under the set condition of V1 = 3.5 V and V2=0 V.

The overcurrent 2 detection delay time (t_{IOV2}) is the time needed for V_{DO} to go "L" after the voltage V2 momentarily increases (within 10 μs) from 0 V to 0.7 V under the set condition of V1 = 3.5 V and V2 = 0 V.

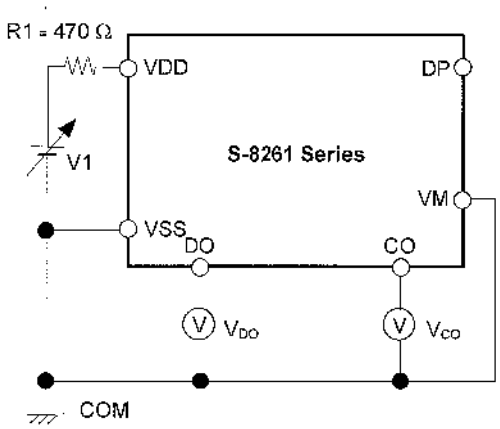
The load short-circuiting detection delay time (t_{SHORT}) is the time needed for V_{DO} to go "L" after the voltage V2 momentarily increases (within 10 μs) from 0 V to 1.6 V under the set condition of V1 = 3.5 V and V2 = 0 V.

The abnormal charge current detection delay time is the time needed for V_{CO} to go from "H" to "L" after the voltage V2 momentarily decreases (within 10 μs) from 0 V to −1.1 V under the set condition of V1 = 3.5 V and V2 = 0 V. The abnormal charge current detection delay time has the same value as the overcharge detection delay time.

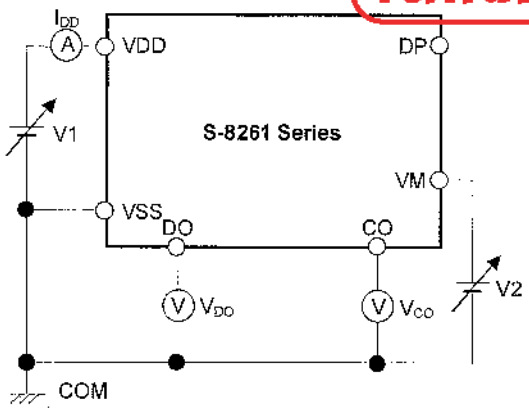
(11) Test Condition 11, Test Circuit 2

(0 V Battery Charge Starting Charger Voltage)

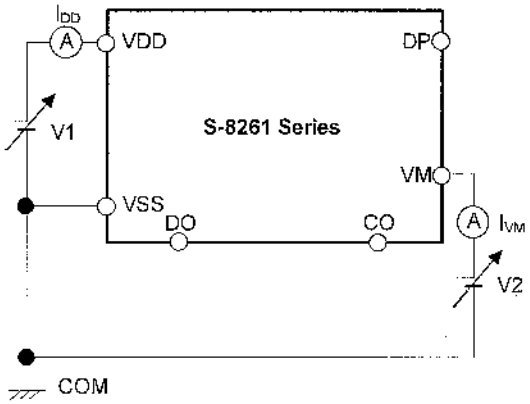
The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the voltage between VDD and VM at which V_{CO} goes "H" (V_{VM} + 0.1 V or higher) when the voltage V2 is gradually decreased from the starting condition of V1 = V2 = 0 V.



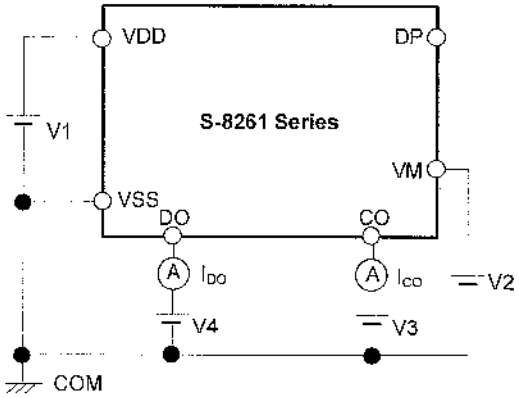
Test Circuit 1



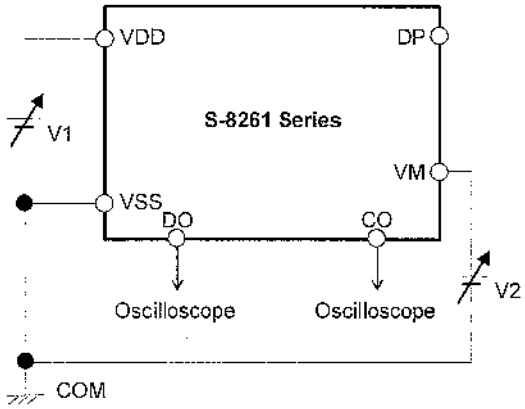
Test Circuit 2



Test Circuit 3



Test Circuit 4



Test Circuit 5

Figure 3

7. Operation

Remark Refer to "**9. Battery Protection IC Connection Example**".

7-1. Normal Status

The S-8261 Series monitors the voltage of the battery connected between VDD pin and VSS pin and the voltage difference between VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from the overdischarge detection voltage (V_{DL}) to the overcharge detection voltage (V_{CU}), and the VM pin voltage is in the range from the charger detection voltage (V_{CHA}) to the overcurrent 1 detection voltage (V_{IOV1}), the IC turns both the charging and discharging control FETs on. This status is called the normal status, and in this status charging and discharging can be carried out freely.

Caution When a battery is connected to the IC for the first time, discharging may not be enabled. In this case, short the VM pin and VSS pin or connect the charger to restore the normal condition.

7-2. Overcurrent Status (Detection of Overcurrent 1, Overcurrent 2 and Load Short-circuiting)

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the overcurrent detection voltage because the discharge current is higher than the specified value and the status lasts for the overcurrent detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the overcurrent status.
In the overcurrent status, the VM and VSS pins are shorted by the resistor between VM and VSS (R_{VMS}) in the IC. However, the voltage of the VM pin is at the V_{DD} potential due to the load as long as the load is connected. When the load is disconnected completely, the VM pin returns to the V_{SS} potential.
The voltage of the VM pin returns to overcurrent 1 detection voltage (V_{IOV1}) or lower and the overcurrent status is restored to the normal status.

7-3. Overcharge Status

When the battery voltage becomes higher than the overcharge detection voltage (V_{CU}) during charging under the normal status and the detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8261 Series turns the charging control FET off to stop charging. This status is called the overcharge status.
The overcharge status is released by the following two cases ((1) and (2)):

(1) When the battery voltage falls below the overcharge detection voltage (V_{CU}) – overcharge hysteresis voltage (V_{HC}), the S-8261 Series turns the charging control FET on and turns to the normal status.
(2) When a load is connected and discharging starts, the S-8261 Series turns the charging control FET on and returns to the normal status. Just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment the VM pin potential becomes V_f, the voltage for the parasitic diode, higher than V_{SS} level. When the battery voltage goes under the overcharge detection voltage (V_{CU}) and provided that the VM pin voltage is higher than the overcurrent 1 detection voltage, the S-8261 Series releases the overcharge status.

Caution 1. If the battery is charged to a voltage higher than the overcharge detection voltage (V_{CU}) and the battery voltage does not fall below the overcharge detection voltage (V_{CU}) even when a heavy load is connected, the detection of overcurrent 1, overcurrent 2 and load short-circuiting do not function until the battery voltage falls below overcharge detection voltage (V_{CU}). Since an actual battery has an internal impedance of several dozens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and the detection of overcurrent 1, overcurrent 2 and load short-circuiting function.
2. When a charger is connected after the overcharge detection, the overcharge status is not released even if the battery voltage is below the overcharge release voltage (V_{CL}). The overcharge status is released when the VM pin voltage goes over the charger detection voltage (V_{CHA}) by removing the charger.

Tentative

7-4. Overdischarge Status

When the battery voltage falls below the overdischarge detection voltage (V_{DL}) during discharging under the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8261 Series turns the discharging control FET off to stop discharging. This status is called the overdischarge status. When the discharging control FET is turned off, the VM pin voltage is pulled up by the resistor between VM and VDD in the IC (R_{VMD}). When the voltage difference between the VM and VDD then is 1.3 V (typ.) or lower, the current consumption is reduced to the power-down current consumption (I_{PDN}). This status is called the power-down status.
The power-down status is released when a charger is connected and the voltage difference between the VM and VDD becomes 1.3 V (typ.) or higher. Moreover when the battery voltage becomes the overdischarge detection voltage (V_{DL}) or higher, the S-8261 Series turns the discharging FET on and returns to the normal status.

7-5. Charger Detection

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than the charger detection voltage (V_{CHA}), the S-8261 Series releases the overdischarge status and turns the discharging control FET on when the battery voltage becomes equal to or higher than the overdischarge detection voltage (V_{DL}) since the charger detection function works. This action is called charger detection.
When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than the charger detection voltage (V_{CHA}), the S-8261 Series releases the overdischarge status when the battery voltage reaches the overdischarge detection voltage (V_{DL}) + overdischarge hysteresis voltage (V_{HD}) or higher.

7-6. Abnormal Charge Current Detection

If the VM pin voltage falls below the charger detection voltage (V_{CHA}) during charging under normal status and it continues for the overcharge detection delay time (t_{CU}) or longer, the charging control FET turns off and charging stops. This action is called the abnormal charge current detection.
Abnormal charge current detection works when the DO pin voltage is "H" and the VM pin voltage falls below the charger detection voltage (V_{CHA}). Consequently, if an abnormal charge current flows to an over-discharged battery, the S-8261 Series turns the charging control FET off and stops charging after the battery voltage becomes higher than the overdischarge detection voltage which make the DO pin voltage "H", and still after the overcharge detection delay time (t_{CU}) elapses.
Abnormal charge current detection is released when the voltage difference between VM pin and VSS pin becomes less than charger detection voltage (V_{CHA}).

7-7. Delay Circuit

The detection delay times are determined by dividing a clock of the approximately 3.5 kHz with the counter.

Remark 1. The detection delay time for overcurrent 2 (t_{IOV2}) and load short-circuiting (t_{SHORT}) start when the overcurrent 1 (V_{IOV1}) is detected. When the overcurrent 2 (V_{IOV2}) or load short-circuiting (V_{SHORT}) is detected over the detection delay time for each of them (= t_{IOV2} or t_{SHORT}) after the detection of overcurrent 1 (V_{IOV1}), the S-8261 Series turns the FET off within t_{IOV2} or t_{SHORT} of each detection.

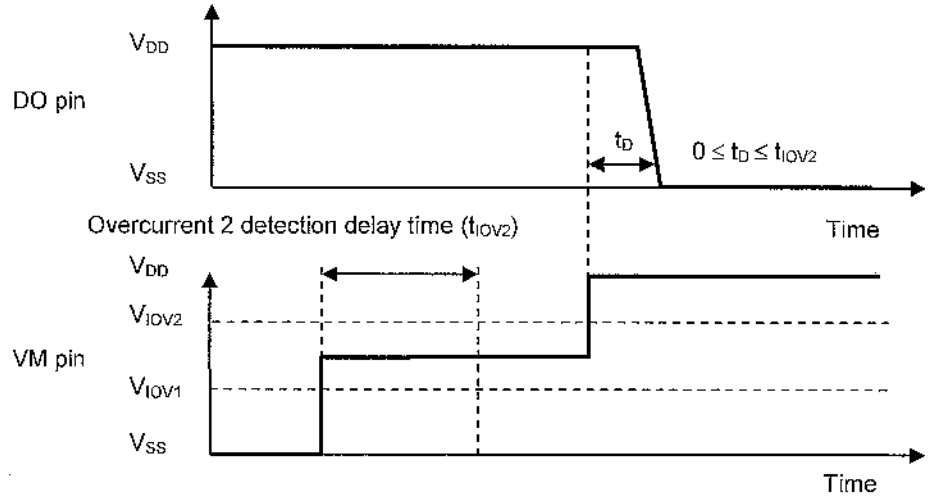


Figure 4

2. When the overcurrent is detected and continues for longer than the overdischarge detection delay time (t_{DL}) without releasing the load, the status changes to the power-down status when the battery voltage falls below the overdischarge detection voltage (V_{DL}). When the battery voltage falls below the overdischarge detection voltage (V_{DL}) due to the overcurrent, the S-8261 Series turns the discharging control FET off by the overcurrent detection. In this case if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time (t_{DL}) is still lower than the overdischarge detection voltage (V_{DL}), the S-8261 Series shifts to the power-down status.

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7-8. DP Pin

The DP pin is a test pin for delay time measurement and it should be open in the actual application. If a capacitor whose capacitance is larger than 1000 pF or a resistor whose resistance is less than 1 MΩ is connected to this pin, error may occur in the delay times or in the detection voltages.

7-9. 0 V Battery Charge Function "Available"

This function is used to recharge the connected battery whose voltage is 0 V due to the self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or higher is applied between EB+ pin and EB− pin by connecting a charger, the charging control FET gate is fixed to VDD pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than the overdischarge detection voltage (V_{DL}) and the overdischarge hysteresis voltage (V_{HD}), the S-8261 Series enters the normal status.

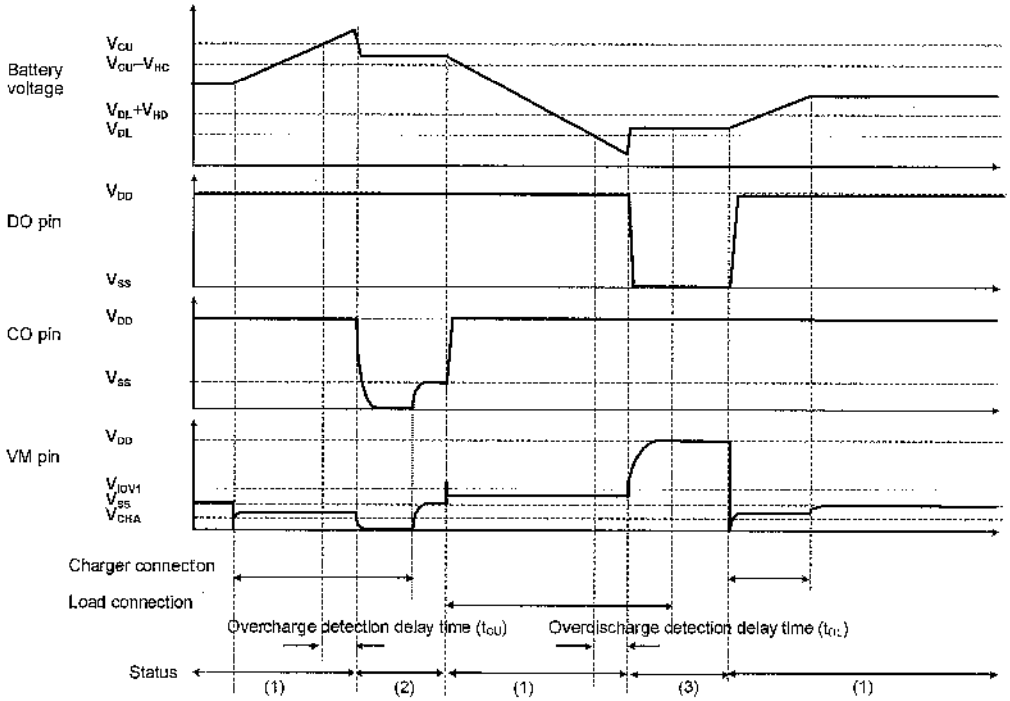
Caution **Some battery providers do not recommend charging for completely self-discharged battery. Please ask battery providers before determine whether to enable or inhibit the 0 V battery charge function.**

Remark The 0 V battery charge function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0 V battery charging function is enabled charges a battery forcibly and abnormal charge current cannot be detected when the battery voltage is low.

Tentative

8. Timing Chart

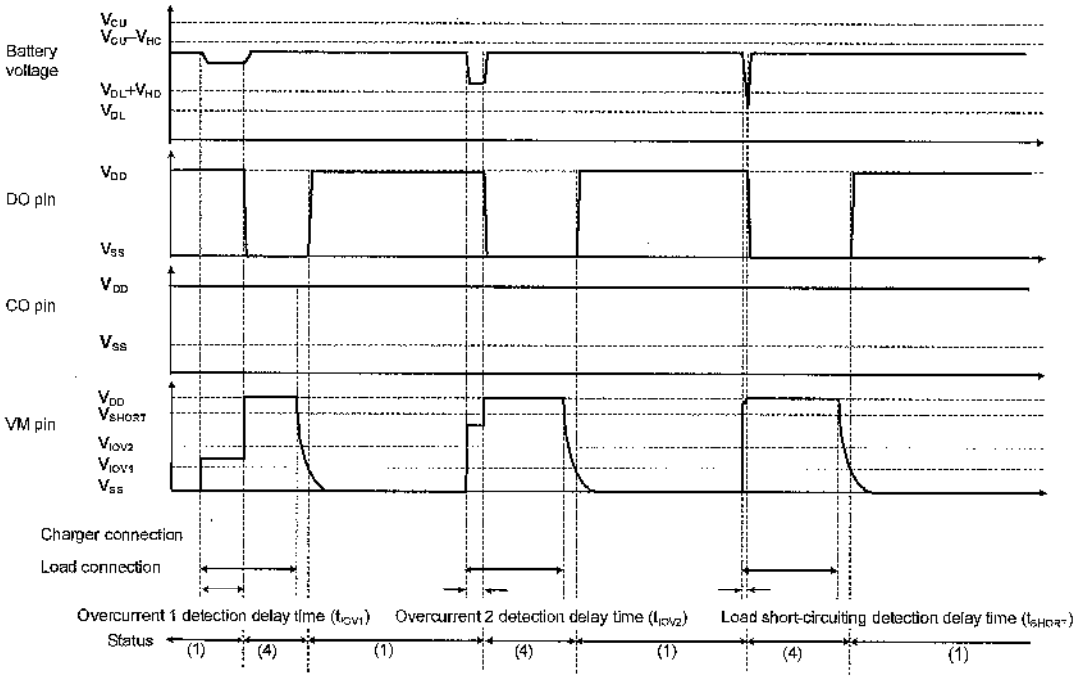
(1) Overcharge and Overdischarge Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
The charger is supposed to charge with constant current.

Figure 5

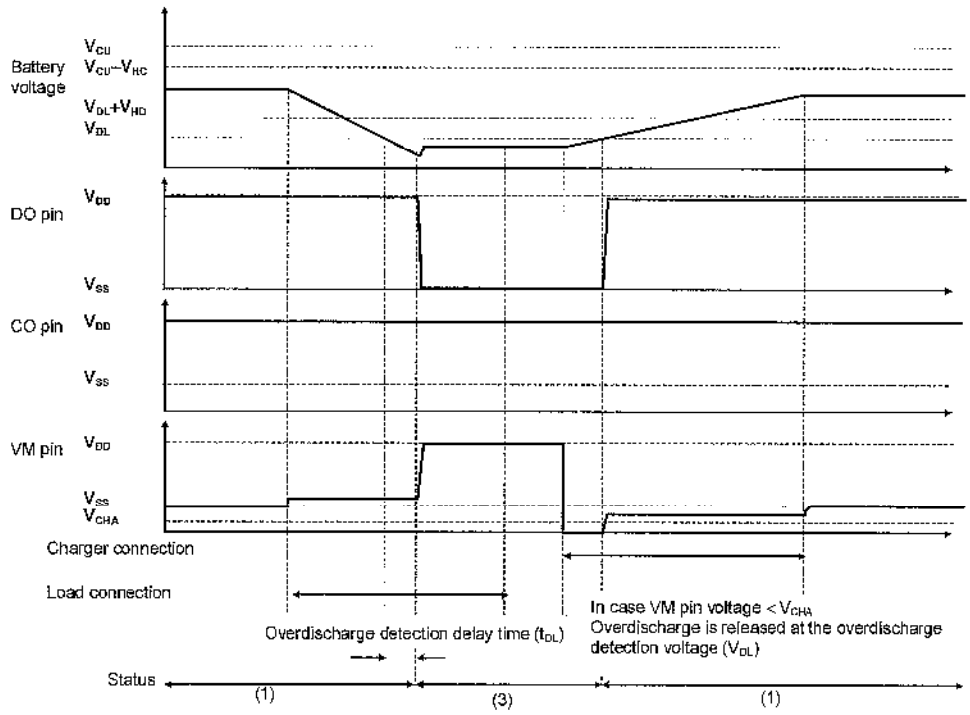
(2) Overcurrent Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
The charger is supposed to charge with constant current.

Figure 6

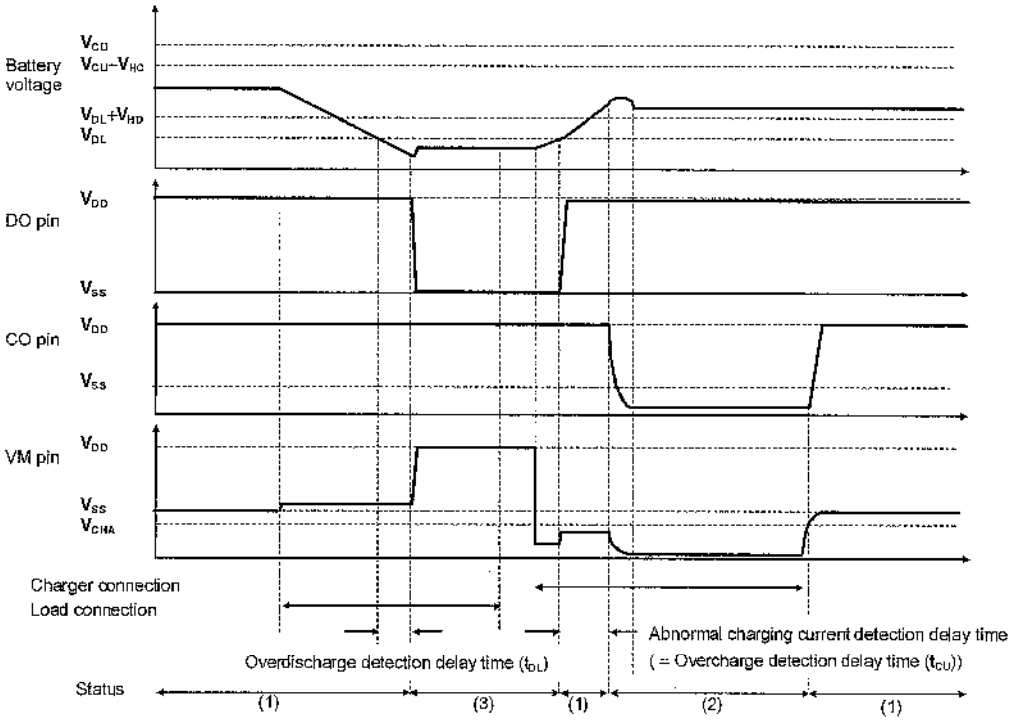
(3) Charger Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
The charger is supposed to charge with constant current.

Figure 7

(4) Abnormal Charge Current Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
The charger is supposed to charge with constant current.

Figure 8

Tentative

9. Battery Protection IC Connection Example

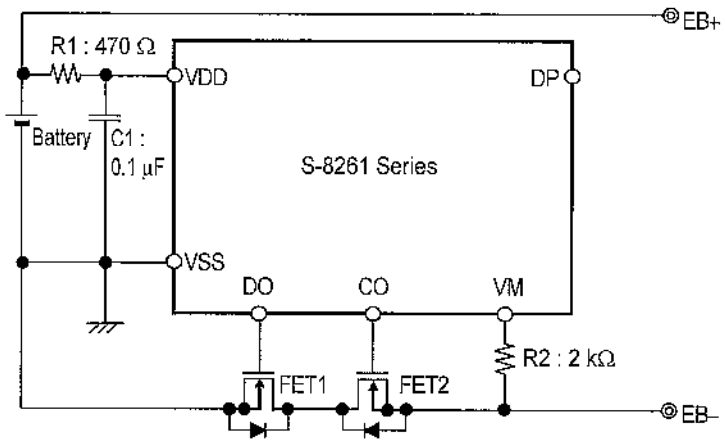


Figure 9

Table 6 Constant for External Components

Symbol	Part	Purpose	Typ.	Min.	Max.	Remarks
FET1	N-channel MOS FET	Discharge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage*1 Gate to source withstanding voltage ≥ Charger voltage*2
FET2	N-channel MOS FET	Charge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage*1 Gate to source withstanding voltage ≥ Charger voltage*2
R1	Resistor	ESD protection, For power fluctuation	470 Ω	300 Ω	1 kΩ	Resistance should be as small as possible to avoid lowering of the overcharge detection accuracy caused by VDD pin current.*3
C1	Capacitor	For power fluctuation	0.1 μF	0.022 μF	1.0 μF	Install a capacitor of 0.022 μF or higher between VDD and VSS.*4
R2	Resistor	Protection for reverse connection of a charger	2 kΩ	300 Ω	4 kΩ	Select a resistance as large as possible to prevent large current when a charger is connected in reverse.*5

*1. If the threshold voltage of an FET is low, the FET may not cut the charging current.
If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

*2. If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

*3. If R1 has a high resistance, the voltage between VDD and VSS may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC. Insert a resistor of 300 Ω or higher to R1 for ESD protection.

*4. If a capacitor of less than 0.022 μF is connected to C1, DO may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.022 μF or higher to C1.

*5. If R2 has a resistance higher than 4 kΩ, the charging current may not be cut when a high-voltage charger is connected.

Caution 1. The DP pin should be open.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

10. Precautions

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- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

Tentative

RELIABILITY TEST DATA

Product name : S-8261AxxMD-xxxTxU
Package type : SOT-23-6

No.	Test item	Test Condition	Test Time	r/n
1	High Temperature Operation	Ta=125 °C V_{DD}=Vopr max.	1000 h	0/22
2	High Temperature Bias	Ta=125 °C V_{DD}=Vabs max.×0.9	1000 h	0/22
3	#1 Temperature Humidity Bias	Ta=85 °C RH=85 % V_{DD}=Vabs max.×0.9	1000 h	0/22
4	#1 Un-saturated Pressure Cooker Bias	Ta=125 °C RH=85 % P=2×10^5 Pa V_{DD}=Vabs max.×0.9	100 h	0/22
5	High Temperature Storage	Tstg max.=150 °C	1000 h	0/22
6	Low Temperature Storage	Tstg min.=–65 °C	1000 h	0/22
7	#1 Temperature Cycle (Gas phase)	Tstg max.=150 °C , Tstg min.=–65 °C (30 min each)	200 cycles	0/22
8	#1 Thermal Shock (Liquid phase)	Tstg max.=150 °C , Tstg min.=–65 °C (5 min each)	100 cycles	0/22
9	#1 Resistance to soldering heat - 1 (reflow)	T=260 °C ,10 s	3 times	0/22
10	#1 Resistance to soldering heat - 2 (Solder iron)	T=380 °C , 5 s	Twice	0/22
11	#2 Solderability	T=230 °C Solder material ; Sn-3.0Ag-0.5Cu	3 s	0/11
12	Whisker - 1 (Room Temperature Storage)	Ta=25±3 °C RH=40～70% criteria ; Whisker should be less than 50μm	3 months	0/10
13	Whisker - 2 (Temperature Cycle)	Tstg max.=85 °C , Tstg min.=–40 °C (30 min each) criteria ; Whisker should be less than 50μm	1000 cycles	0/10
14	Whisker - 3 (Temperature Humidity Storage)	Ta=60 °C RH=93 % criteria ; Whisker should be less than 50μm	2000 h	0/10
15	Solder Joint Reliability (Temperature Cycle + shear test)	Tstg max.=125 °C , Tstg min.=–40 °C (30 min each) Solder material ; Sn-3.0Ag-0.5Cu criteria ;After temperature cycle test, keep strength for shear stress more than the 50 % of initial mean value.	2000 cycles	0/5
16	Lead Strength (Pull test)	Pull force ; 2.5 N	30 s	0/11
17	Lead Strength (Bending test)	Load ; 1.25 N 45 degree Bend a lead	Twice	0/11

18	ESD - 1 (Human Body Model)	V=±2000 V C=100 pF R=1.5 kΩ Ref. To V_{DD} / Vss (5units for each direction)	5 pulses	0/20
19	ESD - 2 (Machine Model)	V=±200 V C=200 pF R=0 Ω Ref. To V_{DD} / Vss (5units for each direction)	3 pulses	0/20
20	Latch Up	±100 mA (V_{CLAMP} = Vopr max.) 10 ms pulse V_{DD} =Vopr max.	1 pulse	0/5

Remark : Vabs max. = Absolute maximum voltage , Vopr max. =Maximum operation voltage
: Each test designated # is performed after Pre-Treatment finished.
Pre-Treatment consists of High Temperature Storage ,Temperature Humidity Storage and Soldering Heat. (See the table below.)

Pre Treatment (#1)		
High Temp. Storage	Temperature Humidity Storage	Soldering Heat
Ta=125 °C t=24 h	Ta=85 °C RH=85 % t=168 h	Infrared Reflow 3 times T=260 °C t=10 s

Pre Treatment (#2)		
High Temp. Storage	Temperature Humidity Storage	Soldering Heat
Ta=125 °C t=24 h	Ta=105 °C RH=100 % t=8 h	—

Tentative

Notes on soldering SOT packages

(1) Storage

The epoxy resin used in SOT packages absorbs moisture in air, and the absorbed moisture vaporizes and expands during mounting. When the absorbed moisture amount becomes large, the separation at the interfaces between the resin and inner lead or package cracks may occur. For this reason, storage in lower humidity environment is recommended.

SOT packages adapted to the storage condition of the ambient temperature (Ta) of 5 to 30 °C and relative humidity (RH) of 40 to 70%.

(2) Rinse

When rinse-free flax is applied, rinsing is not necessary. Good selection of flax is indispensable to avoid corrosion. When normal flax (including rosin) is applied, complete rinsing is necessary to remove the flax so as not to cause corrosion.

(3) Iron soldering

When using a soldering iron or heating collet, you should observe the following precautions.

① Maintain the maximum temperature of the soldering iron at 380°C for 5 seconds or less.

② Maintain the maximum temperature of the resin at 235°C and heating time for 10 seconds or less.

(4) Temperature profile for soldering (Infrared reflow and Flow soldering)

(4)-1 Infrared reflow

Infrared absorption rate depends on resin, lead material, and solder paste. In case of determining the reflow temperature profile, the temperature should be taken at the package surface to prevent the package crack. If the temperature of lead part is used to determine the reflow temperature, a package crack may occur since the package surface temperature is normally higher than that of the lead part.

Figure 1 shows an example of temperature profile for infrared reflow.

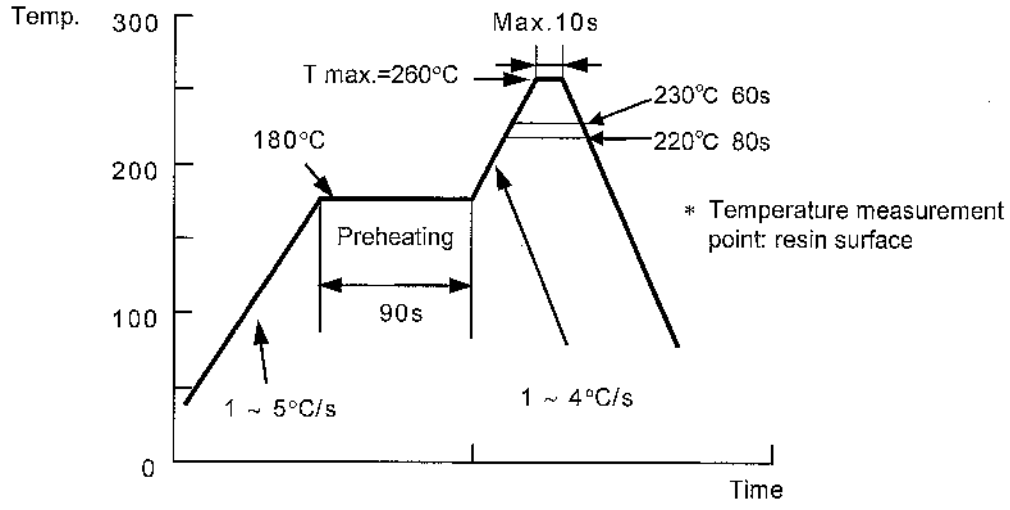


Figure 1 Heat-resistance reflow condition for parts

Number of maximum reflow cycles: Three times

(4)-2 Flow soldering

Flow soldering gives larger thermal stress to IC chips compared to infrared reflow. Preheating is indispensable to relax the thermal stress. Figure 2 shows an example of temperature profile of flow soldering.

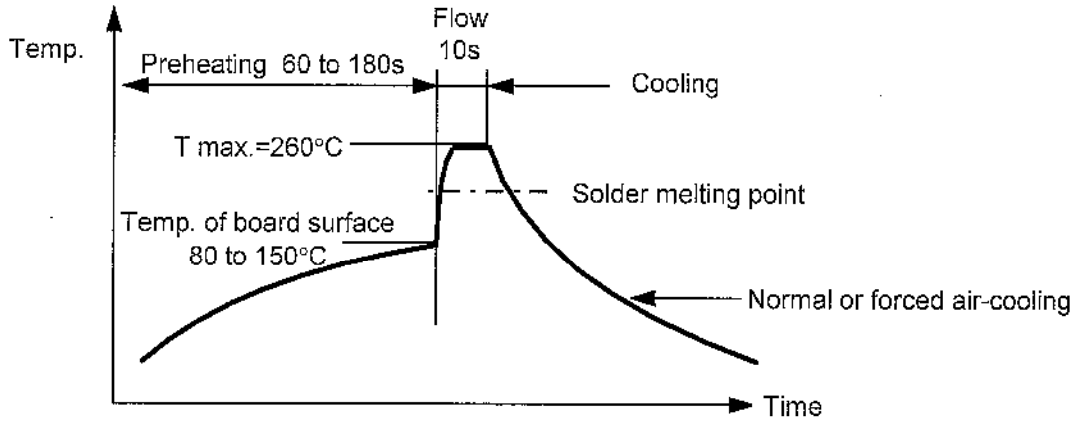


Figure 2 Heat-resistance solder flow condition for parts

Tentative

Package and Reel Specifications

SOT-23-6

1. Package Specifications (Lead-free plating)

(1) Dimensions

Refer to the attached drawing: No. MP006-A-P-SD-2.0

(2) Marking

Refer to the attached drawing: No. MP006-A-M-SD-1.1

Note: The product code to be specified in the drawing is "G4V".

2. Reel Specifications

(1) Supply Unit

The minimum delivery unit is a tape reel. (3,000 pcs/reel)
In principle, a tape reel consists of the same lot products. Remains, if any, are gathered into a tape reel which is composed of remains of various lots. The composing is indicated on the label.

(2) Form

Tape reels shall be put into a delivery container with protection methods against excessive shocks, temperature, humidity, and static electricity during freight.

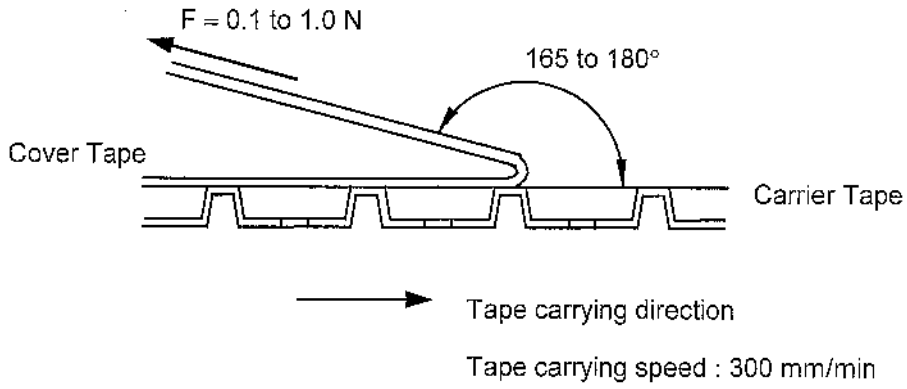
(3) Reel Dimensions

Refer to the attached drawing: No. MP006-A-R-SD-2.1

(4) Carrier Tape Dimensions

Refer to the attached drawing: No. MP006-A-C-SD-3.1

(5) Cover Tape Removal Force



Tape carrying speed : 300 mm/min

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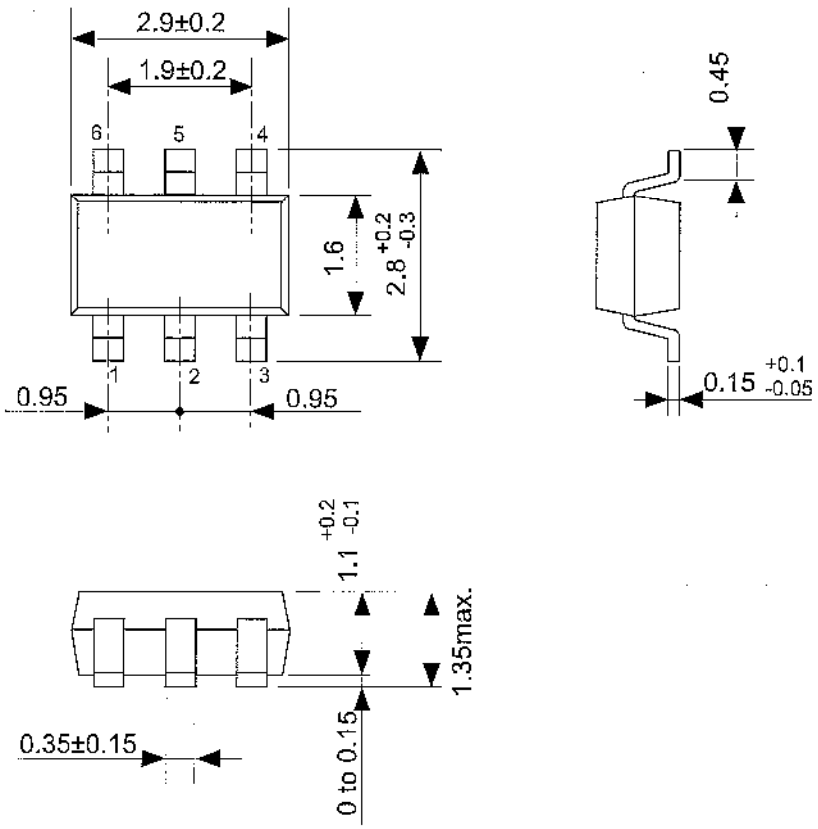
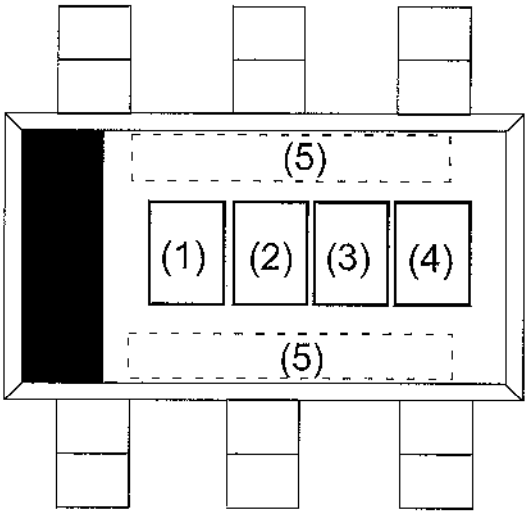


No. MP006-A-P-SD-2.0

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

Tentative



(1) to (3) : Product code

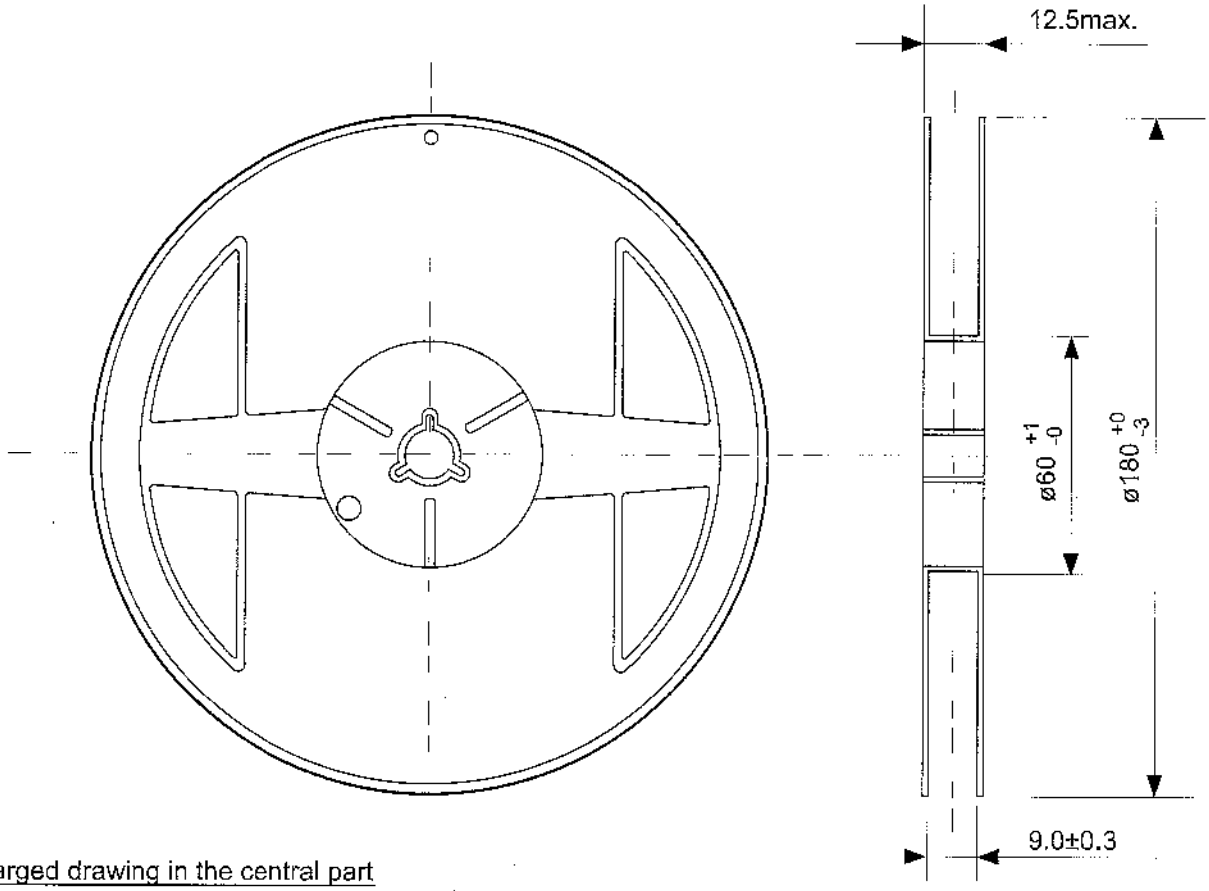
(4) : Month of assembly

(5) : Dot on one side (Year and week of assembly)

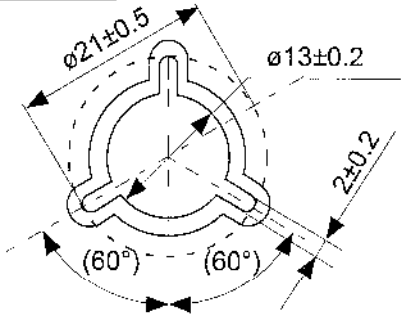
No. MP006-A-M-SD-1.1

TITLE	SOT236-A-Markings		
No.	MP006-A-M-SD-1.1		
SCALE			
UNIT	mm	TYPE	LASER
Seiko Instruments Inc.			

Tentative



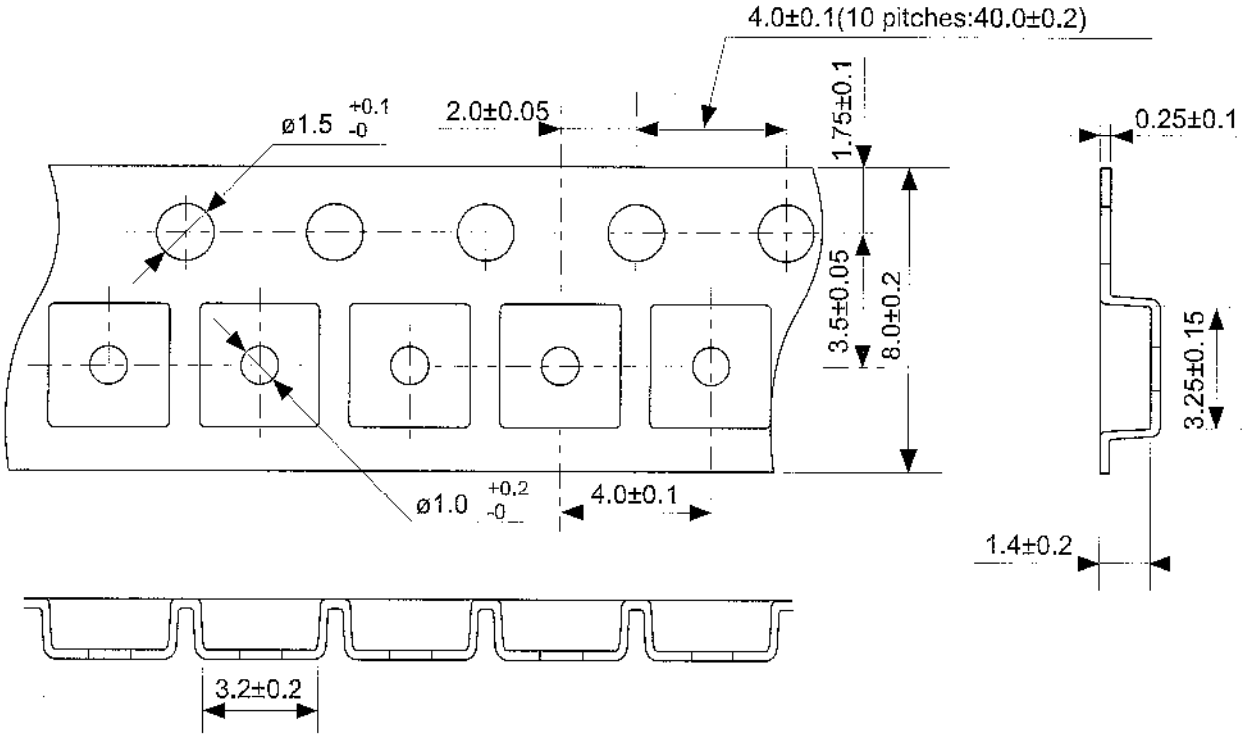
Enlarged drawing in the central part

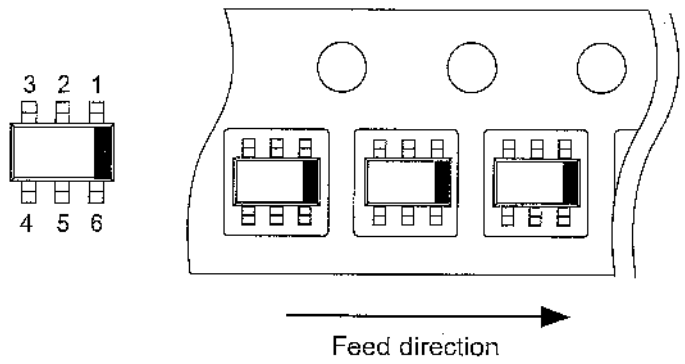


No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
SCALE		QTY	3,000
UNIT	mm		
Seiko Instruments Inc.			

Tentative





No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	