

TLVx170 36-V, Single-Supply, EMI-Hardened, Low-Power Operational Amplifiers for Cost-Sensitive Systems

1 Features

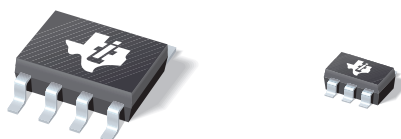
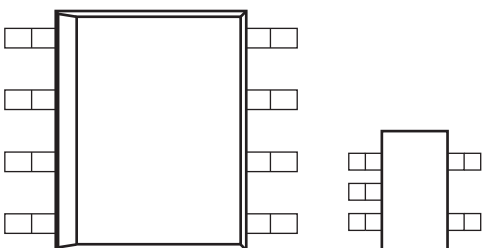
- Supply Range: 2.7 V to 36 V, ± 1.35 V to ± 18 V
- Low Noise: 22 nV/ $\sqrt{\text{Hz}}$
- EMI-Hardened with RFI-Filtered Inputs
- Input Range Includes the Negative Supply
- Unity-Gain Stable: 200-pF Capacitive Load
- Rail-to-Rail Output
- Gain Bandwidth: 1.2 MHz
- Low Quiescent Current: 125 μA per Amplifier
- High Common-Mode Rejection: 110 dB
- Low Bias Current: 10 pA (typical)

2 Applications

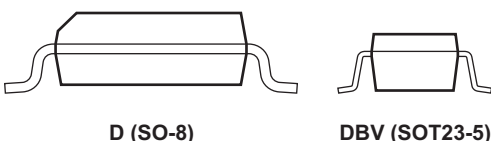
- Currency Counters
- AC-DC Converters
- Tracking Amplifiers in Power Modules
- Server Power Supplies
- Inverters
- Test Equipment
- Battery-Powered Instruments
- Transducer Amplifiers
- Line Drivers or Line Receivers

Smallest Packaging for 36-V Operational Amplifiers

Package Footprint Comparison (to Scale)



Package Height Comparison (to Scale)



3 Description

The TLVx170 family of electromagnetic interference (EMI)-hardened, 36-V, single-supply, low-noise operational amplifiers (op amps) have a THD+N of 0.0002% at 1 kHz and can operate on supplies that range from 2.7 V (± 1.35 V) to 36 V (± 18 V). These features, along with low noise and very high power-supply rejection ratio (PSRR), make the single-channel TLV170, dual-channel TLV2170, and quad-channel TLV4170 suitable for use in microvolt-level signal amplification. The TLVx170 family of devices also gives good offset, drift, and bandwidth with low quiescent current.

Unlike most op amps that are specified at only one supply voltage, the TLVx170 family of op amps is specified from 2.7 V to 36 V with the ability to swing input signals beyond the supply rails without phase reversal. The TLVx170 family is also unity-gain stable with a 200-pF capacitive load with a 1.2-MHz bandwidth and a 0.4-V/ μs slew rate for use in current-to-voltage converters.

The device inputs can operate 100 mV below the negative rail and within 2 V of the positive rail for normal operation, and with full rail-to-rail input with reduced performance. The TLVx170 devices are specified from -40°C to $+125^{\circ}\text{C}$.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV170	SOIC (8)	4.90 mm \times 3.91 mm
	SOT-23 (5)	2.90 mm \times 1.60 mm
TLV2170	SOIC (8)	4.90 mm \times 3.91 mm
	VSSOP (8)	3.00 mm \times 3.00 mm
TLV4170	SOIC (14)	8.65 mm \times 3.91 mm
	TSSOP (14)	5.00 mm \times 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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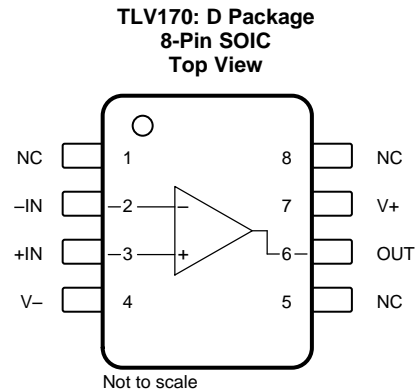
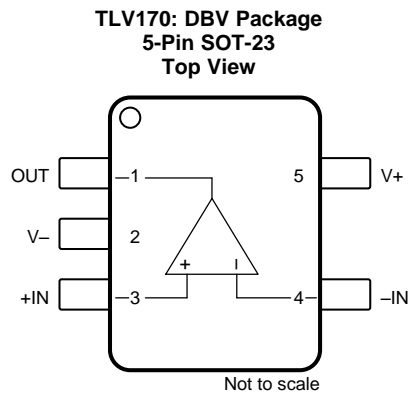
4 Revision History

Changes from Original (November 2016) to Revision A	Page
• Updated the <i>Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application</i> figure.....	18

Table 1. Device Comparison

PART NUMBER	NO OF CHANNELS	PACKAGE-LEAD			
		SOT23-5	D	VSSOP (micro size)	TSSOP
TLV170	1	5	8	—	—
TLV2170	2	—	8	8	—
TLV4170	4	—	14	—	14

5 Pin Configuration and Functions

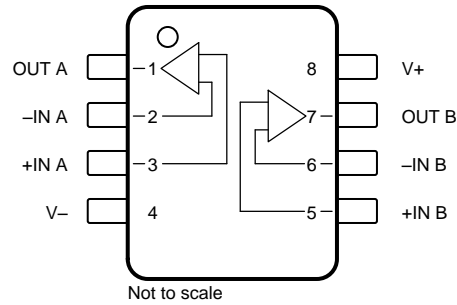


Pin Functions: TLV170

NAME	PIN		I/O	DESCRIPTION
	TLV170			
	SOT-23	D		
-IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC ⁽¹⁾	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V-	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

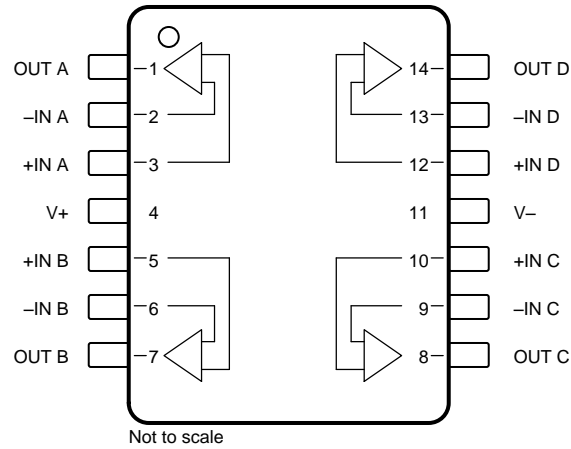
(1) NC indicates no internal connection.

**TLV2170: D and DGK Packages
8-Pin SOIC and VSSOP
Top View**



Pin Functions: TLV2170

NAME	PIN		I/O	DESCRIPTION
	TLV2170			
	SOIC	VSSOP (micro size)		
-IN A	2	2	I	Inverting input, channel A
-IN B	6	6	I	Inverting input, channel B
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V-	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

**TLV4170: D and PW Packages
14-Pin SOIC and TSSOP
Top View**

Pin Functions: TLV4170

PIN			I/O	DESCRIPTION
NAME	SOIC	TSSOP		
-IN A	2	2	I	Inverting input, channel A
-IN B	6	6	I	Inverting input, channel B
-IN C	9	9	I	Inverting input, channel C
-IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V-	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply voltage, [(V+) – (V–)]		40	V
	Single-supply voltage		40	
	Signal input pin	(V–) – 0.5	(V+) + 0.5	
Current	Signal input pin	–10	10	mA
	Output short-circuit ⁽²⁾	Continuous		
Temperature	Operating, T _A	–55	150	°C
	Junction, T _J		150	
	Storage, T _{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	Supply, V _S = (V+) – (V–)	2.7	36	V
T _A	Specified temperature	–40	125	°C
T _A	Operating temperature	–55	150	°C

6.4 Thermal Information: TLV170

THERMAL METRIC ⁽¹⁾		TLV170		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	133.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: TLV2170

THERMAL METRIC ⁽¹⁾		TLV2170		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	130	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.2	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.8	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: TLV4170

THERMAL METRIC ⁽¹⁾		TLV4170		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics

 at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
V_{OS} Input offset voltage	$T_A = 25^\circ\text{C}$		0.5	± 2.5	mV
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 2.7	
dV_{OS}/dT Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 2		$\mu\text{V}/^\circ\text{C}$
PSRR Power-supply rejection ratio	$V_S = 4\text{ V}$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	90	105		dB
	Channel separation, dc		5		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT					
I_B Input bias current	$T_A = 25^\circ\text{C}$		± 10		pA
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 1		nA
I_{OS} Input offset current	$T_A = 25^\circ\text{C}$		± 10		pA
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 50		
NOISE					
Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		2		μV_{PP}
e_n Input voltage noise density	$f = 100\text{ Hz}$		27		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		22		
INPUT VOLTAGE					
V_{CM} Common-mode voltage range ⁽¹⁾		$(V-) - 0.1$		$(V+) - 2$	V
CMRR Common-mode rejection ratio	$V_S = \pm 2\text{ V}$, $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		100		dB
	$V_S = \pm 18\text{ V}$, $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	95	110		
INPUT IMPEDANCE					
Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
Common-mode			$6 \parallel 3$		$10^{12}\ \Omega \parallel \text{pF}$
OPEN-LOOP GAIN					
A_{OL} Open-loop voltage gain	$V_S = 36\text{ V}$, $(V-) + 0.35\text{ V} < V_O < (V+) - 0.35\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	94	130		dB
FREQUENCY RESPONSE					
GBP Gain bandwidth product			1.2		MHz
SR Slew rate	$G = +1$		0.4		$\text{V}/\mu\text{s}$
t_s Settling time	To 0.1%, $V_S = \pm 18\text{ V}$, $G = +1$, 10-V step		20		μs
	To 0.01% (12-bit), $V_S = \pm 18\text{ V}$, $G = +1$, 10-V step		28		
THD+N Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3\text{ V}_{RMS}$		0.0002%		
OUTPUT					
V_O Voltage output swing from rail	$V_S = \pm 18\text{ V}$, $R_L = 10\text{ k}\Omega$; $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V-) + 0.2$		$(V+) - 0.3$	V
	$R_L = 10\text{ k}\Omega$, $A_{OL} \geq 94\text{ dB}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V-) + 0.35$		$(V+) - 0.35$	
I_{SC} Short-circuit current		-20		17	mA
C_{LOAD} Capacitive load drive		See Typical Characteristics: Table of Graphs			pF
R_O Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$		900		Ω
POWER SUPPLY					
V_S Specified voltage range		2.7		36	V
I_Q Quiescent current per amplifier	$I_O = 0\text{ A}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		125	175	μA

(1) The input range can be extended beyond $(V+) - 2\text{ V}$ up to $V+$. See the [Typical Characteristics: Table of Graphs](#) and [Application and Implementation](#) sections for additional information.

6.8 Typical Characteristics: Table of Graphs

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

Table 2. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 3
Input Bias Current vs Temperature	Figure 4
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 5
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 6
0.1-Hz to 10-Hz Noise	Figure 7
Input Voltage Noise Spectral Density vs Frequency	Figure 8
Quiescent Current vs Supply Voltage	Figure 9
Open-Loop Gain and Phase vs Frequency	Figure 10
Closed-Loop Gain vs Frequency	Figure 11
Open-Loop Gain vs Temperature	Figure 12
Open-Loop Output Impedance vs Frequency	Figure 13
Small-Signal Overshoot vs Capacitive Load	Figure 14 , Figure 15
No Phase Reversal	Figure 16
Small-Signal Step Response (100 mV)	Figure 17 , Figure 18
Large-Signal Step Response	Figure 19 , Figure 20
Large-Signal Settling Time	Figure 21 , Figure 22
Short-Circuit Current vs Temperature	Figure 23
Maximum Output Voltage vs Frequency	Figure 24
EMIRR IN+ vs Frequency	Figure 25

6.9 Typical Characteristics

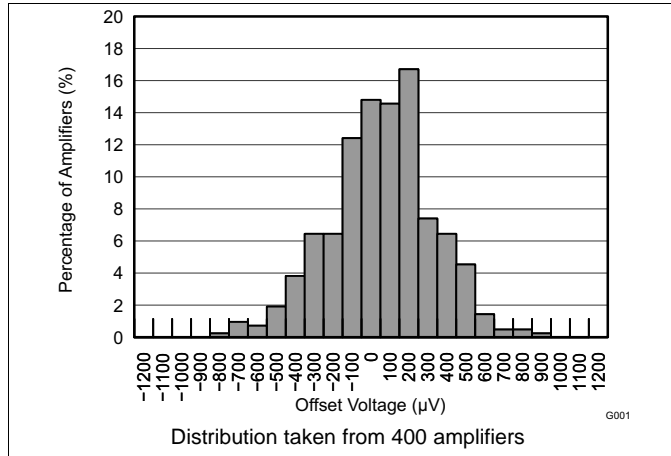


Figure 1. Offset Voltage Production Distribution

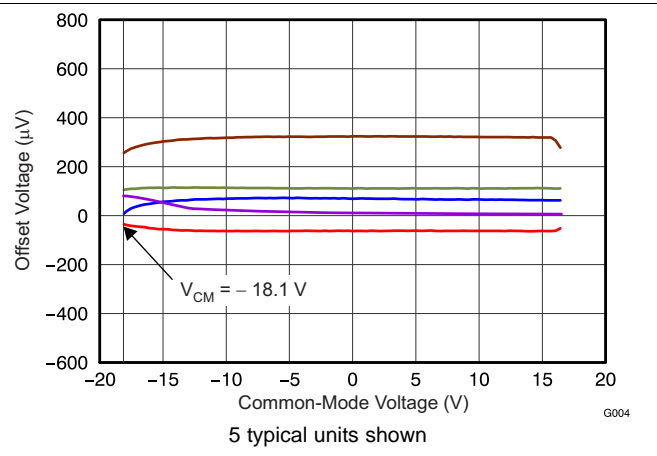


Figure 2. Offset Voltage vs Common-Mode Voltage

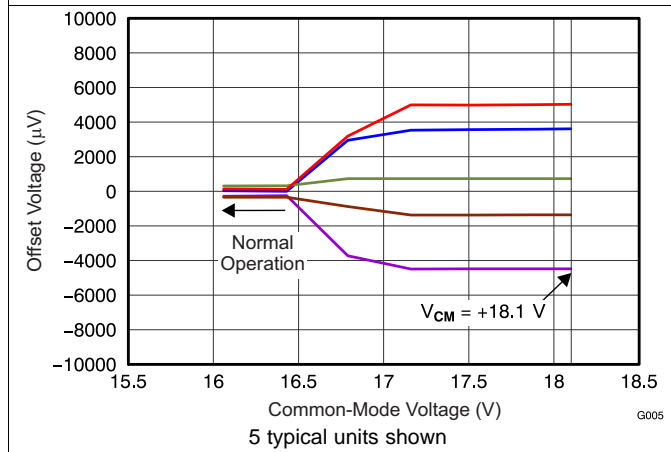


Figure 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)

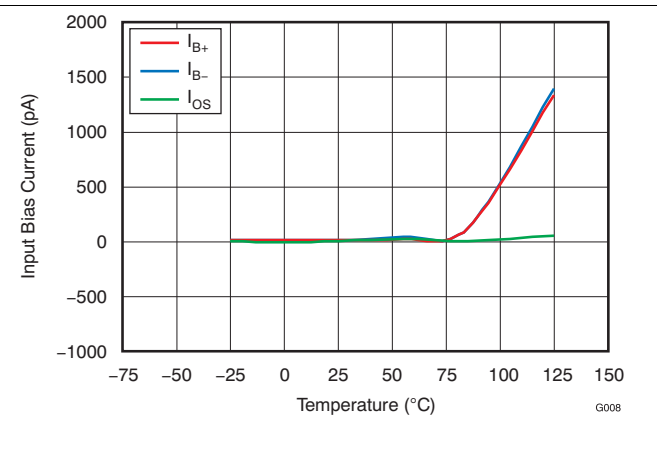


Figure 4. Input Bias Current vs Temperature

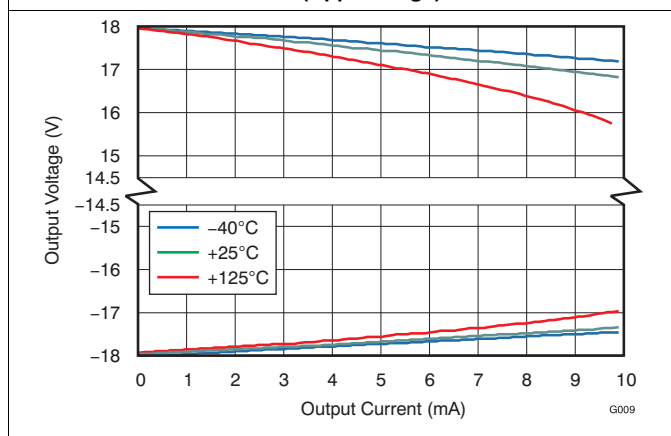


Figure 5. Output Voltage Swing vs Output Current (Maximum Supply)

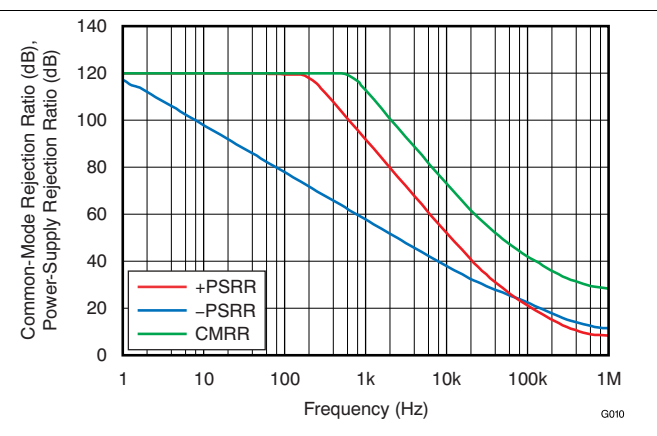
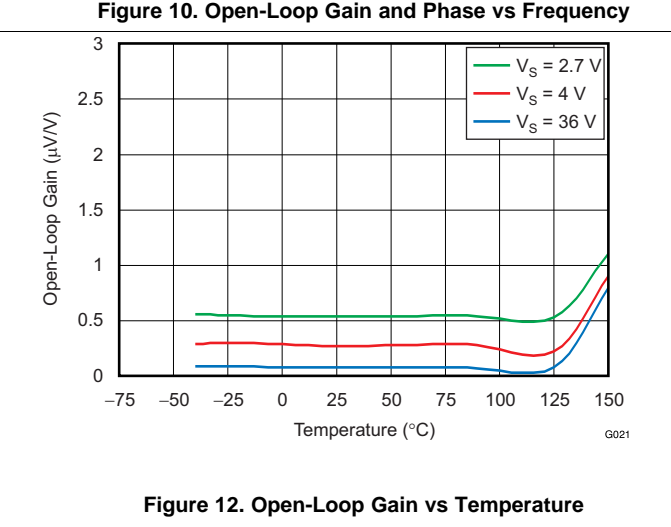
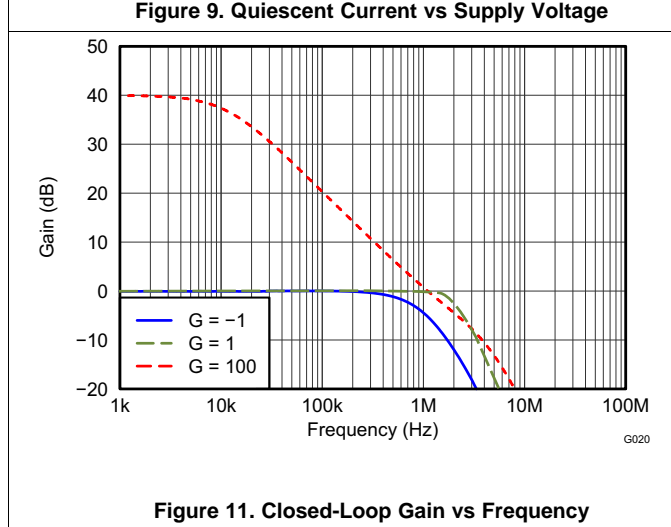
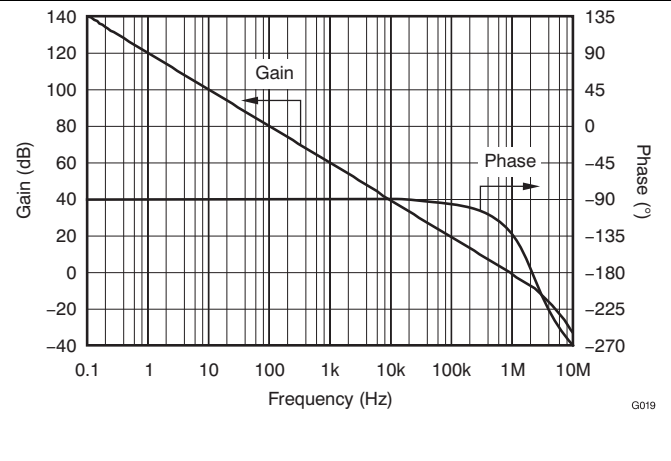
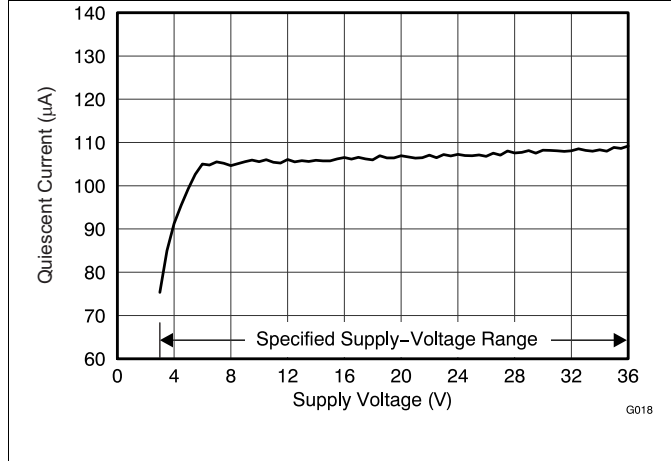
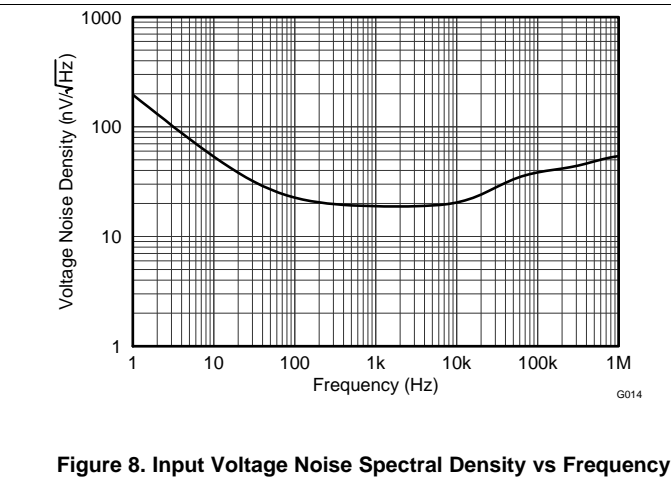
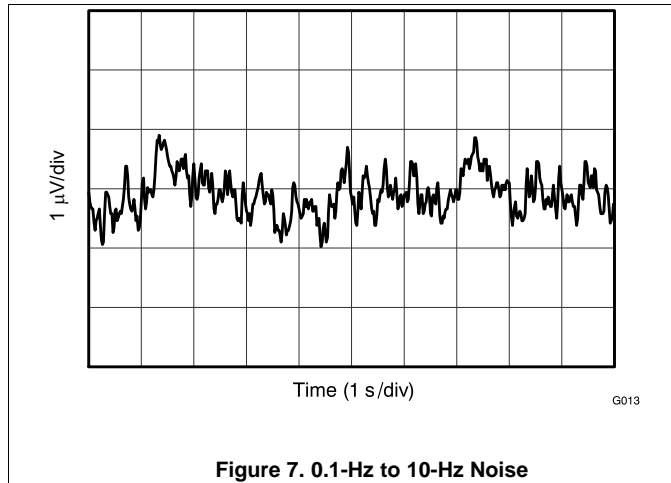
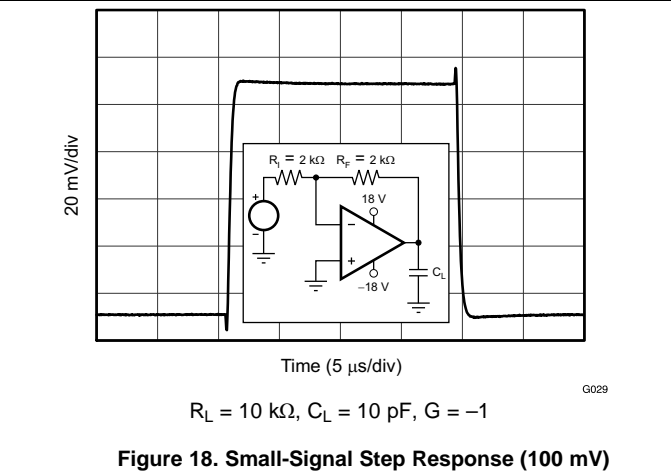
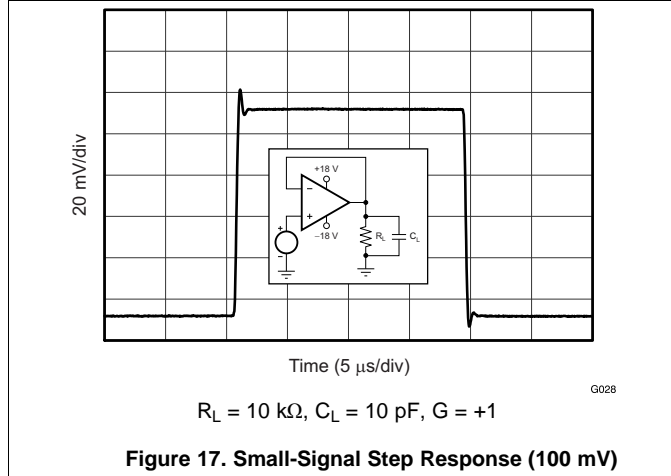
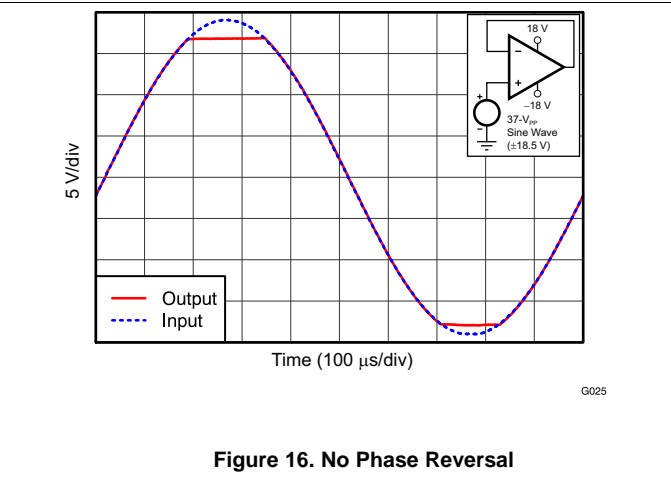
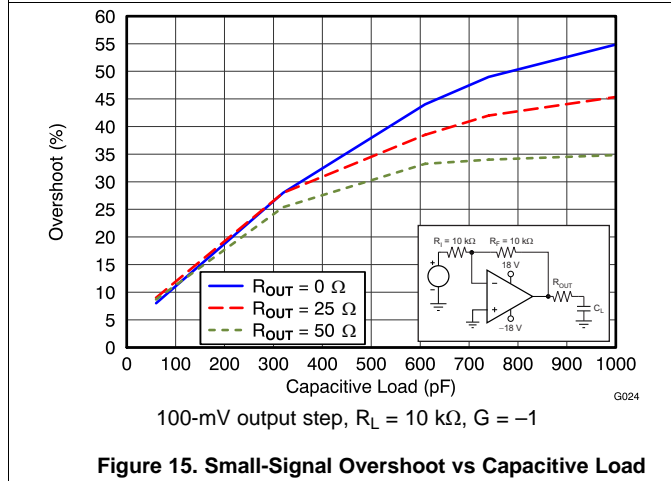
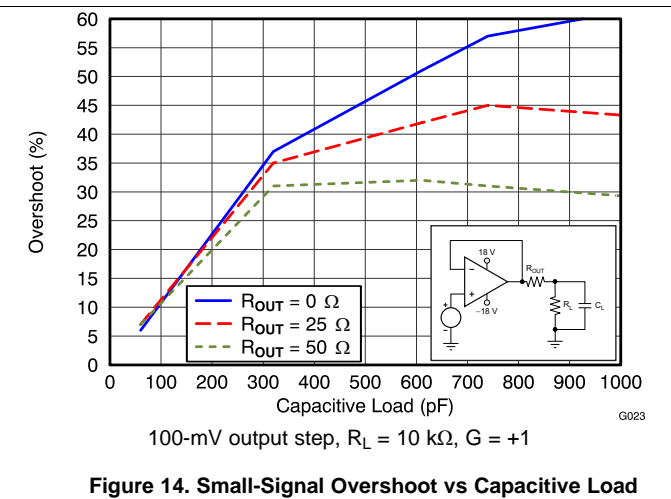
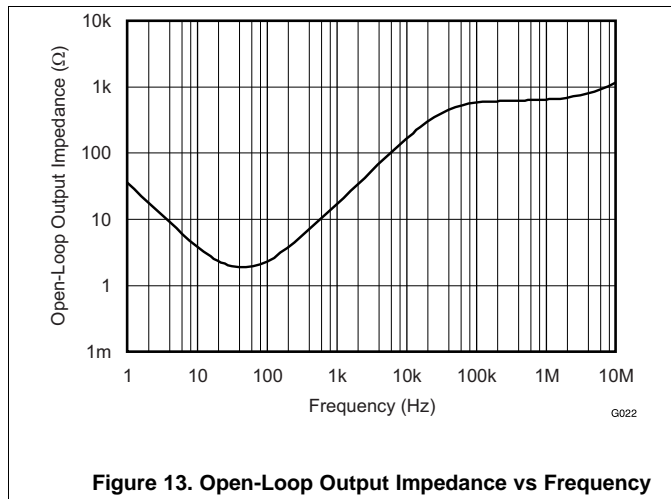


Figure 6. CMRR and PSRR vs Frequency (Referred-to Input)

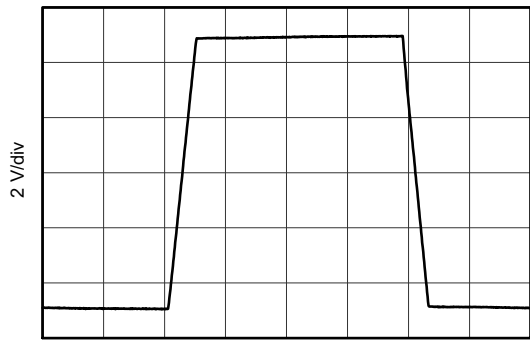
Typical Characteristics (continued)



Typical Characteristics (continued)



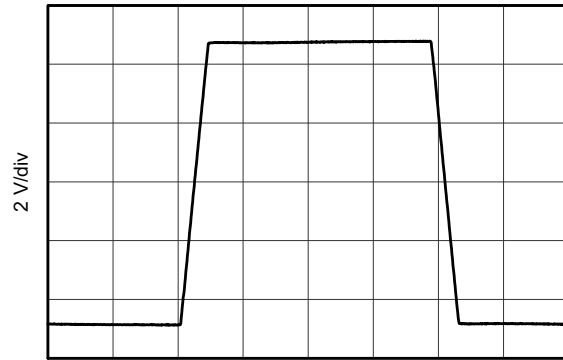
Typical Characteristics (continued)



$G = +1, R_L = 10 \text{ k}\Omega, C_L = 10 \text{ pF}$

G030

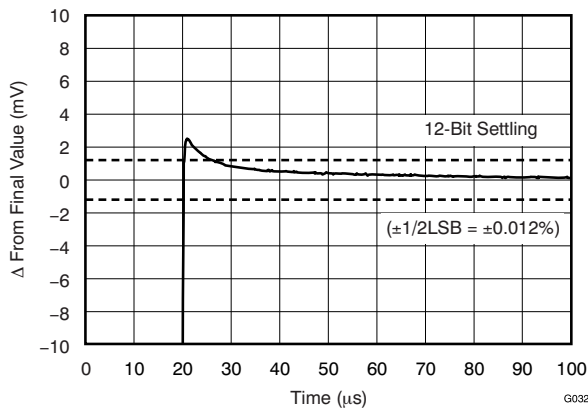
Figure 19. Large-Signal Step Response



$G = -1, R_L = 10 \text{ k}\Omega, C_L = 10 \text{ pF}$

G031

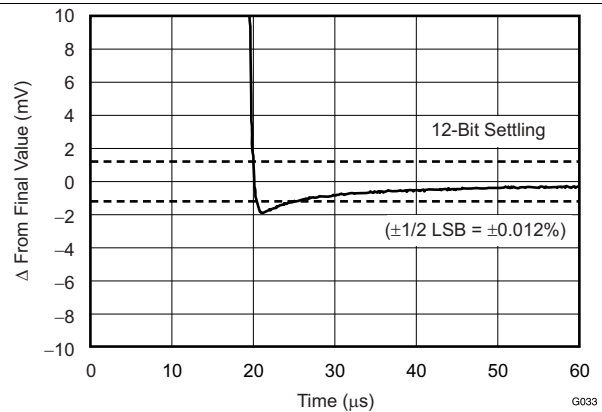
Figure 20. Large-Signal Step Response



10-V positive step, $G = +1$

G032

Figure 21. Large-Signal Settling Time



10-V negative step, $G = -1$

G033

Figure 22. Large-Signal Settling Time

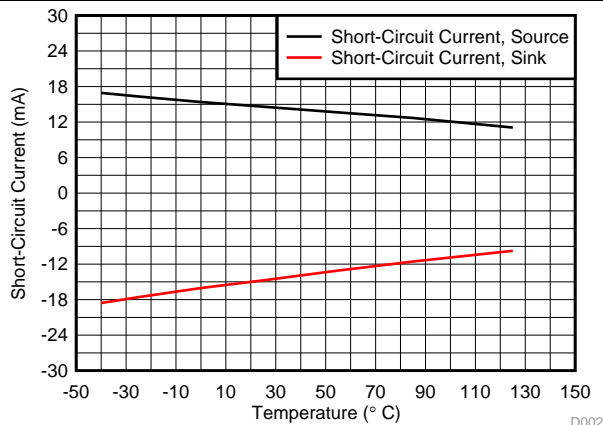


Figure 23. Short-Circuit Current vs Temperature

D002

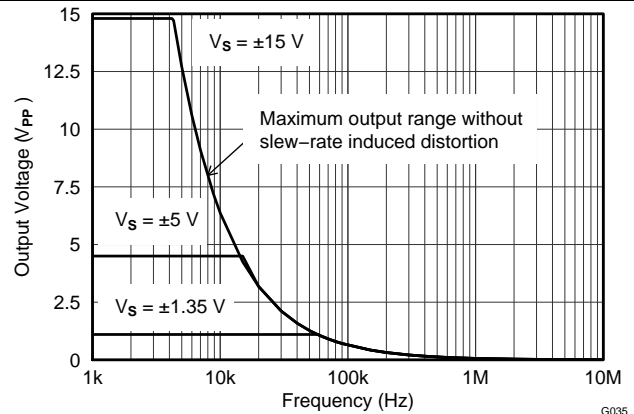
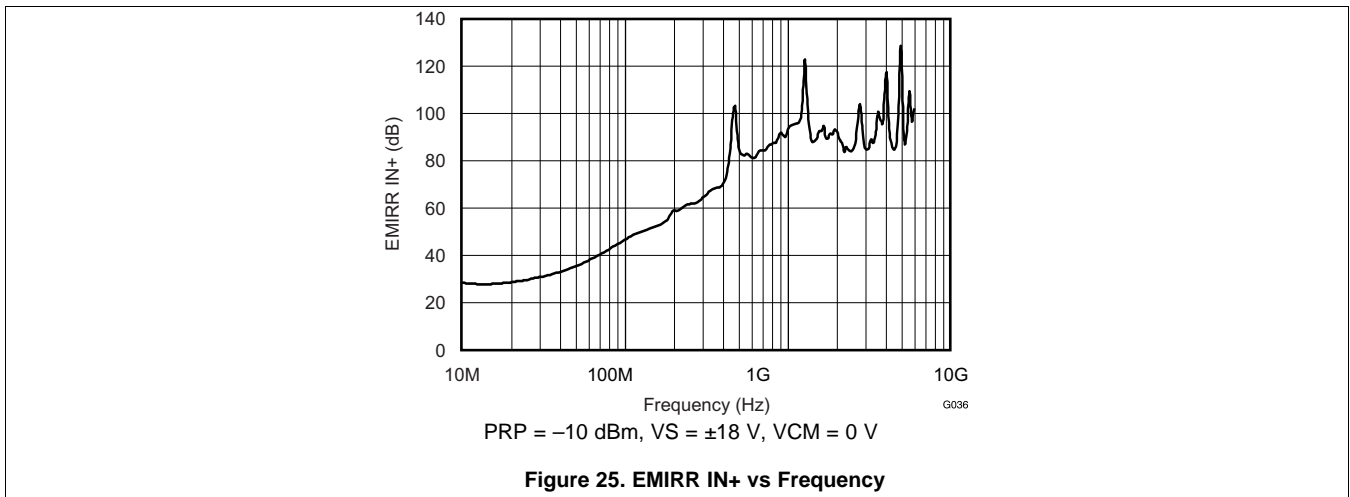


Figure 24. Maximum Output Voltage vs Frequency

G035

Typical Characteristics (continued)

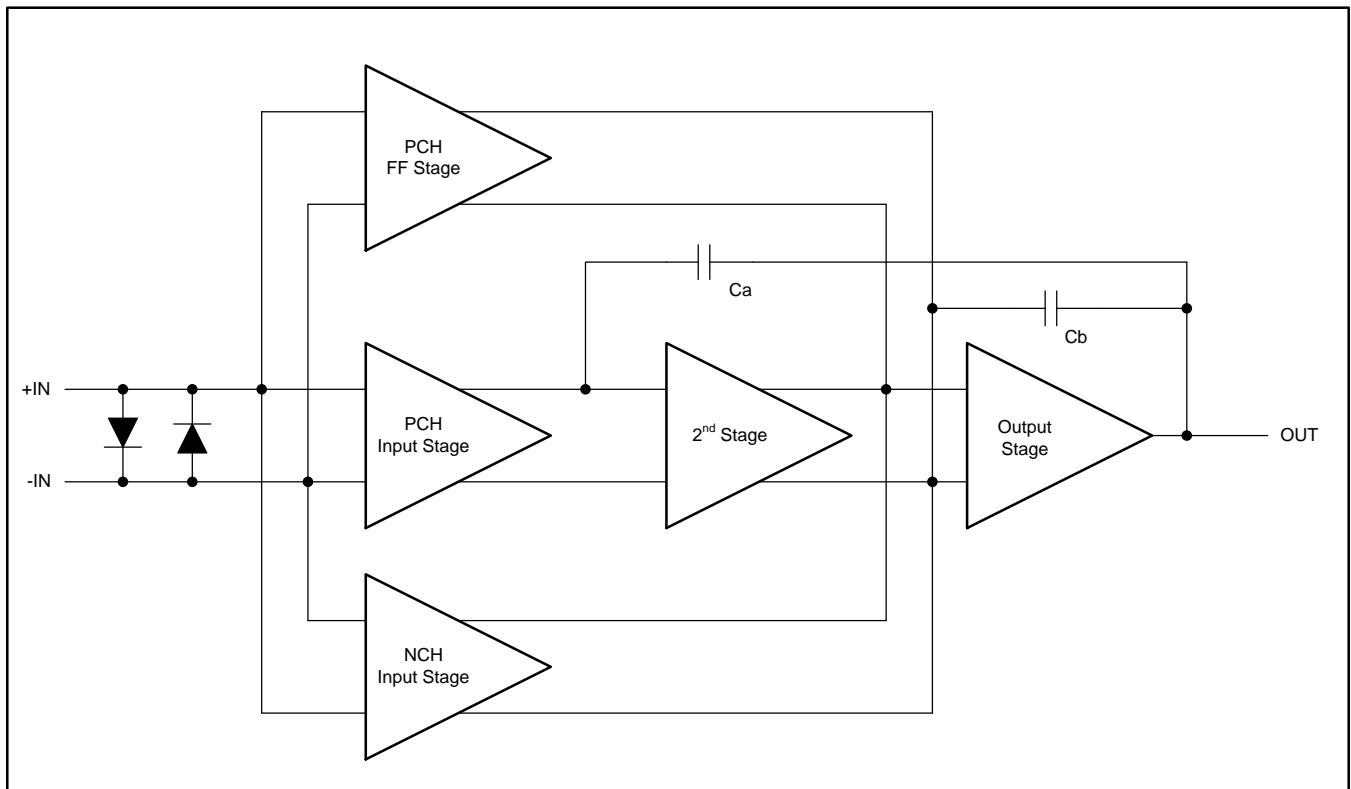


7 Detailed Description

7.1 Overview

The TLVx170 family of op amps provides high overall performance, making the devices ideal for many general-purpose applications. The excellent offset drift of only $2 \mu\text{V}/^\circ\text{C}$ provides excellent stability over the entire temperature range. In addition, the family offers very good overall performance with high CMRR, PSRR, and A_{OL} .

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The TLVx170 family of amplifiers is specified for operation from 2.7 V to 36 V (± 1.35 V to ± 18 V). Many of the specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics: Table of Graphs](#) section.

7.3.2 Phase-Reversal Protection

The TLVx170 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx170 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 26](#).

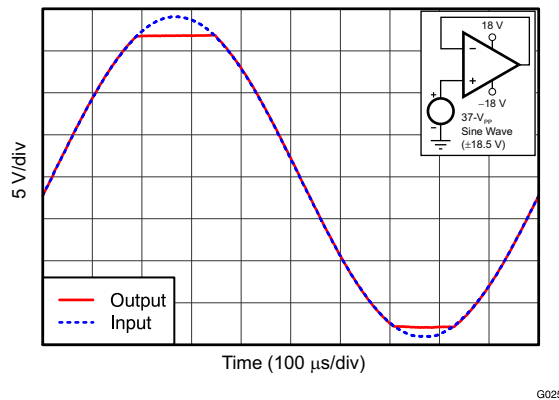


Figure 26. No Phase Reversal

7.3.3 Electrical Overstress

Designers often ask questions about the capability of an op amp to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. [Figure 27](#) illustrates the ESD circuits contained in the TLVx170 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the op amp. This protection circuitry is intended to remain inactive during normal circuit operation.

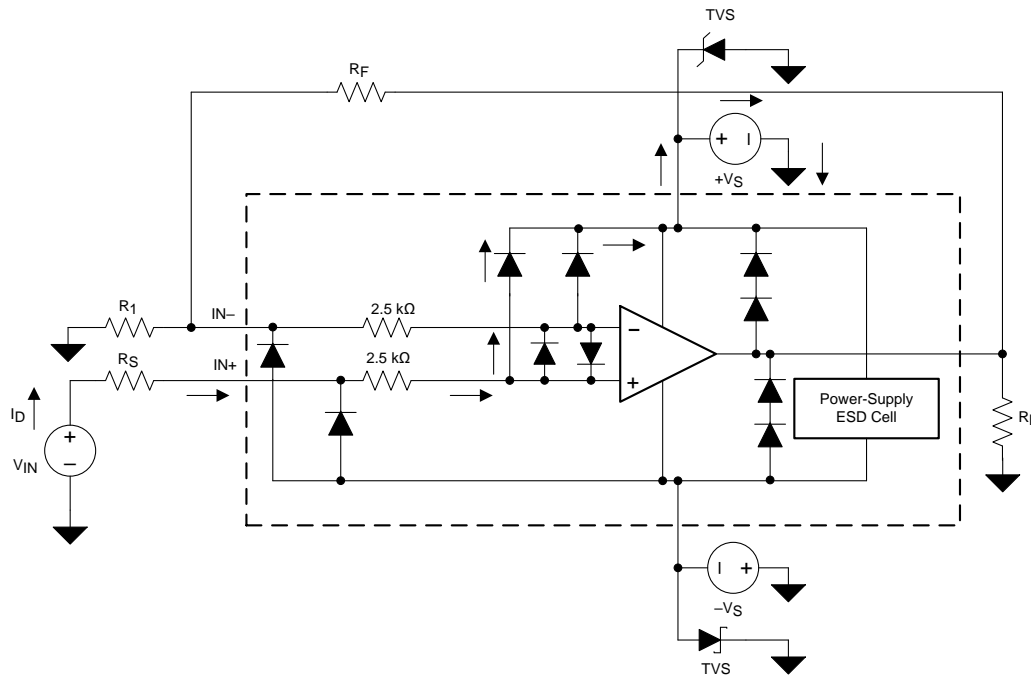
Feature Description (continued)


Figure 27. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the op amp core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLVx170 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the op amp connects into a circuit, as shown in [Figure 27](#), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

[Figure 27](#) shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($V+$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $V+$ can sink the current, then one of the upper input steering diodes conducts and directs current to $V+$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the op amp and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the op amp absolute maximum ratings.

Feature Description (continued)

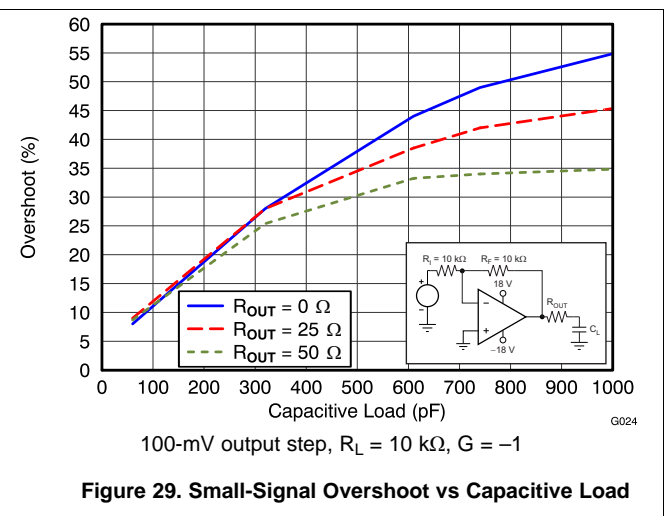
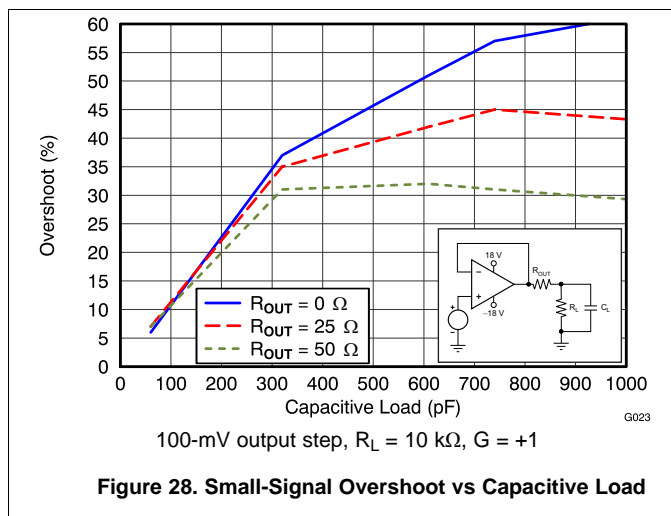
Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ($V+$ or $V-$) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the op amp current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 27](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The TLVx170 input pins are protected from excessive differential voltage with back-to-back diodes; see [Figure 27](#). In most circuit applications, the input protection circuitry has no effect. However, in low-gain or $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the TLVx170. [Figure 27](#) illustrates an example configuration that implements a current-limiting feedback resistor.

7.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLVx170 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω) in series with the output. [Figure 28](#) and [Figure 29](#) show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . Also, see the [Feedback Plots Define Op Amp AC Performance](#) application report for details of analysis techniques and application circuits.



7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx170 family extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in [Table 3](#).

Table 3. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	$(V+) - 2$		$(V+) + 0.1$	V
Offset voltage		7		mV
Offset voltage vs temperature		12		$\mu\text{V}/^\circ\text{C}$
Common-mode rejection ratio		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/ μs

7.4.2 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx170 is approximately 2 μs .

8 Application and Implementation

NOTE

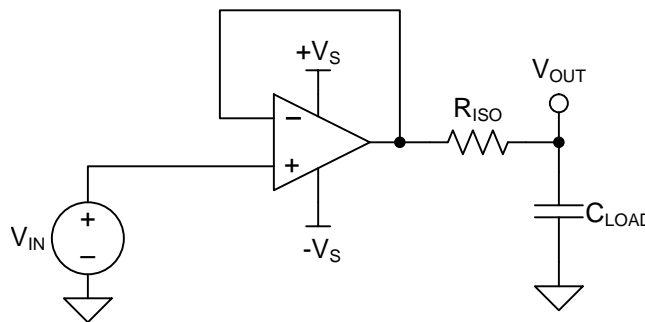
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLVx170 family of op amps provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1- μ F capacitors are adequate. Follow the additional recommendations in the [Layout Guidelines](#) section in order to achieve the maximum performance from this device. Many applications can introduce capacitive loading to the output of the amplifier (potentially causing instability). One method of stabilizing the amplifier in such applications is to add an isolation resistor between the amplifier output and the capacitive load. The design process for selecting this resistor is given in the [Typical Application](#) section.

8.2 Typical Application

This circuit can be used to drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.



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Figure 30. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (± 15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μ F, 0.1 μ F, and 1 μ F
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

[Figure 30](#) shows a unity-gain buffer driving a capacitive load. [Equation 1](#) shows the transfer function for the circuit in [Figure 30](#). Not shown in [Figure 30](#) is the open-loop output resistance of the op amp, R_o .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in [Equation 1](#) has a pole and a zero. The frequency of the pole (f_p) is determined by $(R_o + R_{ISO})$ and C_{LOAD} . Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and $1/\beta$ is 20 dB per decade; see [Figure 31](#). The $1/\beta$ curve for a unity-gain buffer is 0 dB.

Typical Application (continued)

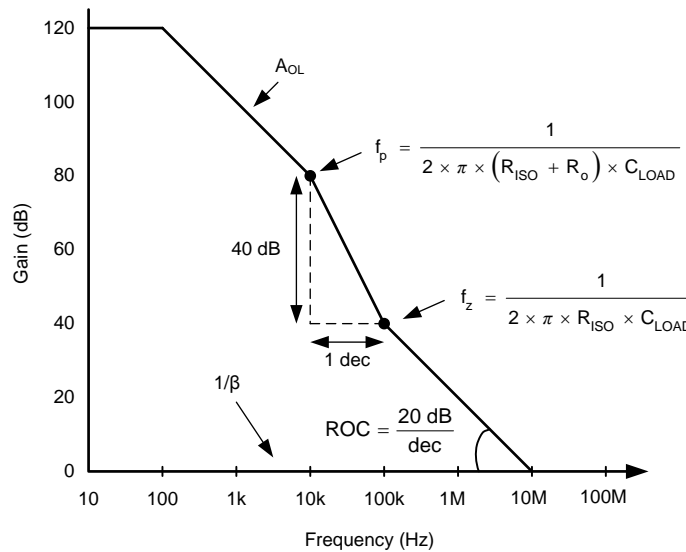


Figure 31. T1PD128 Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 4 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLV170, see the [Capacitive Load Drive Solution Using an Isolation Resistor](#) precision design.

Table 4. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45° and 60° for various capacitive loads were determined. The results are shown in Figure 32.

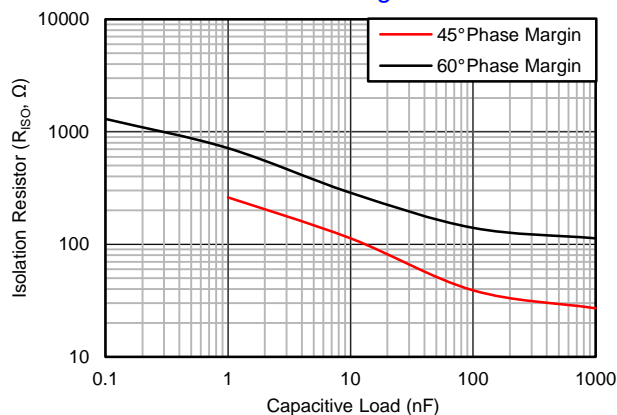


Figure 32. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

9 Power Supply Recommendations

The TLVx170 is specified for operation from 2.7 V to 36 V (± 1.35 V to ± 18 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics: Table of Graphs](#) section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 34](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

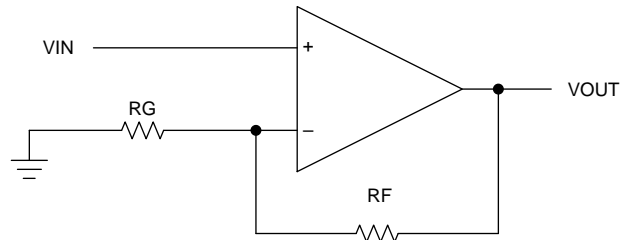


Figure 33. Schematic Representation

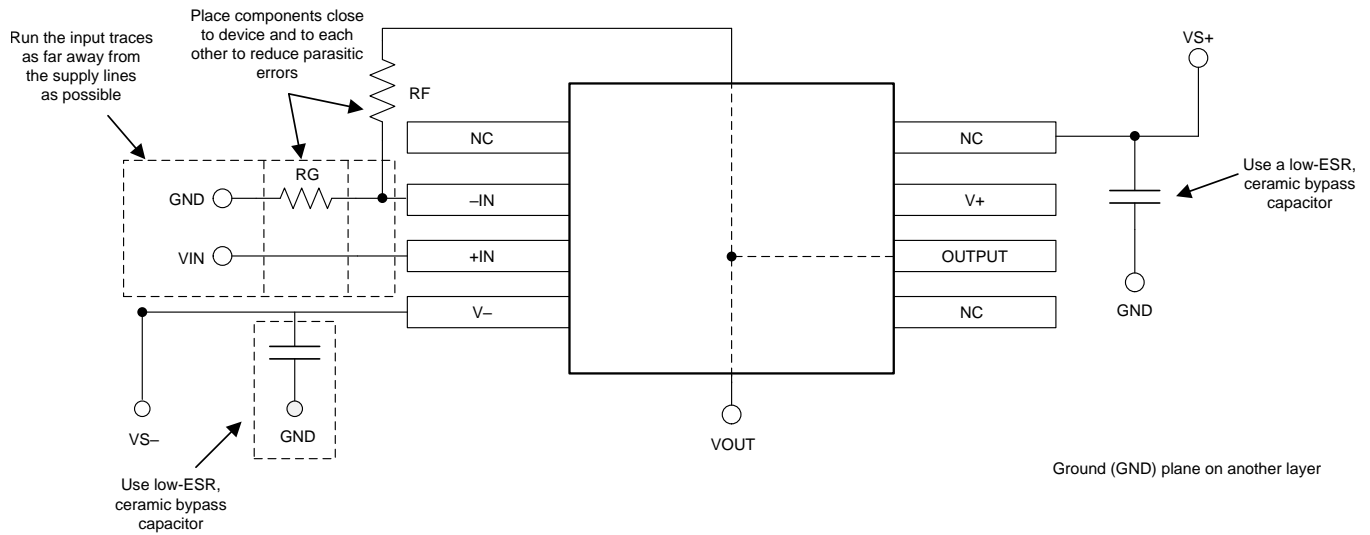


Figure 34. Op Amp Board Layout for a Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA-TI™ software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or the TINA-TI™ software be installed. Download the free TINA-TI™ software from the [TINA-TI™ folder](#).

11.1.1.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface-mount devices. The evaluation tool uses these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5, and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP adapter EVM can also be used with terminal strips or can be wired directly to existing circuits.

11.1.1.3 Universal Op Amp EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP, and SOT23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the universal op amp EVM.

11.1.1.4 TI Precision Designs

TI precision designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, a complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI precision designs are available online at www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer

The [WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI op amps and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® design center, the WEBENCH® filter designer allows complete multistage active filter solutions to be designed, optimized, and simulated within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

[Feedback Plots Define Op Amp AC Performance](#) (SBOA015)

11.3 Related Links

[Table 5](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV170	Click here	Click here	Click here	Click here	Click here
TLV2170	Click here	Click here	Click here	Click here	Click here
TLV4170	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.

11.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV170IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14QT	Samples
TLV170IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14QT	Samples
TLV170IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV170	Samples
TLV2170IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14NV	Samples
TLV2170IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14NV	Samples
TLV2170IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL2170	Samples
TLV4170ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLV4170	Samples
TLV4170IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLV4170	Samples
TLV4170IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4170	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV170IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV170IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV170IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2170IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2170IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2170IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4170IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4170IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV170IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
TLV170IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
TLV170IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV2170IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2170IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV2170IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV4170IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV4170IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

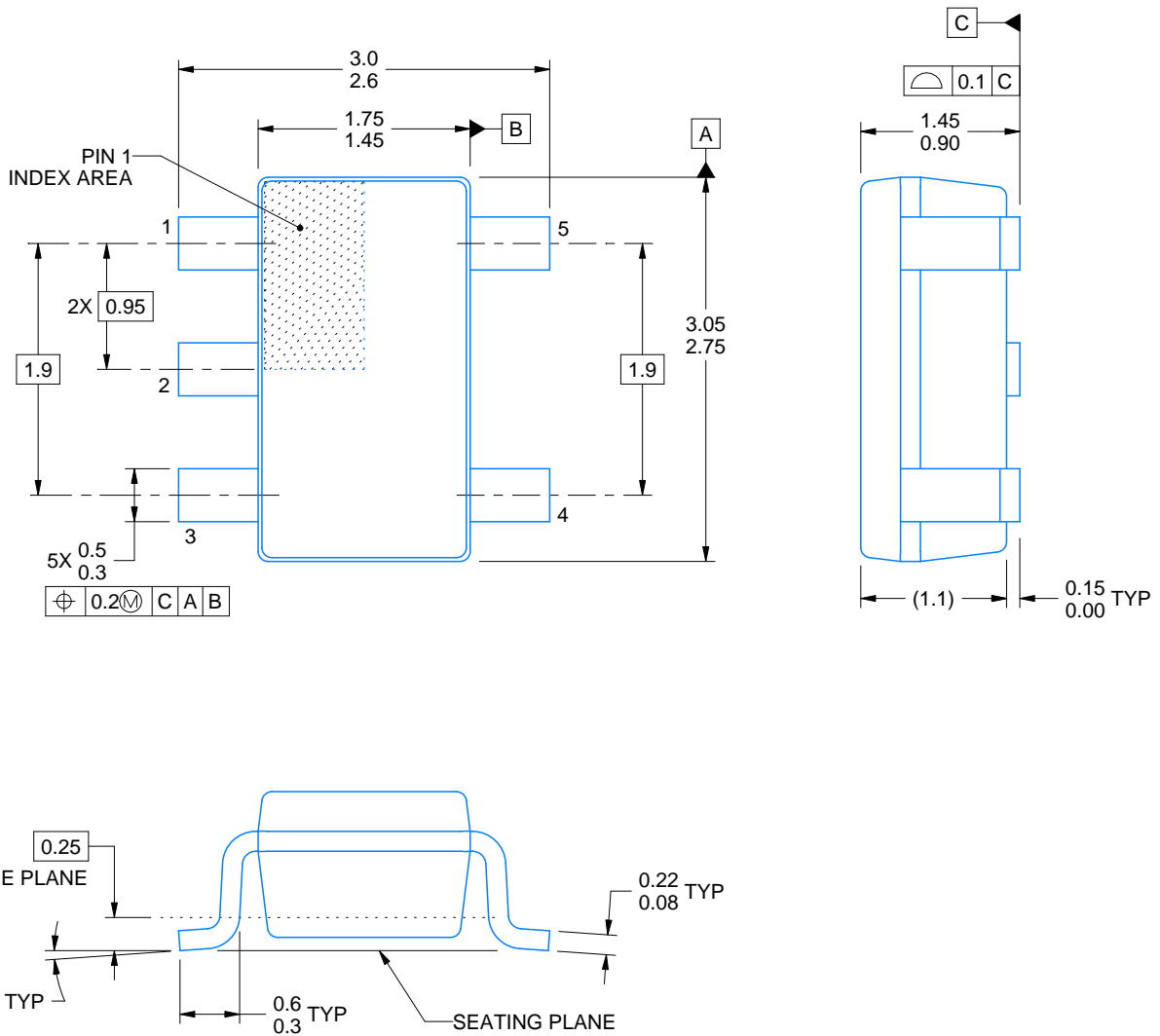


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

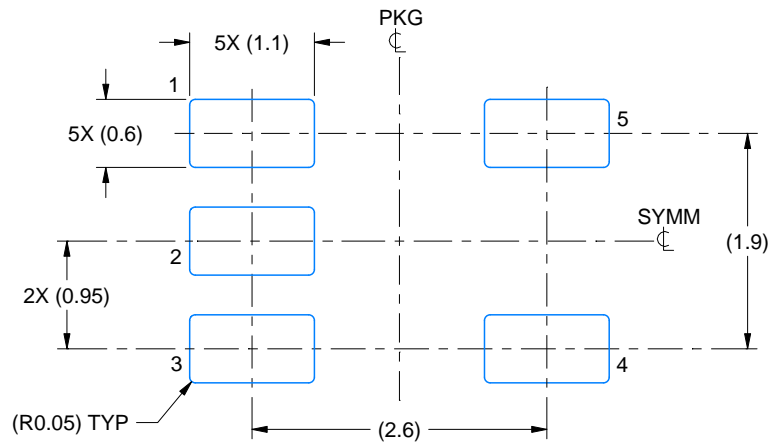
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

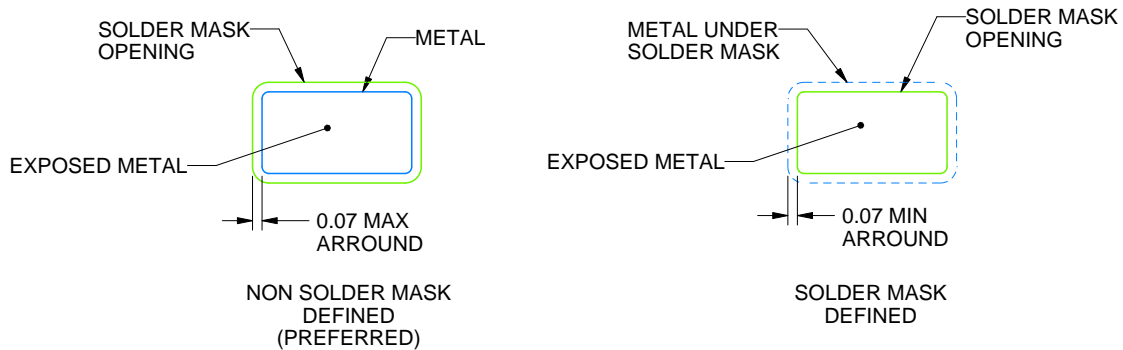
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

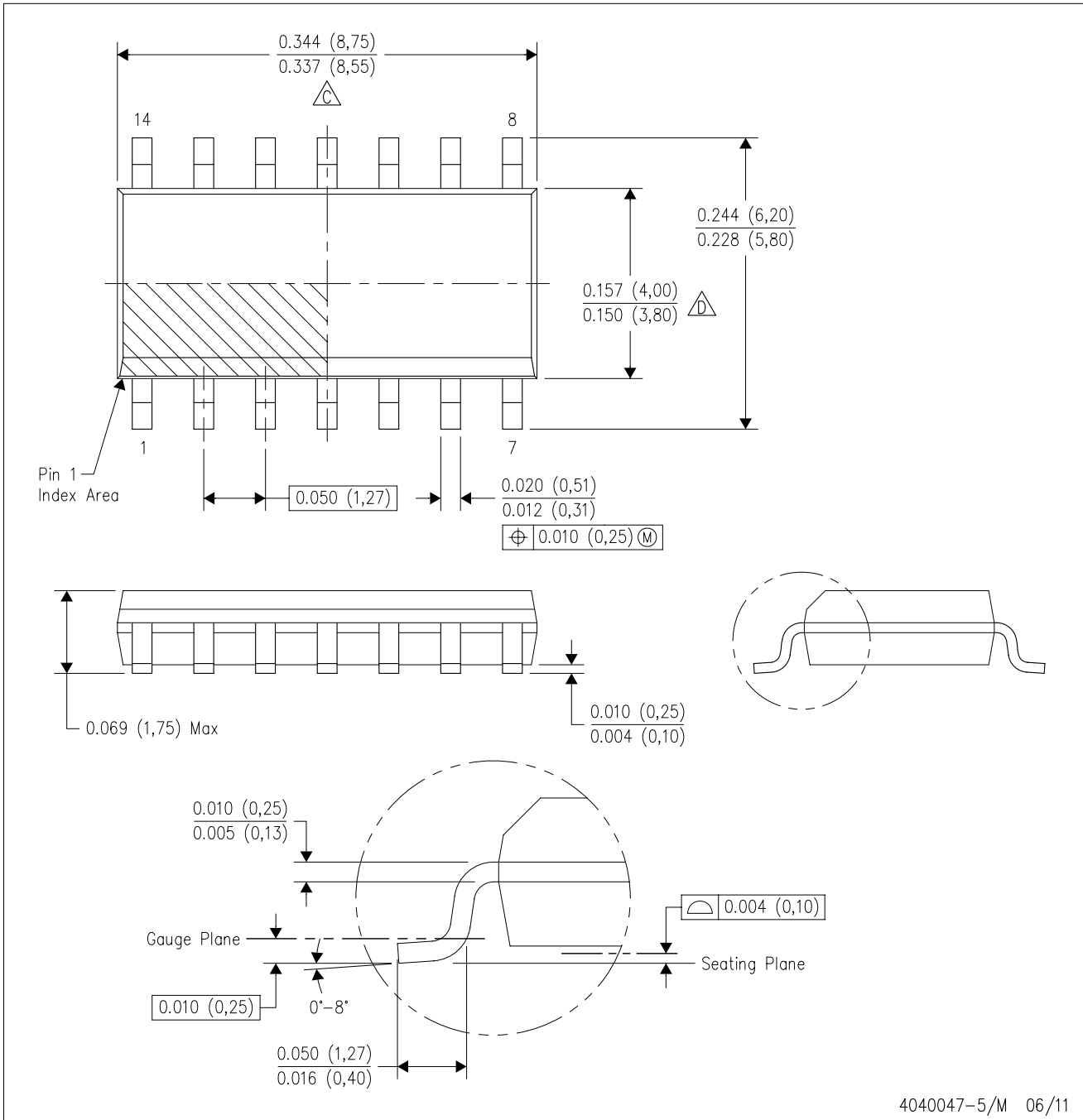
4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

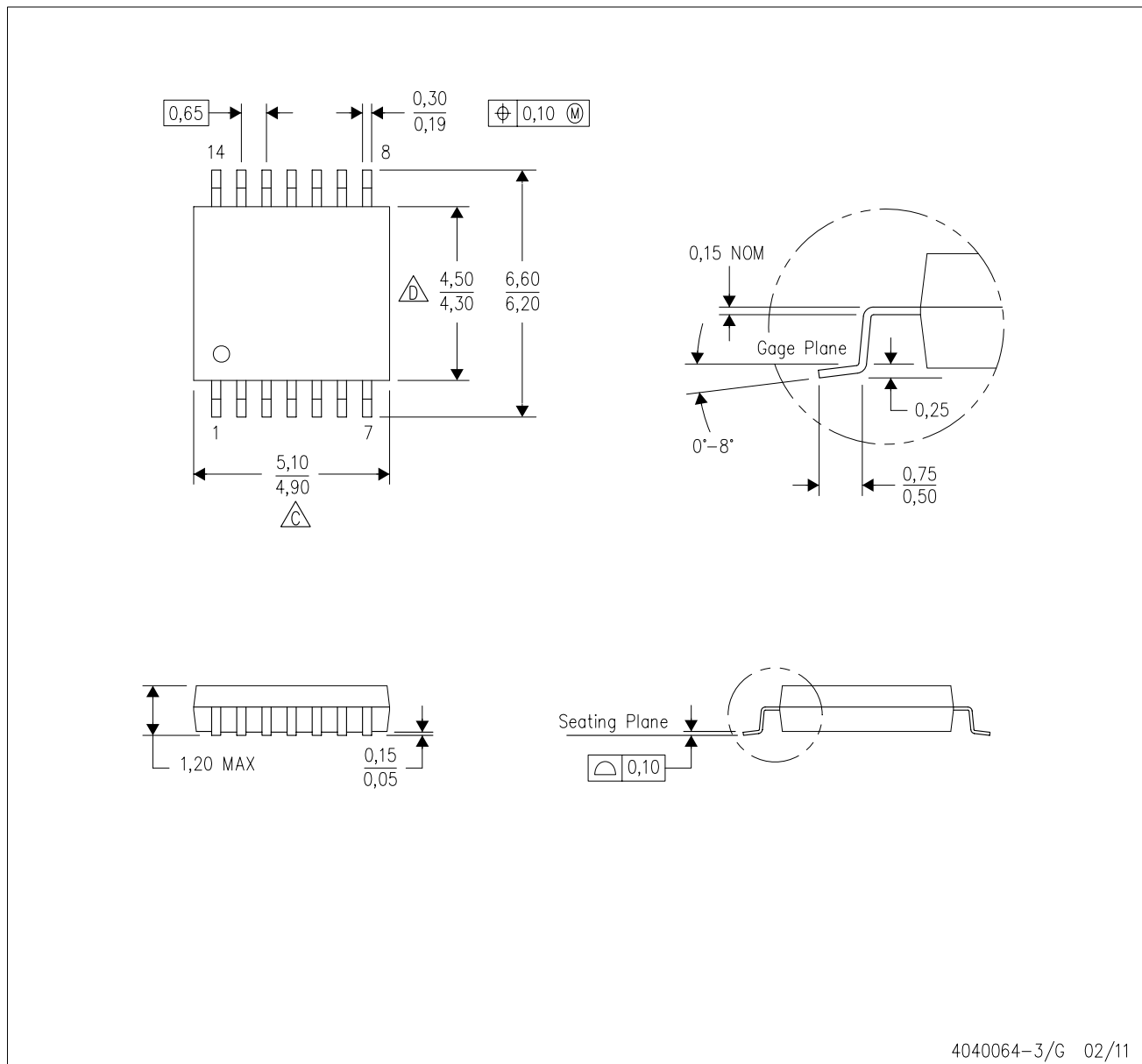


4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

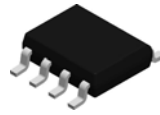
PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

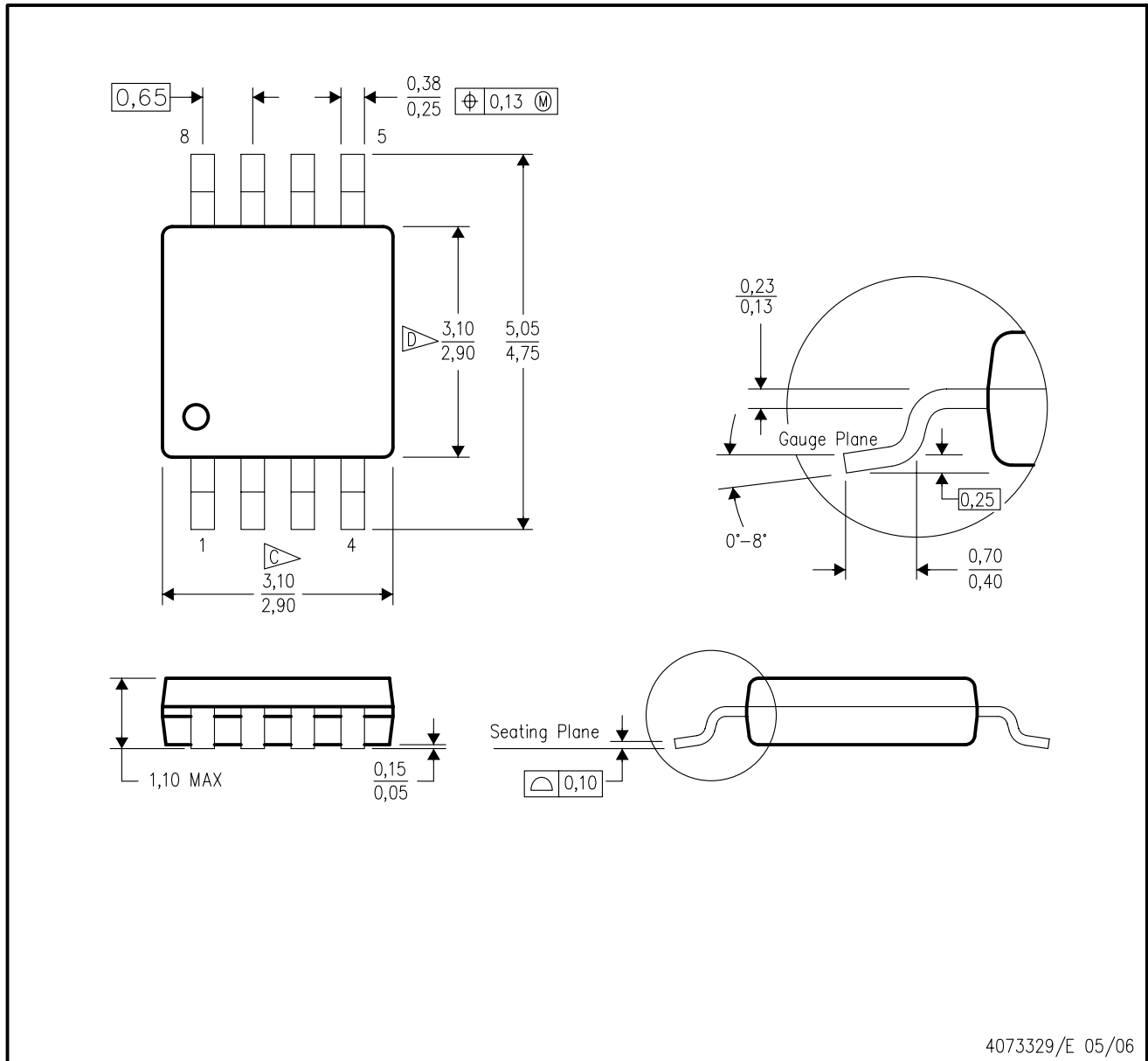
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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