Autonomous Audio Headset Switch with Reduced GND Switch R_{ON} and FM Capability

Check for Samples: TS3A226AE

FEATURES

- **Ground FET Switches (60mΩ typical)**
- **Autonomous Detection of Headset Types: 3-Poles or 4-Poles (with MIC on SLEEVE or RING2)**
- **Microphone Line Switches**
- **Supports FM Signal Transmission Through the Ground FETs**
- **Reduction of Click/Pop Noise**
- **VDD Range: 2.6 V – 4.7 V**
- **THD (Mic): 0.002% Typical**
- **Low Current Consumption: 6.5-µA Typical**
- **±8kV Contract Discharge (IEC 61000-4-2) ESD Performance on SLEEVE and RING2 Pins**

APPLICATIONS

- **Mobile Phones / Tablet PCs**
- **Notebook/Ultrabook Computers**

DESCRIPTION

The TS3A226AE is an audio headset switch that detects 3- or 4-pole 3.5mm accessories. For a 4-pole accessory with a microphone, the TS3A226AE also detects the MIC location and routes the microphone and ground signals automatically. The ground signal is routed through a pair of low-impedance ground FETs (60mΩ typical), resulting minimal impact on audio cross-talk performance. The autonomous detection feature allows end users to plug in accessories with different audio pole configurations into the mobile device and have them operate properly with no added software control and complexity. The ground FETs of the device are designed to allow FM signal pass-through, making it possible to use the ground line of the headset as an FM antenna in mobile audio application.

The TS3A226AE is packaged within a 1.2mm × 1.2mm WCSP package, making it suitable for use in mobile application.

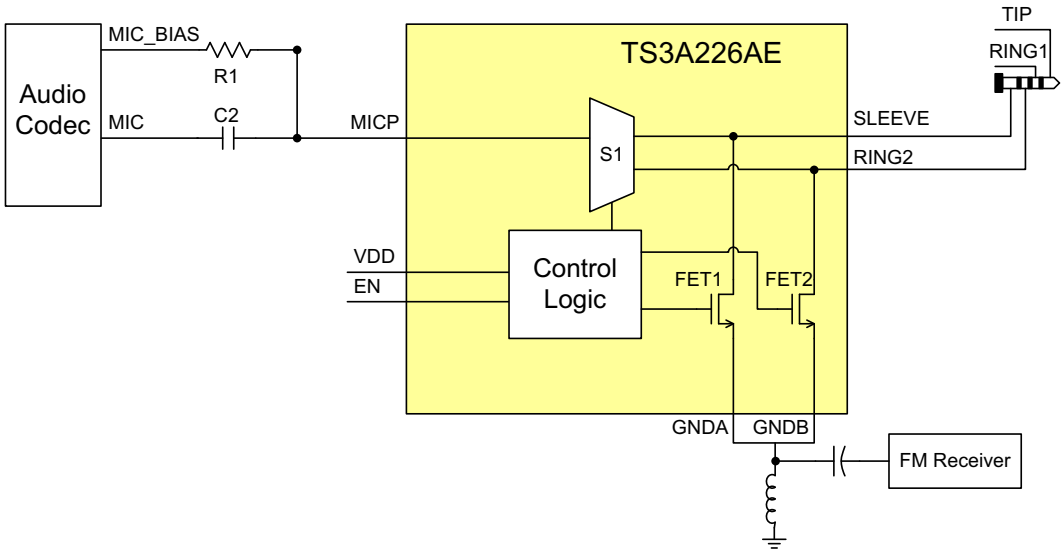


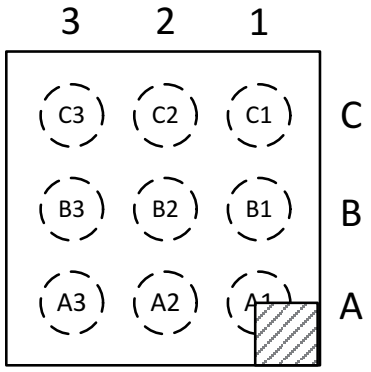
Figure 1. Typical Application Diagram

ORDERING INFORMATION

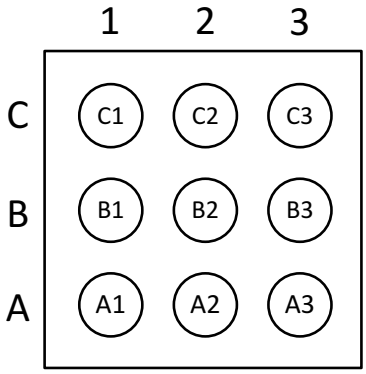
For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE; YFF-WCSP



Top View/Footprint



Bump View

Die Size: 1.2mm ×1.2mm
Bump Size: 0.25mm
Bump Pitch: 0.4mm

TS3A226AE Pin Mapping (Top View)

	3	2	1
C	GND	TIP	EN
B	SLEEVE	GNDA	MICp
A	RING2	GNDB	VDD

PIN FUNCTIONS

PIN			DESCRIPTION
NUMBER	NAME	TYPE	
A1	VDD	Supply	Power supply for the chip.
A2	GNDB	Ground	FET2 ground reference.
A3	RING2	I/O	Connected to the RING2 segment of the jack. The pin will be routed automatically by TS3A226AE to either MICp or GNDB depending on the type of accessory.
B1	MICp	I/O	Microphone signal connection to codec. Microphone bias should be fed into this pin.
B2	GNDA	Ground	FET1 ground reference.
B3	SLEEVE	I/O	Connected to the SLEEVE segment of the jack. The pin will be routed automatically by TS3A226AE to either MICp or GNDA depending on the type of accessory.
C1	EN	Input	A rising edge triggers the detection sequence. This pin can be connected to the headset jack to allow automatic pull-up to supply after headset insertion.
C2	TIP	I/O	Connected to the TIP segment of the headphone jack.
C3	GND	Ground	Chip ground reference.

S1 MUX DETAIL

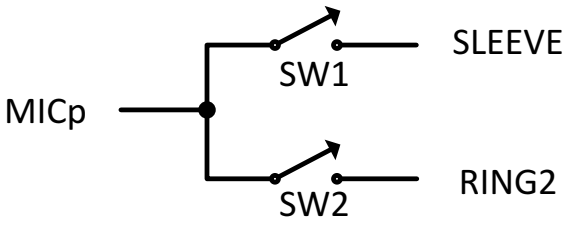


Figure 2. S1 Mux Detail

FUNCTIONAL TABLES: INTERNAL SWITCHES

EN	Accessory Type	Accessory Configuration	SW1	SW2	FET1	FET2
0	N/A	—	High Z	High Z	High Z	High Z
1	TRS 3-pole Headphone or Speaker	TIP = Audio Left Ring = Audio Right Sleeve = **Ground**	On	On	On	On
1	TRRS 4-pole Headphone	TIP = Audio Left Ring1 = Audio Right Ring2 = **Ground** Sleeve = **Microphone**	On	High Z	High Z	On
1	TRRS 4-pole Headphone	TIP = Audio Left Ring1 = Audio Right Ring2 = **Microphone** Sleeve = **Ground**	High Z	On	On	High Z
1	N/A	—	On	On	On	On

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_I	Voltage range on VDD(2)	–0.3 to 5	V
	Voltage range on EN, MICP, RING2, SLEEVE, TIP(2)	–0.3 to V_{DD}+0.5	V
T_A	Operating ambient temperature range(3)	–40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD rating	Charge device model (JESD 22 C101)	500	V
	Human body model(JESD 22 A114)	2	kV
	Contact discharge on RING2, SLEEVE, TIP (IEC 61000-4-2)	8	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		2.6	4.5	V
V_{IO}	Input/Output voltage range (EN, MICP, RING2, SLEEVE, TIP)		0	V_{DD}	V
$V_{IO(TIP)}$	Input/Output voltage range for TIP		-2.0	V_{DD}	V
V_{IH}	Input Logic High for EN	VDD = 2.6 V	1.16	V_{DD}	V
		VDD = 3.3 V	1.24	V_{DD}	
		VDD = 4.5 V	1.48	V_{DD}	
V_{IL}	Input Logic Low for EN	VDD = 2.6 V	0	0.19	V
		VDD = 3.3 V	0	0.3	
		VDD = 4.5 V	0	0.5	
T_A	Operating temperature range		–40	85	°C

KEY ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temperature –40°C ≤ T_A ≤ 70°C. Typical values are for V_{DD} = 3.3V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input Voltage Range		2.6	3.3	4.5	V
I_{DD}	Quiescent Current	V_{DD} = 4.5 V, V_{MICp} = 1.8 V to V_{DD}, EN=L or EN=H (after detection)		6.5	14	µA
SWITCH RESISTANCE						
R_{F1}	FET1 On Resistance	V_{DD} = 2.6 V, V_{GND} = 0 V, I_{GND} = 10 mA		60	85	mΩ
R_{F2}	FET2 On Resistance			60	85	
R_{SW1}	SW1 On Resistance	V_{DD} = 2.6 V, $V_{SLEEVE/RING2}$ = 0 V to 2.6 V, I_{MIC} = ±10 mA		8.5	10.5	Ω
R_{SW2}	SW2 On Resistance			8.5	10.5	
SWITCH LEAKAGE CURRENT						
$I_{OFF-0.1}$	FET1 and FET2 off leakage	V_{IN} = 0 V to 2.6 V, V_{OUT} = 0 V, V_{DD} = 4.5 V			1	µA
I_{OFF-10}	SW1, SW2 off leakage				1	
I_{ON-10}	SW1, SW2 on leakage				1	
SWITCH DYNAMIC CHARACTERISTICS						
BW_{F1}	FET1 Bandwidth	V = 60 mV_{PP}, I_{bias} = 10 mA	160	200		MHz
BW_{F2}	FET2 Bandwidth		160	200		
PSR_{217}	Power Supply Rejection, R_L = 50 Ω	V = 200 mV_{PP}, f = 217 Hz		–110		dB
PSR_{1k}		V = 200 mV_{PP}, f = 1 kHz		–100		dB
PSR_{20k}		V = 200 mV_{PP}, f = 20 kHz		–85		dB
ISO_{S1}	SLEEVE or RING2 to MICP Isolation	V = 200 mV_{PP}, f = 20 kHz, R_L = 50 Ω		–80		dB
SEP_{S1}	SLEEVE to RING2 Separation	V = 200 mV_{PP}, f = 20 kHz, R_L = 50 Ω (see Figure 5)		–80		dB
THD_{10}	Total Harmonic Distortion	V = 10 mV_{PP}, f = 20-20 kHz, R_S = 600 Ω		0.01%		
THD_{200}		V = 200 mV_{PP}, f = 20-20 kHz, R_S = 600 Ω		0.002%		
TIMING CHARACTERISTICS						
t_{dect}	Total detection time	From EN=H to S1 switch(es) closing		180		ms

TYPICAL CHARACTERISTICS

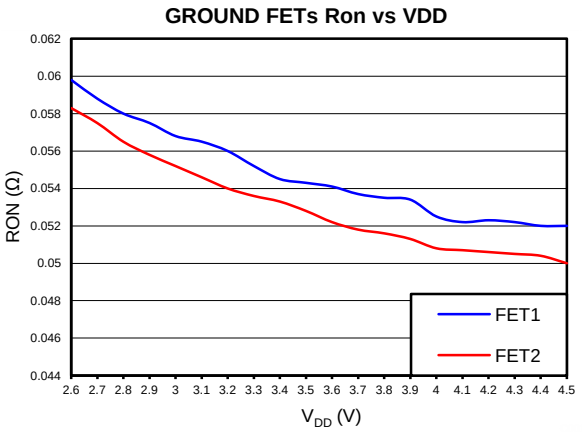


Figure 3.

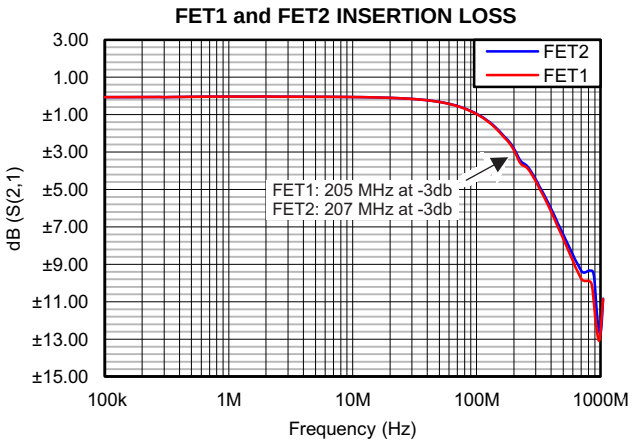


Figure 4.

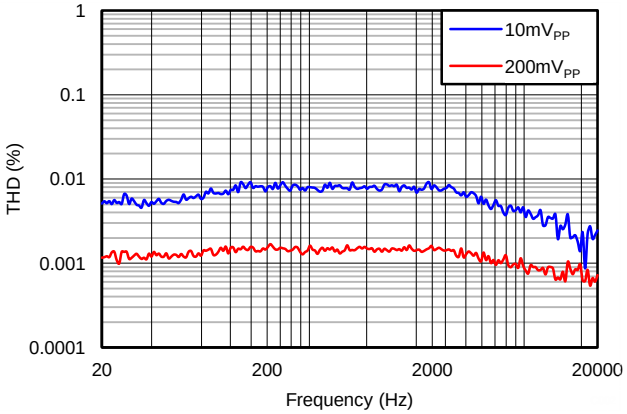


Figure 5.

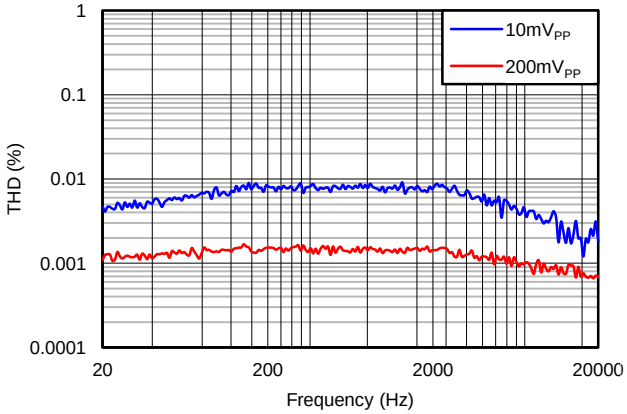


Figure 6.

REVISION HISTORY

Changes from Original (June 2013) to Revision A **Page**

- Removed Machine Model ESD specification. 3
- Added EN=L or EN=H (after detection) to I_{DD} TEST CONDITIONS. 4
- Added typical values to R_{SW1} and R_{SW2}. 4
- Added t_{dect} PARAMETER to KEY ELECTRICAL CHARACTERISTICS table. 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A226AEYFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YP2 26AE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

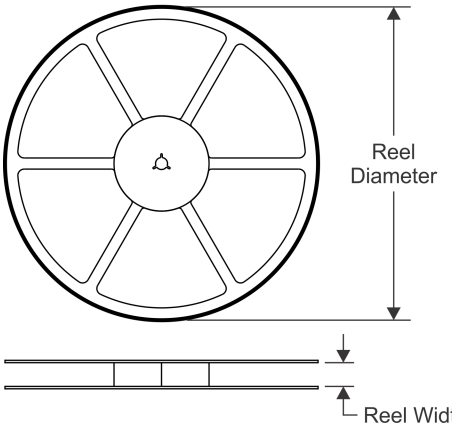
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

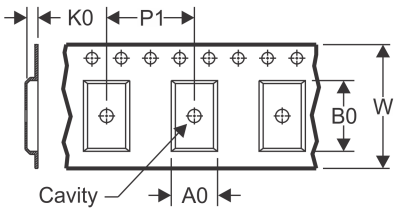
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

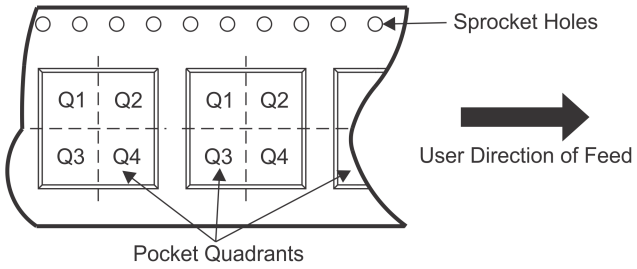


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

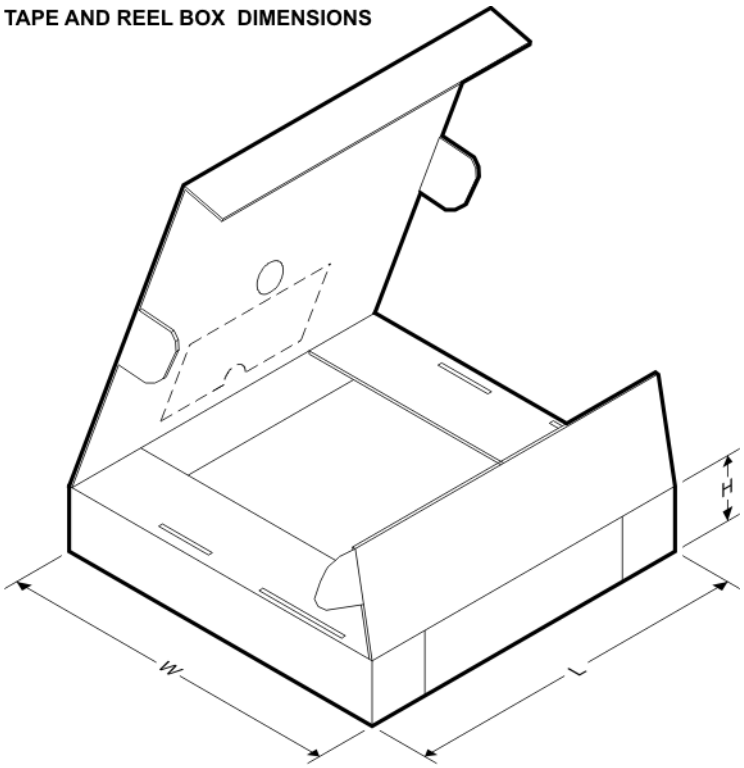
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A226AEYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.46	1.36	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

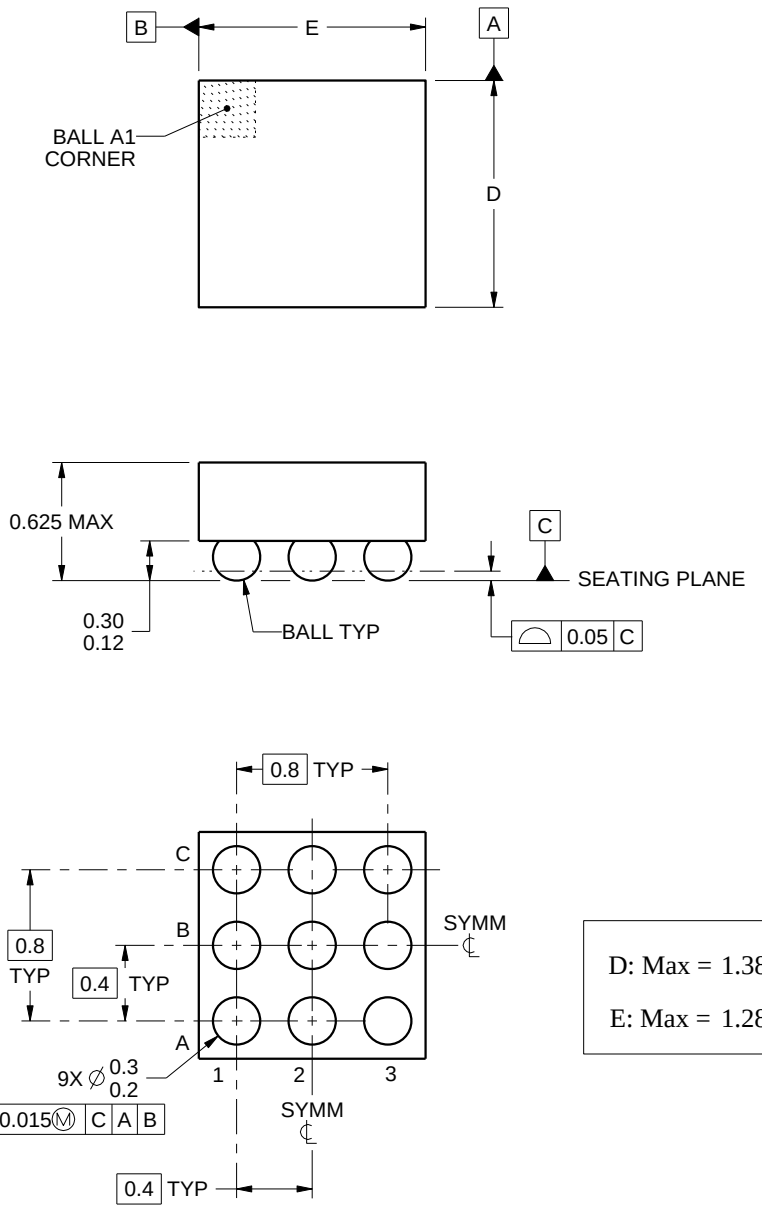
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A226AEYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.386 mm, Min =1.326 mm

E: Max = 1.286 mm, Min =1.226 mm

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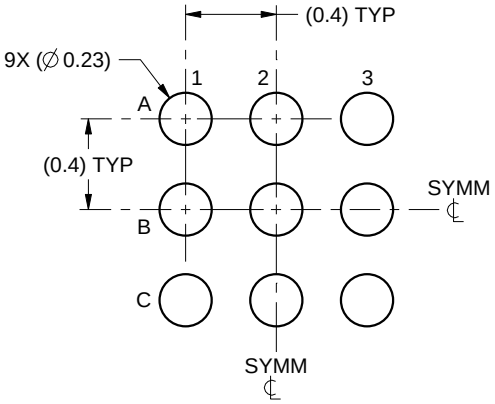
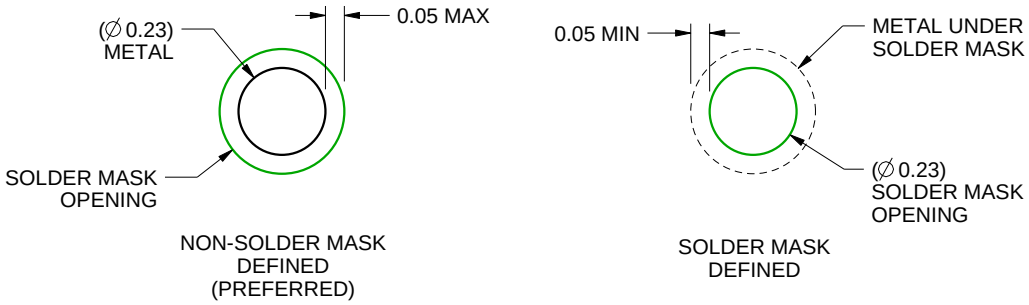
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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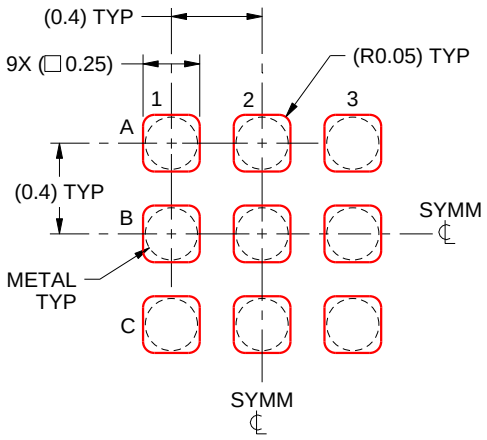
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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