LP5910 300-mA Low-Noise, Low-I_Q LDO

1 Features

- Input Voltage Range: 1.3 V to 3.3 V
- Output Voltage Range: 0.8 V to 2.3 V
- Output Current: 300 mA
- PSRR: 75 dB at 1 kHz
- Output Voltage Tolerance: ±2%
- Low Dropout: 120 mV (Typical)
- Very Low I_Q (Enabled, No Load): 12 µA
- Low Output-Voltage Noise: 12 μV_{RMS}
- Stable with Ceramic Input and Output Capacitors
- Thermal Overload Protection
- Short-Circuit Protection
- Reverse Current Protection
- Automatic Output Discharge for Fast Turnoff
- Create a Custom Design Using the LP5910 With the WEBENCH® Power Designer

2 Applications

- Mobile Phones, Tablets
- Digital Cameras and Audio Devices
- Portable and Battery-Powered Equipment
- Portable Medical Equipment
- Virtual Reality
- RF, PLL, VCO, and Clock Power Supplies
- IP Cameras

3 Description

The LP5910 is a low-noise LDO that can supply up to 300 mA of output current. Designed to meet the requirements of RF and analog circuits, this device provides low noise, high PSRR, low quiescent current, and superior line transient and load transient response. Using new innovative design techniques the LP5910 offers class-leading noise performance without a noise bypass capacitor and with the option for remote output capacitor placement.

The device contains a reverse current protection circuit that prevents a reverse current flow through the LDO to the IN pin when the input voltage is lower than the output voltage.

When the Enable (EN) pin is low, and the output is in an OFF state, an automatic output discharge circuit discharges the output capacitance for fast turnoff.

With its low input and low output voltage range the LP5910 is well-suited as a post DC-DC regulator (post BUCK regulator) or for single- or dual-cell applications.

The device is designed to work with a 1-µF input and a 1-µF output ceramic capacitor. A separate noise bypass capacitor is not required.

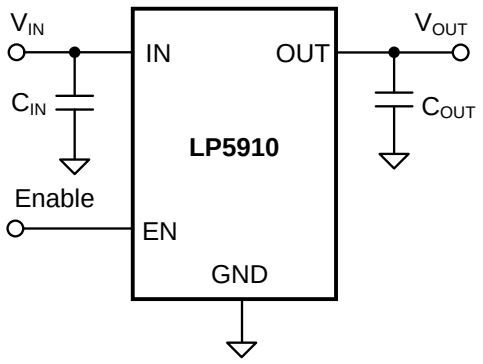
This device is available with fixed output voltages from 0.8 V to 2.3 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option needs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LP5910	WSON (6)	2.00 mm × 2.00 mm (NOM)
	DSBGA (4)	0.742 mm × 0.742 mm (MAX)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2016) to Revision E — **Page**

- Added new package, YKA0004-C01 associated with orderables LP5910-1.1BYKAR and LP5910-1.1BYKAT; added links for WEBENCH ... 1

Changes from Revision C (June 2016) to Revision D — **Page**

- Changed wording of data sheet title and list of *Applications* ... 1
- Changed "Very Low Noise Without a Noise Bypass Capacitor: 12 μV_{RMS} Typical" to "Low Output-Voltage Noise: 12 μV_{RMS}" ... 1
- Changed wording of first sentence of *Description* ... 1

Changes from Revision B (October 2015) to Revision C — **Page**

- Changed "linear regulator" to "LDO" on page 1 ... 1

Changes from Revision A (October 2015) to Revision B — **Page**

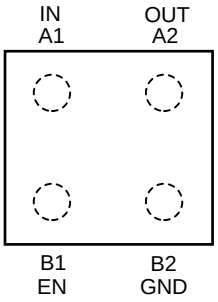
- Changed "... = 2.3 V" to "... ≤ 2.3 V" in Dropout Voltage rows; added DSBGA only; also added new rows in Dropout Voltage for WSON package. ... 5

Changes from Original (September 2015) to Revision A — **Page**

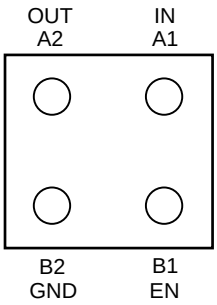
- Changed device data sheet from product preview to production data status; added icon for reference design to top navigators ... 1

5 Pin Configuration and Functions

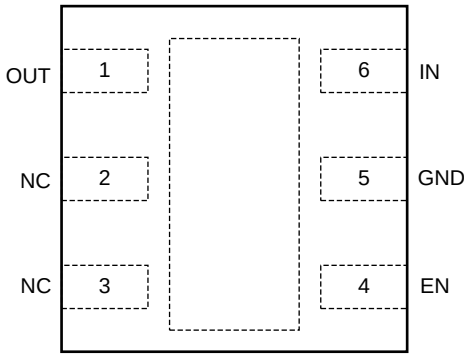
YKA Package
4-Pin Ultra-Thin DSBGA
Top View



YKA Package
4-Pin Ultra-Thin DSBGA
Bottom View



DRV Package
6-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSBGA	WSON		
EN	B1	4	I	Enable input; disables the regulator when logic low. Enables the regulator when logic high. An internal 1-MΩ pull down resistor connects this input to ground.
GND	B2	5	—	Common ground
IN	A1	6	I	Voltage supply input. A 1-µF capacitor must be connected at this input.
NC	—	2, 3	—	No internal connection. Connect to ground or leave open.
OUT	A2	1	O	Voltage output. A 1-µF low-ESR capacitor must be connected from this pin to the GND pin. Connect this output to the load circuit.
Exposed Pad	—	Thermal Pad	—	The exposed thermal pad on the bottom of the package must be connected to a copper area under the package on the PCB. Connect to ground potential or leave floating. Do not connect to any potential other than the same ground potential seen at device pin 5 (GND). See *Power Dissipation* for more information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage, V_{IN}	–0.3	3.6	V
Output voltage, V_{OUT}	–0.3	3.6	V
Enable input voltage, V_{EN}	–0.3	3.6	V
Continuous power dissipation(3)	Internally Limited		W
Junction temperature, $T_{J(MAX)}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage, V_{IN}	1.3	3.3	V
Output voltage, V_{OUT}	0.8	2.3	V
Enable input voltage, V_{EN}	0	3.3	V
Output current, I_{OUT}	0	300	mA
Junction temperature, T_J(1)	–40	125	°C
Ambient temperature, T_A(1)	–40	85	°C

(1) The maximum ambient temperature, ($T_{A(MAX)}$) is a recommended value only and can vary depending on device power dissipation and $R_{\theta JA}$. For reliable operation, the junction temperature (T_J) must be limited to a maximum of 125°C. Ambient temperature (T_A), thermal resistance ($R_{\theta JA}$) , V_{IN}, V_{OUT}, and I_{OUT} all define $T_J : T_J = T_A + (R_{\theta JA} \times ((V_{IN} – V_{OUT}) \times I_{OUT})$.

6.4 Thermal Information

THERMAL METRIC(1)		LP5910		UNIT
		YKA (DSBGA)	DRV (WSON)	
		4 PINS	6 PINS	
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance, High-K	202.8	79.2(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.3	110.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.0	48.7	
ψ_{JT}	Junction-to-top characterization parameter	0.4	5.2	
ψ_{JB}	Junction-to-board characterization parameter	36.0	49.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	18.1	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the WSON/DRV package $R_{\theta JA}$ includes two (2) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

Unless otherwise specified, $V_{IN} = V_{OUT(NOM)} + 0.5$ V, $V_{EN} = 1$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF.(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	$V_{IN} = (V_{OUT(NOM)} + 0.5\ V)$ to 3.3 V, I_{OUT} = 1 mA to 300 mA		–2		2	$\%V_{OUT}$
	Line regulation	$V_{IN} = (V_{OUT(NOM)} + 0.5\ V)$ to 3.3 V, I_{OUT} = 1 mA			0.01		%/V
	Load regulation	I_{OUT} = 1 mA to 300 mA			0.002		%/mA
I_{LOAD}	Load current	See(4)		0		300	mA
I_Q	Quiescent current(5)	V_{EN} = 1 V, I_{OUT} = 0 mA			12	25	µA
		V_{EN} = 1 V, I_{OUT} = 300 mA			230	350	
$I_{Q(SD)}$	Quiescent current in shutdown(5)	V_{EN} = 0.3 V, –40°C ≤ T_J ≤ 85°C			0.02	2	
I_{RO}	Output reverse current(6) $V_{OUT} > V_{IN}$	V_{OUT} = 3.3 V, $V_{IN} = V_{EN}$ = 0 V		–20		0	µA
		V_{OUT} = 3.3 V, $V_{IN} = V_{EN}$ = 1.3 V		0		50	µA
I_G	Ground current(7)	I_{OUT} = 0 mA (V_{OUT} = 2.3 V)			15		µA
V_{DO}	Dropout voltage(8)	1.3 V ≤ V_{OUT} < 1.5 V, I_{OUT} = 300 mA	DSBGA only		200	300	mV
		1.5 V ≤ V_{OUT} ≤ 2.3 V, I_{OUT} = 300 mA	DSBGA only		120	180	
		1.3 V ≤ V_{OUT} < 1.5 V, I_{OUT} = 300 mA	WSON only		245	370	
		1.5 V ≤ V_{OUT} ≤ 2.3 V, I_{OUT} = 300 mA	WSON only		145	220	
I_{LIMIT}	Output current limit	$V_{OUT} = V_{OUT(NOM)} - 0.1$ V, $V_{IN} = V_{OUT(NOM)} + 0.5$ V			450		mA
PSRR	Power supply rejection ratio(9)	f = 100 Hz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			80		dB
		f = 1 kHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			75		
		f = 10 kHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			65		
		f = 100 kHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			40		
		f = 2 MHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			25		
		f = 100 Hz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			65		
		f = 1 kHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			65		
		f = 10 kHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			65		
		f = 100 kHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			40		
		f = 2 MHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			25		
e_N	Output noise voltage(9)	BW = 10 Hz to 100 kHz	I_{OUT} = 1 mA		12		μV_{RMS}
			I_{OUT} = 300 mA		12		
T_{SD}	Thermal shutdown	T_J rising until output is OFF			160		°C
	Thermal hysteresis	T_J falling from shutdown			15		

(1) All voltages are with respect to the device GND pin.
(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the T_J range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount-Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) The device maintains a stable, regulated output voltage without a load current.
(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}. $I_Q = (I_{IN} - I_{OUT})$
(6) Output reverse current (I_{RO}) is measured at the IN pin.
(7) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(8) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. Dropout voltage is not a valid condition for output voltages less than 1.3 V as compliance with the minimum operating input voltage can not be ensured.
(9) This specification is verified by design.

Electrical Characteristics (continued)

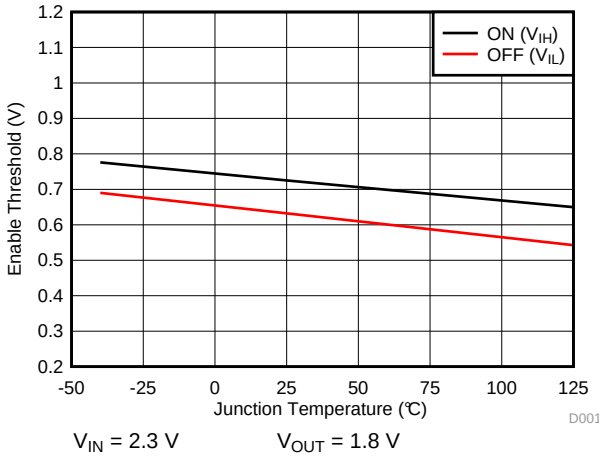
Unless otherwise specified, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT THRESHOLDS						
V_{IL}	EN low threshold (Off)	V_{IN} = 1.3 V to 3.3 V			0.3	V
V_{IH}	EN high threshold (On)		1			
I_{EN}	EN pin current(10)	V_{EN} = 3.3 V, V_{IN} = 3.3 V		3.3		µA
		V_{EN} = 0 V, V_{IN} = 3.3 V		0.001		
TRANSIENT CHARACTERISTICS(10)						
ΔV_{OUT}	Line transient(9)	V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 µs, I_{OUT} = 1 mA		0	1	mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 0.5 V) in 30 µs, I_{OUT} = 1 mA	–1	0		
	Load transient(9)	I_{OUT} = 1 mA to 100 mA in 10 µs	–45			mV
		I_{OUT} = 100 mA to 1 mA in 10 µs			45	
	Overshoot on start-up(9)				5%	
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$		80	200	µs
OUTPUT DISCHARGE						
R_{AD}	Output discharge pulldown resistance	V_{EN} = 0 V, V_{IN} = 2.3 V		160		Ω

(10) There is a 1-MΩ resistor between EN and ground on the device.

6.6 Typical Characteristics

Unless otherwise stated: V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C.



V_{IN} = 2.3 V V_{OUT} = 1.8 V

Figure 1. V_{EN} Threshold vs Temperature

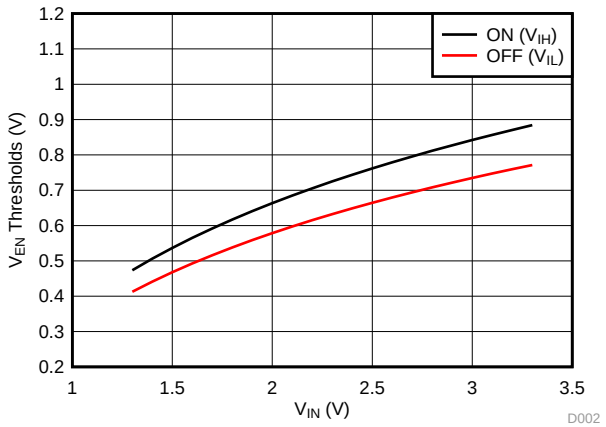
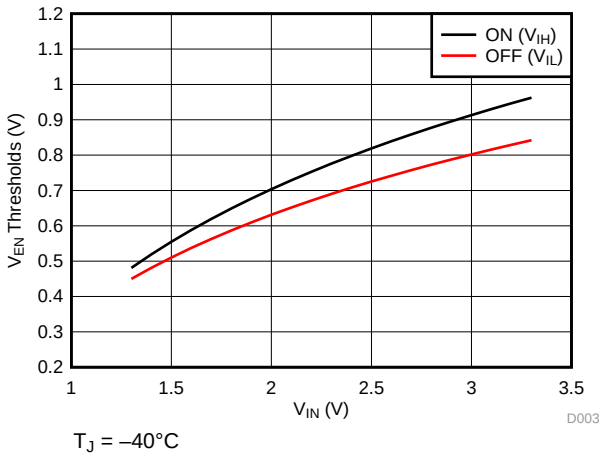
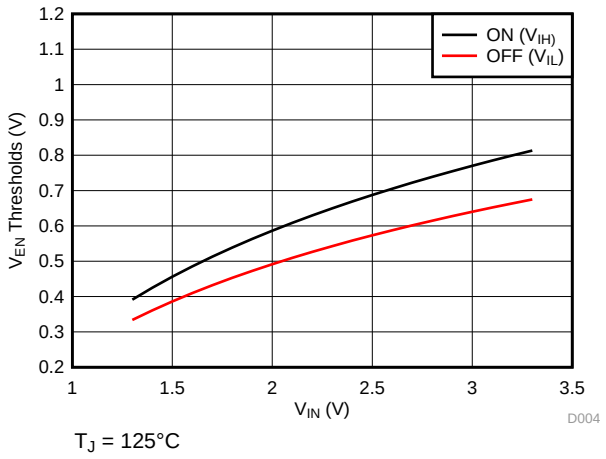


Figure 2. V_{EN} Thresholds vs V_{IN}



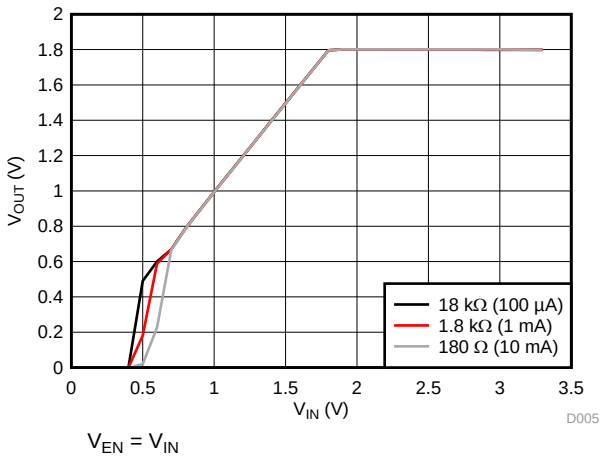
T_J = –40°C

Figure 3. V_{EN} Thresholds vs V_{IN}



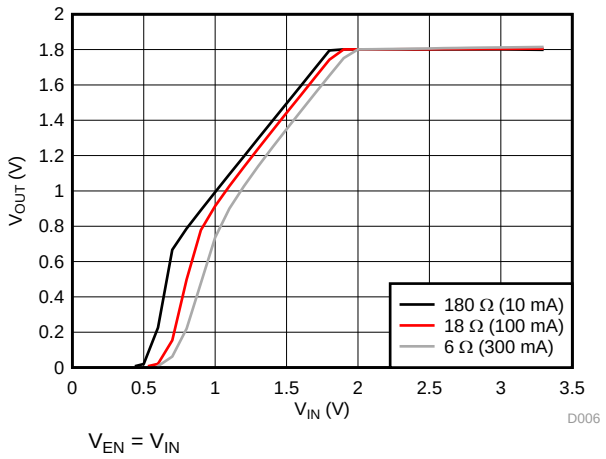
T_J = 125°C

Figure 4. V_{EN} Thresholds vs V_{IN}



V_{EN} = V_{IN}

Figure 5. V_{OUT} vs V_{IN}

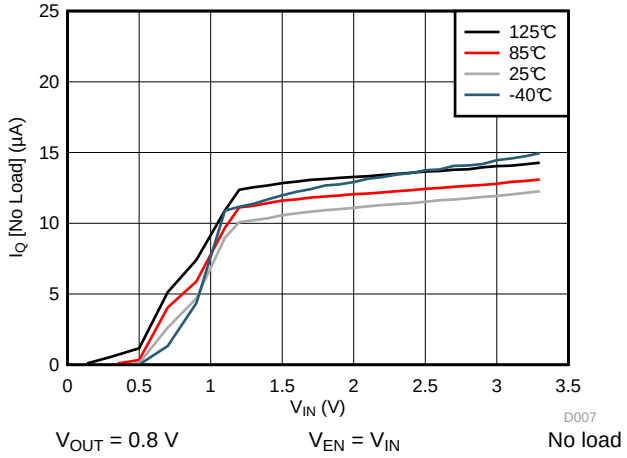


V_{EN} = V_{IN}

Figure 6. V_{OUT} vs V_{IN}

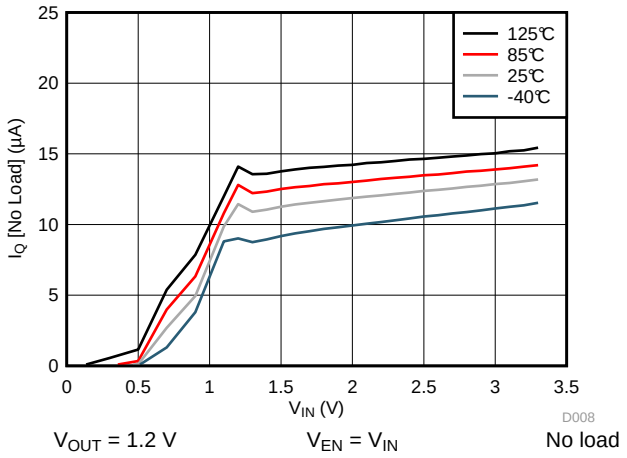
Typical Characteristics (continued)

Unless otherwise stated: V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C.



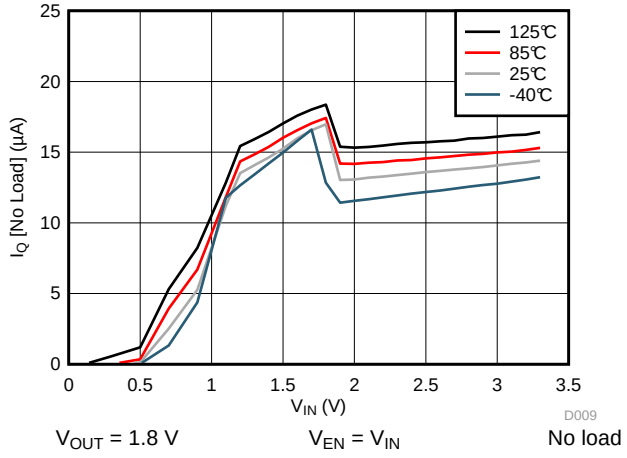
V_{OUT} = 0.8 V V_{EN} = V_{IN} No load

Figure 7. I_Q vs V_{IN}



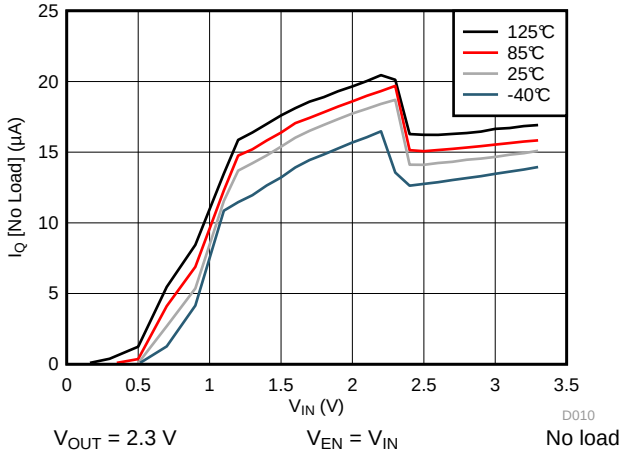
V_{OUT} = 1.2 V V_{EN} = V_{IN} No load

Figure 8. I_Q vs V_{IN}



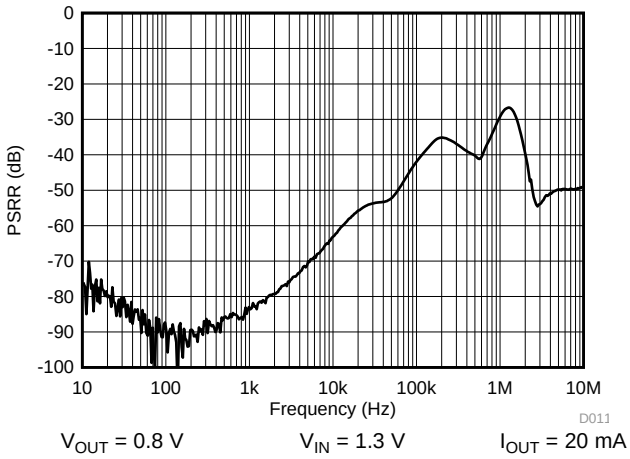
V_{OUT} = 1.8 V V_{EN} = V_{IN} No load

Figure 9. I_Q vs V_{IN}



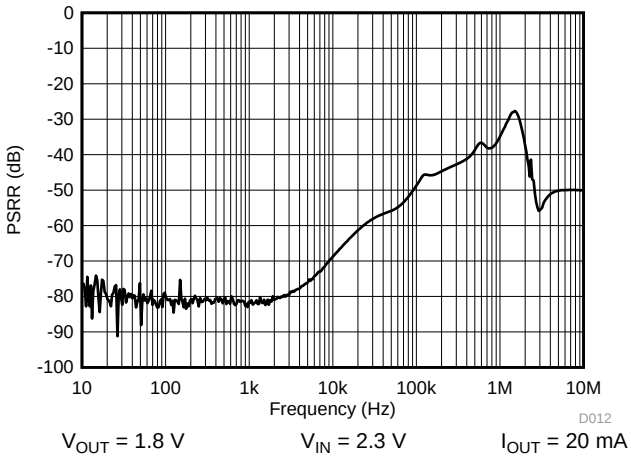
V_{OUT} = 2.3 V V_{EN} = V_{IN} No load

Figure 10. I_Q vs V_{IN}



V_{OUT} = 0.8 V V_{IN} = 1.3 V I_{OUT} = 20 mA

Figure 11. PSRR vs Frequency

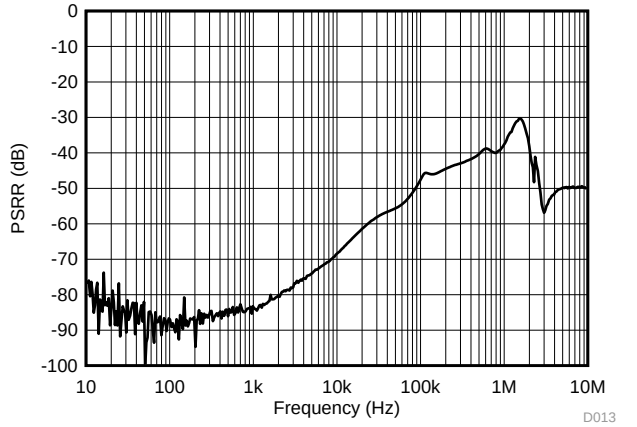


V_{OUT} = 1.8 V V_{IN} = 2.3 V I_{OUT} = 20 mA

Figure 12. PSRR vs Frequency

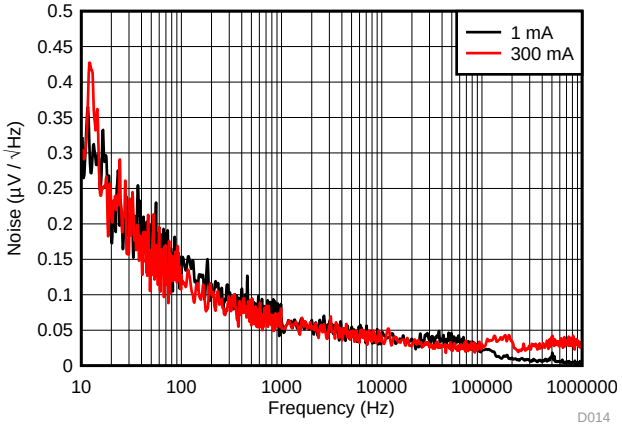
Typical Characteristics (continued)

Unless otherwise stated: V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C.



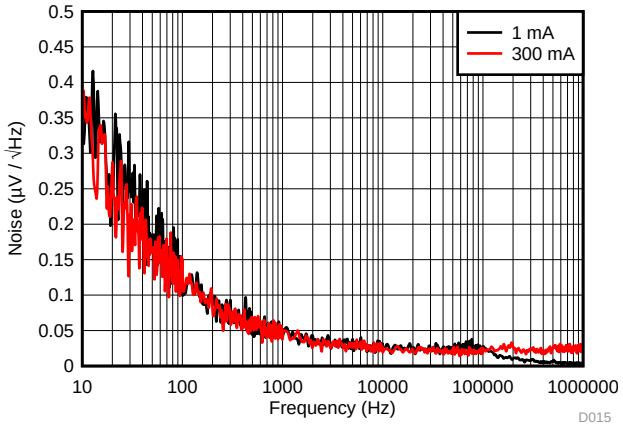
V_{OUT} = 2.3 V V_{IN} = 2.8 V I_{OUT} = 20 mA

Figure 13. PSRR vs Frequency



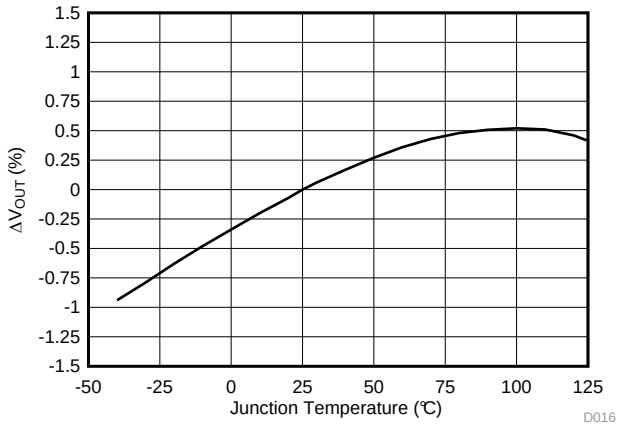
V_{OUT} = 0.8 V V_{IN} = 1.3 V

Figure 14. Noise Density



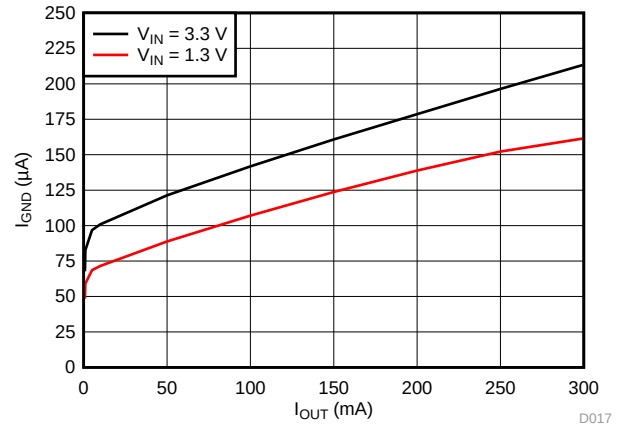
V_{OUT} = 2.3 V V_{IN} = 2.8 V

Figure 15. Noise Density



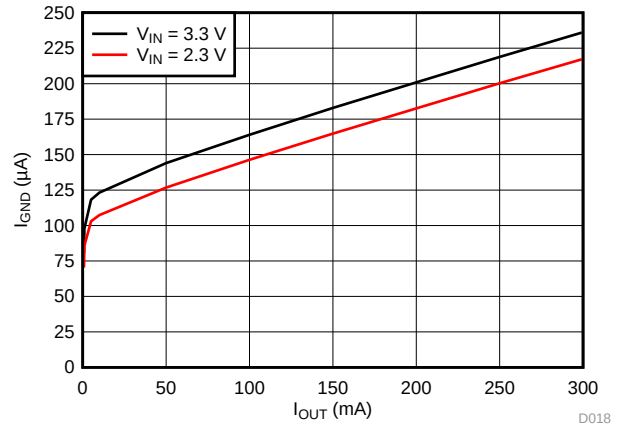
V_{IN} = V_{OUT} + 0.5 V I_{OUT} = 1 mA

Figure 16. ΔV_{OUT} vs Temperature



V_{OUT} = 0.8 V

Figure 17. I_{GND} vs I_{OUT}

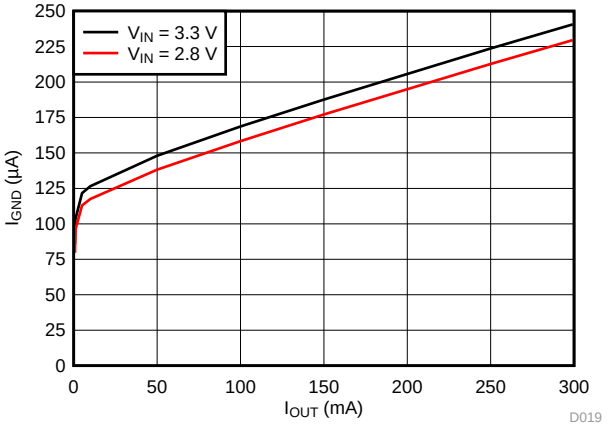


V_{OUT} = 1.8 V

Figure 18. I_{GND} vs I_{OUT}

Typical Characteristics (continued)

Unless otherwise stated: V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C.



V_{OUT} = 2.3 V

Figure 19. I_{GND} vs I_{OUT}

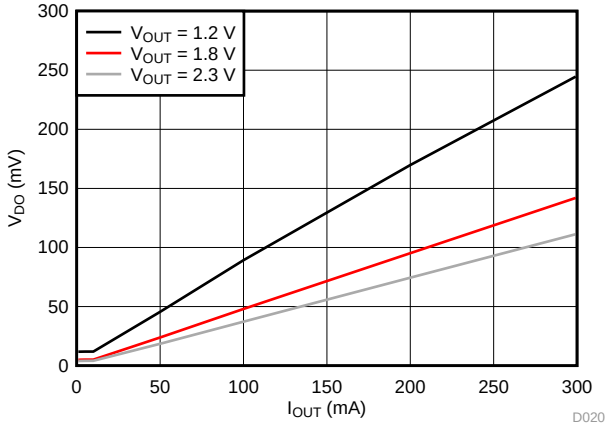
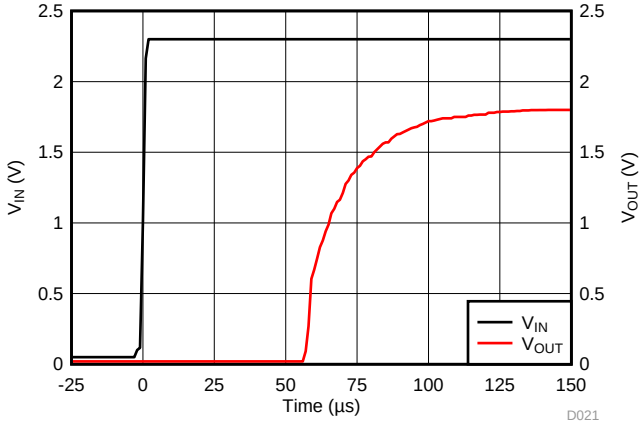
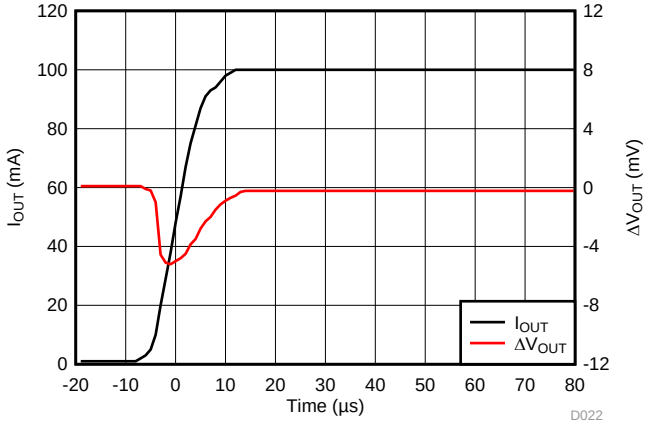


Figure 20. Dropout Voltage vs I_{OUT}



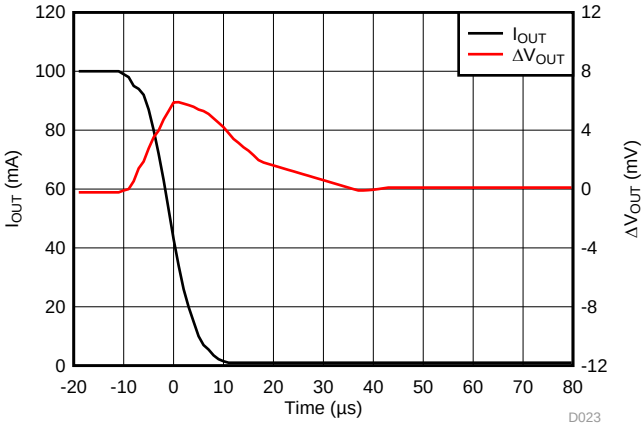
V_{EN} = V_{IN} V_{OUT} = 1.8 V C_{OUT} = 1 µF

Figure 21. Turnon Time



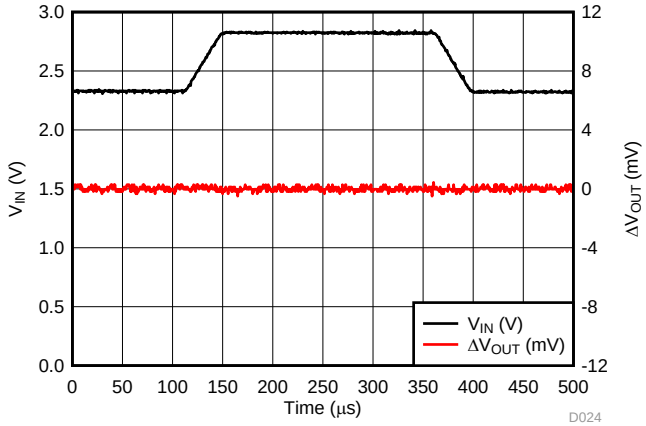
V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
I_{OUT} = 1 mA to 100 mA t_{RISE} = 10 µs

Figure 22. Load Transient Response



V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
I_{OUT} = 100 mA to 1 mA t_{FALL} = 10 µs

Figure 23. Load Transient Response



ΔV_{IN} = 0.5 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
t_{RISE} = t_{FALL} = 30 µs I_{OUT} = 1 mA

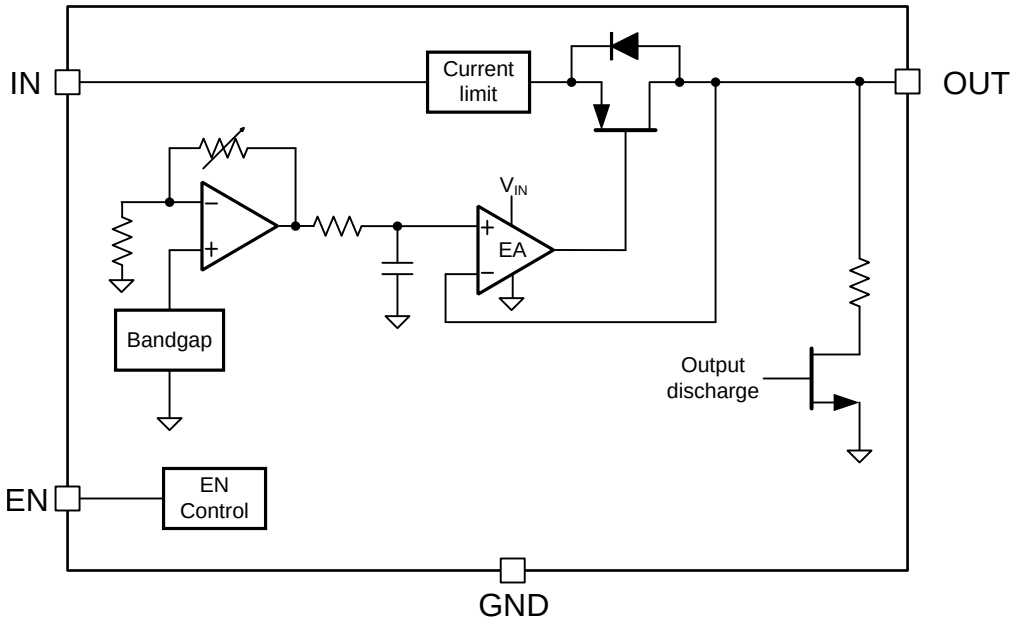
Figure 24. Line Transient Response

7 Detailed Description

7.1 Overview

The LP5910 is a linear regulator capable of supplying 300-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5910 device provides low noise, high PSRR, low quiescent current, and low line/load transient response figures. Using new innovative design techniques the LP5910 offers class-leading noise performance without a noise bypass capacitor and the option for remote output capacitor placement.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP5910 remains stable and in regulation with no external load.

7.3.2 Thermal Overload Protection

The LP5910 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 145°C (typical).

7.3.3 Short-Circuit Protection

The LP5910 contains internal current limit which reduces output current to a safe value if the output is overloaded or shorted. Depending upon the value of V_{IN}, thermal limiting may also become active as the average power dissipated causes the die temperature to increase to the limit value (about 160°C). The hysteresis of the thermal shutdown circuitry can result in a *cyclic* behavior on the output as the die temperature heats and cools.

7.3.4 Output Automatic Discharge

The LP5910 output employs an internal 160-Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

Feature Description (continued)

7.3.5 Reverse Current Protection

The device contains a reverse current protection circuit that prevents a backward current flowing through the LDO from the OUT pin to the IN pin.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5910 may be switched to the ON or OFF state by logic input at the EN pin. A logic-high voltage on the EN pin turns the device to the ON state. A logic-low voltage on the EN pin turns the device to the OFF state. If the application does not require the shutdown feature, the EN pin must be tied to VIN to keep the regulator output permanently in the ON state when power is applied

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH}.

A 1-MΩ pulldown resistor ties the EN input to ground. If the EN pin is left open, the internal 1-MΩ pulldown resistor ensures that the device is turned into an OFF state by default.

When the EN pin is low, and the output is in an OFF state, the output activates an internal pulldown resistance to discharge the output capacitance for fast turnoff.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5910 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The LP5910 delivers this performance in an industry-standard DSBGA package which, for this device, is specified with a T_J of –40°C to +125°C.

8.2 Typical Application

Figure 25 shows the typical application circuit for the LP5910. Input and output capacitances may need to be increased above 1-µF minimum for some applications.

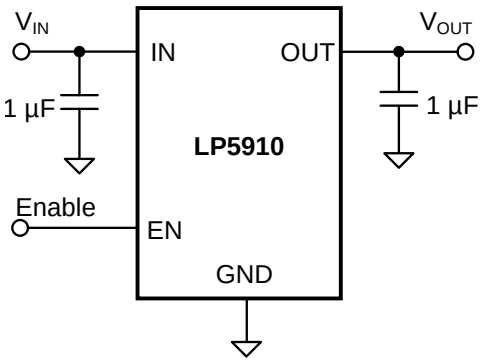


Figure 25. LP5910 Typical Application

8.2.1 Design Requirements

For typical LP5910 applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	1.3 V to 3.3 V
Output voltage	0.8 V to 2.3 V
Output current	300 mA
Output capacitor range	1 µF to 10 µF

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP5910 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 External Capacitors

Like most low-dropout regulators, the LP5910 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected from the LP5910 IN pin to ground. (This capacitance value may be increased without limit.) The input capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains 1 µF ±30% over the entire operating temperature range.

8.2.2.4 Output Capacitor

For capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5910. The temperature performance of ceramic capacitors varies by type. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

8.2.2.5 Capacitor Characteristics

The LP5910 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5910.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 10-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.6 Remote Capacitor Operation

The LP5910 requires at least a 1-µF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the OUT pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum, using as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many vias as possible between the connection layers. It is recommended to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, an input capacitor is recommended, equal to or larger to the sum of the capacitance at the output node, for the best load-transient performance.

8.2.2.7 No-Load Stability

The LP5910 remains stable, and in regulation, with no external load.

8.2.2.8 Enable Control

The LP5910 may be switched to an ON or OFF state by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 µA. Additionally, an output pulldown circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-MΩ pulldown resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

Table 2. Recommended Output Capacitor Specification

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Output capacitor, C_{OUT}	Capacitance for stability	0.7	1	10	µF
	ESR	5		500	mΩ

8.2.2.9 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} – V_{OUT}) \times I_{OUT(MAX)} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad to the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area .

On the DSBGA (YKA) package, the primary conduction path for heat is through the four bumps to the PCB.

The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.10 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 1.
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

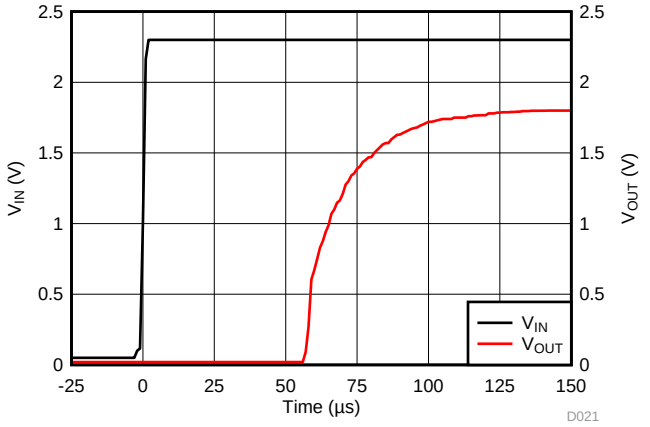
- $P_{D(MAX)}$ is explained in Equation 1.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see the TI Application Report: *Semiconductor and IC Package Thermal Metrics* (SPRA953), available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report: *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

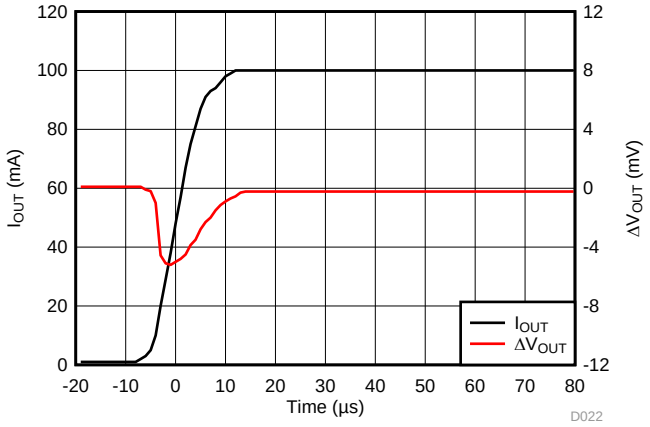
For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017), available for download at www.ti.com.

8.2.3 Application Curves



$V_{EN} = V_{IN}$ V_{OUT} = 1.8 V C_{OUT} = 1 µF

Figure 26. Turnon Time



V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
I_{OUT} = 1 mA to 100 mA t_{RISE} = 10 µs

Figure 27. Load Transient Response

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.3 V to 3.3 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5910 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 0.5 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5910 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5910.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5910 device, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP5910 GND pin using as wide and as short of a copper trace as is practical.

Avoid connections using long trace lengths, narrow trace widths, and/or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

10.2 Layout Examples

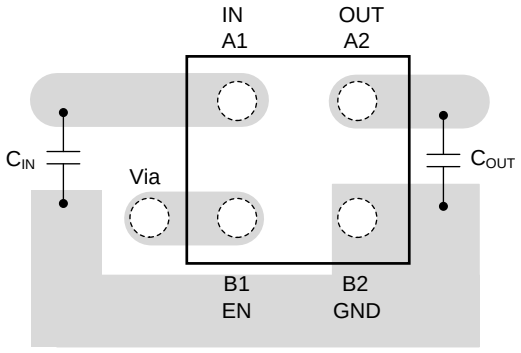


Figure 28. LP5910 Typical DSBGA Layout

Layout Examples (continued)

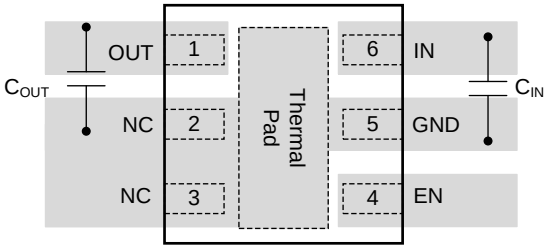


Figure 29. LP5910 Typical WSON Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. High intensity light sources such as halogen lamps can affect electrical performance if they are situated in close proximity to the device. The wavelengths that have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has little effect on performance.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP5910 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.1.2 Related Documentation

For related documentation, see the following:

- *AN-1112 DSBGA Wafer Level Chip Scale Package*
- *Semiconductor and IC Package Thermal Metrics*
- *Using New Thermal Metrics*
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

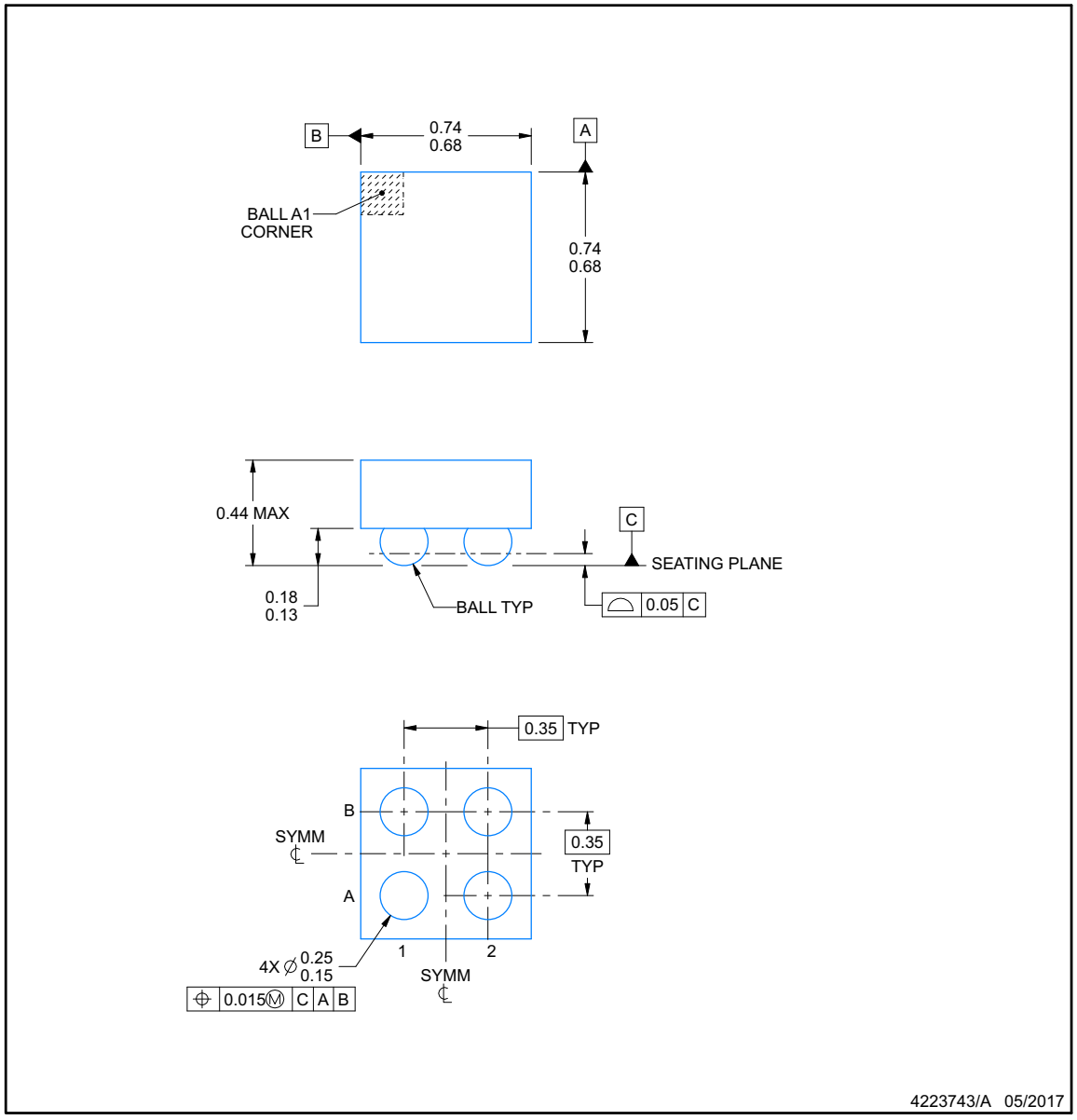
LP5910-1.1BYKA

YKA0004-C01

PACKAGE OUTLINE

DSBGA - 0.44 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

www.ti.com

Figure 30.

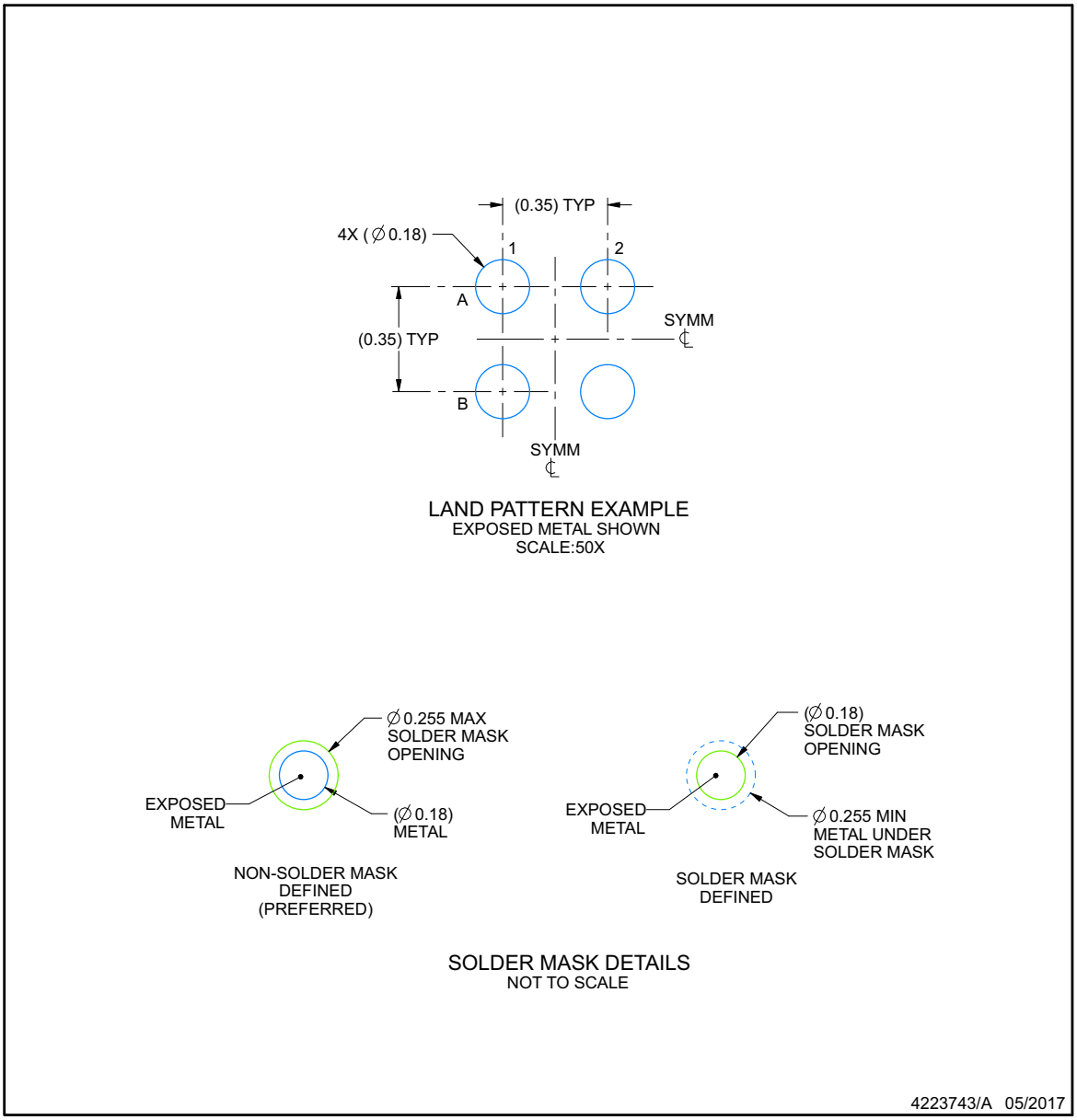
LP5910-1.1BYKA

EXAMPLE BOARD LAYOUT

YKA0004-C01

DSBGA - 0.44 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

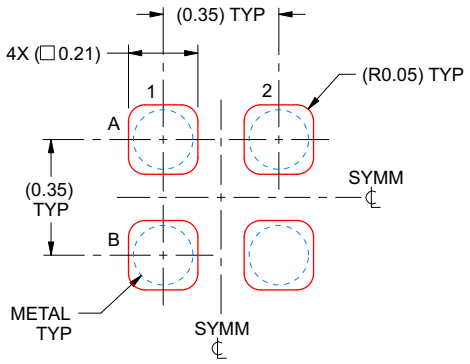
LP5910-1.1BYKA

EXAMPLE STENCIL DESIGN

YKA0004-C01

DSBGA - 0.44 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223743/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5910-0.9YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5910-1.0DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	59A	Samples
LP5910-1.0YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A	Samples
LP5910-1.1BYKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
LP5910-1.1BYKAT	ACTIVE	DSBGA	YKA	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
LP5910-1.1YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
LP5910-1.2YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5910-1.825YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
LP5910-1.825YKAT	ACTIVE	DSBGA	YKA	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
LP5910-1.8DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C	Samples
LP5910-1.8DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C	Samples
LP5910-1.8YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5910-1.8YKAT	ACTIVE	DSBGA	YKA	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
PLP5910-1.2PYCPR	ACTIVE	DSBGA	YCP	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

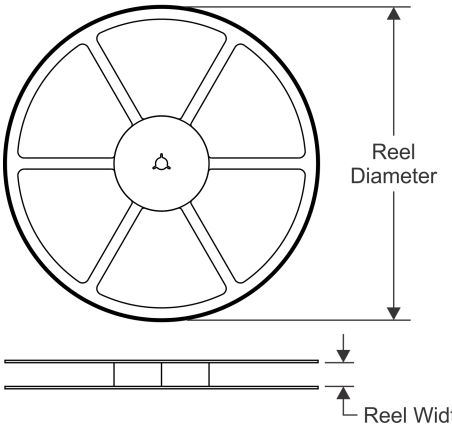
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

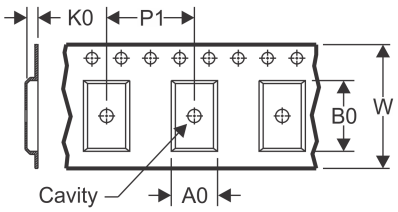
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

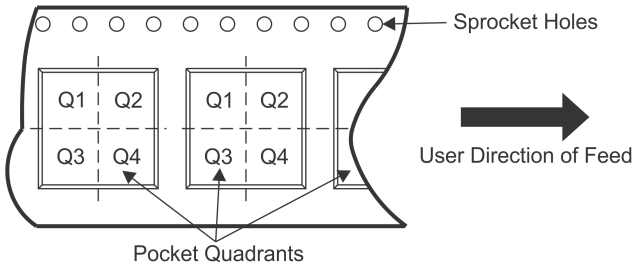


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

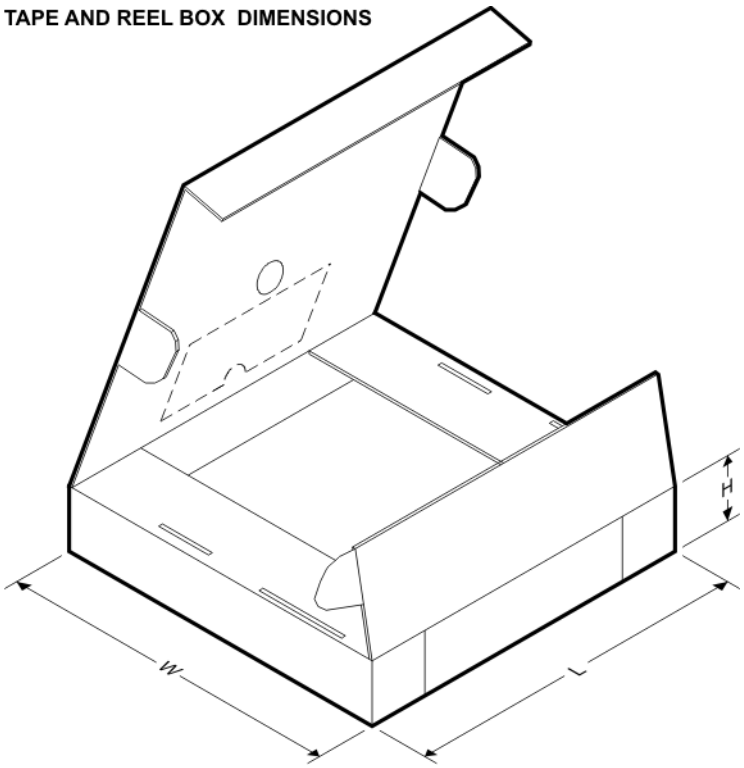
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5910-0.9YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.0DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.0YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.1BYKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.1BYKAT	DSBGA	YKA	4	250	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.825YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.825YKAT	DSBGA	YKA	4	250	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.8DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.8DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.8YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.8YKAT	DSBGA	YKA	4	250	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

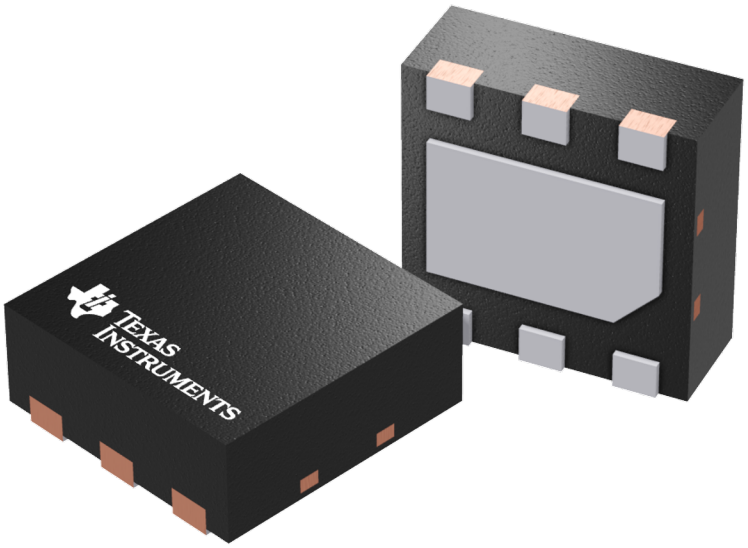


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5910-0.9YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.0DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
LP5910-1.0YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.1BYKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.1BYKAT	DSBGA	YKA	4	250	182.0	182.0	20.0
LP5910-1.1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.825YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.825YKAT	DSBGA	YKA	4	250	182.0	182.0	20.0
LP5910-1.8DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
LP5910-1.8DRVT	WSON	DRV	6	250	182.0	182.0	20.0
LP5910-1.8YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.8YKAT	DSBGA	YKA	4	250	182.0	182.0	20.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



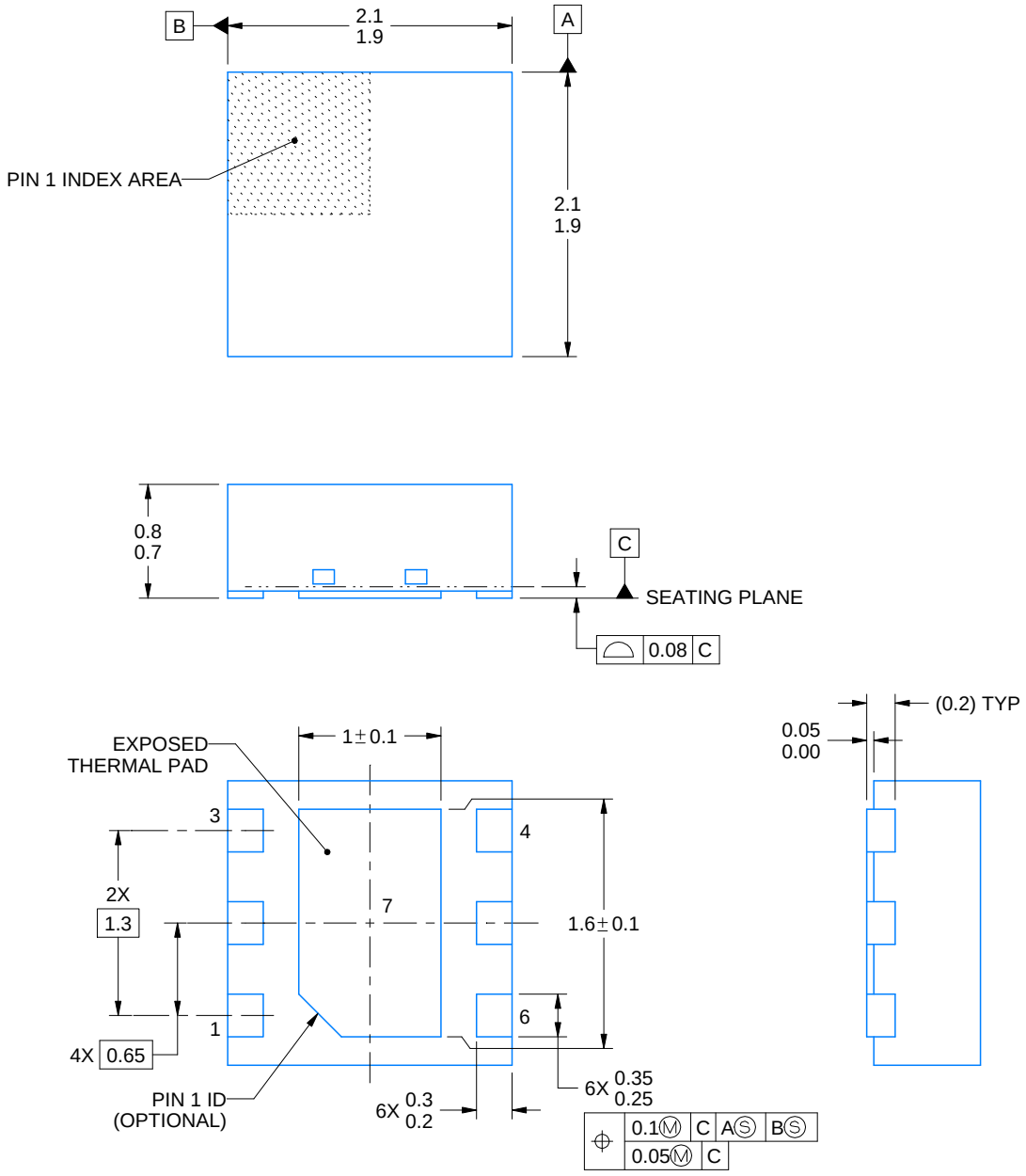
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

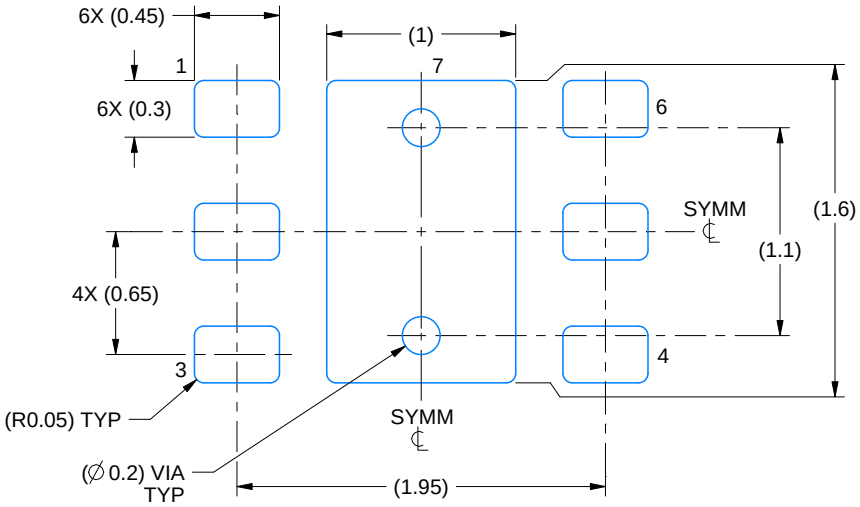
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

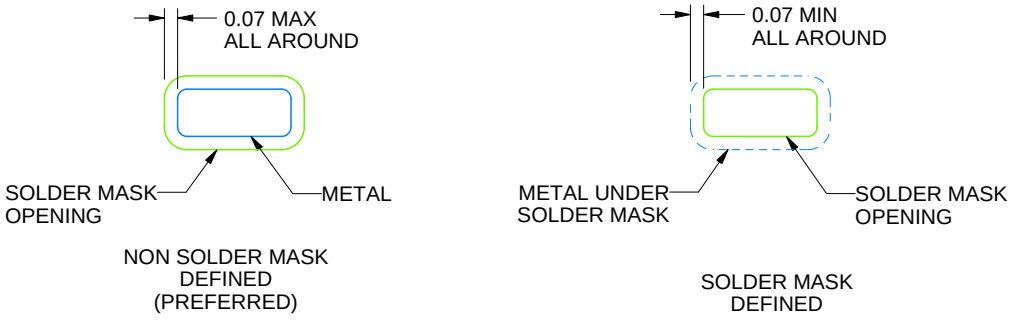


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

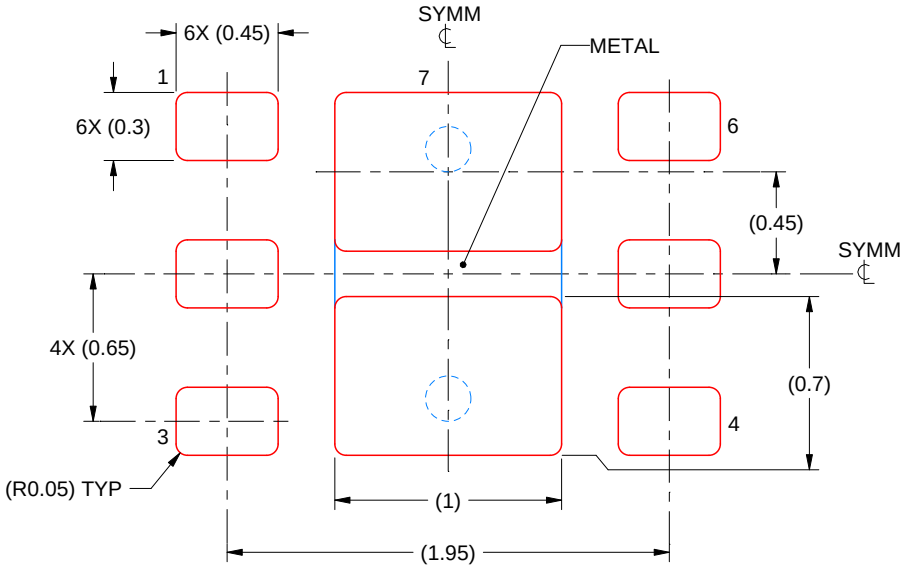
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

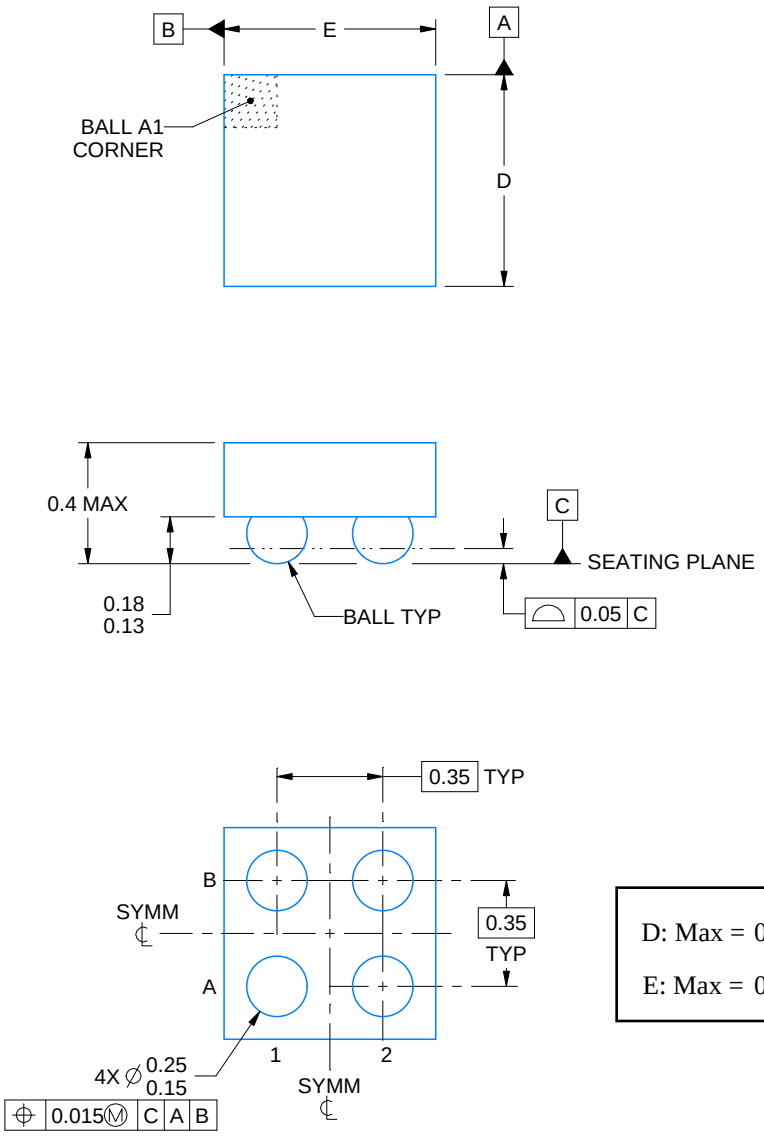
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



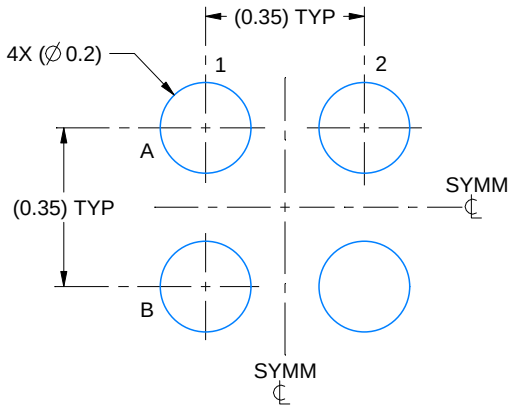
D: Max = 0.742 mm, Min =0.682 mm

E: Max = 0.742 mm, Min =0.682 mm

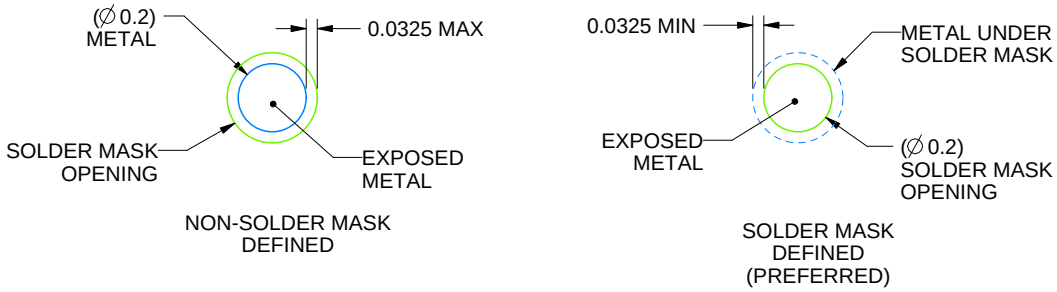
4221909/B 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

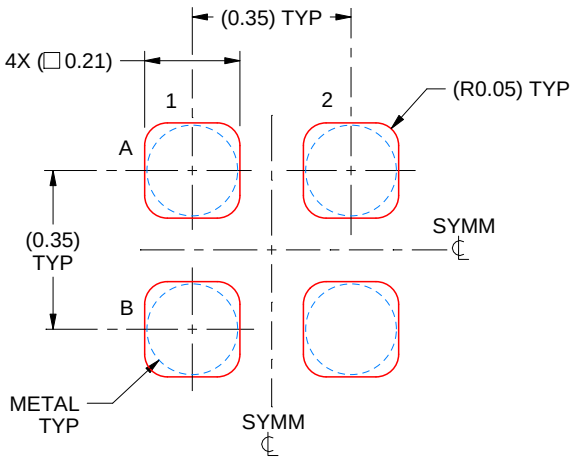


SOLDER MASK DETAILS
NOT TO SCALE

4221909/B 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

4221909/B 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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