

TAS2557 5.7-W Class-D mono audio amplifier with class-H boost and speaker sense

1 Features

- Ultra low-noise mono boosted class-D amplifier
 - 5.7 W at 1% THD+N and 6.9 W at 10% THD+N into 4- Ω load from 4.2-V supply
 - 3.8 W at 1% THD+N and 4.5 W at 10% THD+N into 8- Ω load from 4.2-V supply
- Output noise for DAC + class-D (ICN) is 15.9 μ V
- DAC + class-D SNR 111 dB at 1%THD+N/8 Ω
- THD+N –90 dB at 1 W / 8 Ω with flat frequency response
- Post-filter feedback (PFFB)
- PSRR 110 dB for 200 mV_{pp} ripple at 217 Hz
- Input sample rates from 8 kHz to 96 kHz
- Built-in speaker sense
 - Measures speaker current and voltage
 - Measures V_{BAT} voltage, chip temperature
- Dedicated real-time dual-core DSP for speaker protection
 - Thermal and excursion protection
 - Detects speaker leaks and damage
- High efficiency class-H boost converter with multi-level tracking
 - 86% at 500 mW in 8 Ω with 3.6 V V_{BAT}
 - 87% at 700 mW in 8 Ω with 4.2 V V_{BAT}
- Configurable automatic gain control (AGC)
 - Limits battery current consumption
- Adjustable class-D switching edge-rate control
- Thermal, short-circuit, and under-voltage protection
- I²S, Left-justified, right-justified, DSP, and TDM input and output interface,
- I²C or SPI interface for register control
- Stereo configuration using two TAS2557 devices
- Power supplies
 - Boost input: 2.9 V to 5.5 V
 - Analog/digital: 1.65 V to 1.95 V
 - Digital I/O: 1.62 V to 3.6 V
- 42-ball, 0.5-mm pitch, DSBGA package

2 Applications

- Mobile phones and tablets
- Video doorbells and voice enabled thermostats
- Personal computers
- Bluetooth speakers and accessories

3 Description

The TAS2557 device is a state-of-the-art Class-D audio amplifier which is a full system on a Chip (SoC). The device features a ultra low-noise audio DAC and Class-D power amplifier which incorporates speaker voltage and current sensing feedback. An on-chip, low-latency DSP supports Texas Instruments SmartAmp speaker protection algorithms to maximizes loudness while maintaining safe speaker conditions.

The device can be used easily with any processor with an I2S output and stereo implementations are possible when using two TAS2557 devices. Separate tuning for different speakers is supported allowing customers to add value while maintaining form factor designs. Additionally, the TAS2557 supports separate voice and audio tuning dynamically with ultra-low 15.9 μ V ICN regardless of mode of operation making receiver/speaker implementations possible.

A Class-H boost converter generates the Class-D amplifier supply rail. When the audio signal only requires a lower Class-D output power, the boost improves system efficiency by deactivating and connecting V_{BAT} directly to the Class-D amplifier supply. When higher audio output power is required, the multi-level boost quickly activates tracking the signal to provide the additional voltage to the load.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| TAS2557 | DSBGA (42) | 3.47 mm x 3.23 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

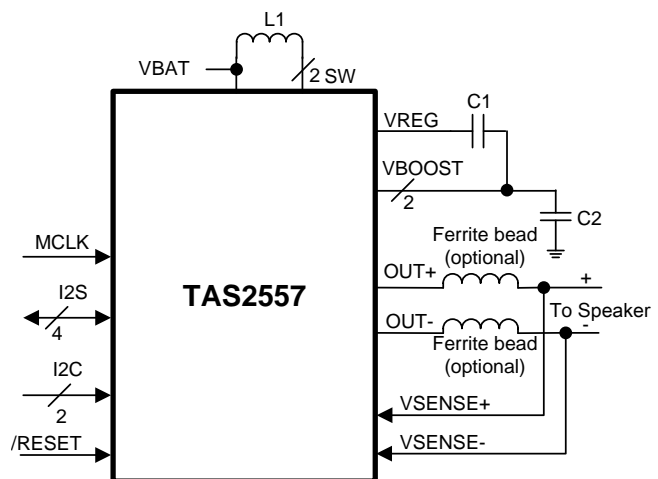


Table of Contents

| | | | |
|---|-----------|--|------------|
| 1 Features | 1 | 9.3 Feature Description | 18 |
| 2 Applications | 1 | 9.4 Device Functional Modes | 29 |
| 3 Description | 1 | 9.5 Programming | 36 |
| 4 Revision History | 2 | 9.6 Register Map | 39 |
| 5 Device Comparison Table | 3 | 10 Application and Implementation | 96 |
| 6 Pin Configuration and Functions | 4 | 10.1 Application Information | 96 |
| 7 Specifications | 6 | 10.2 Typical Application | 96 |
| 7.1 Absolute Maximum Ratings | 6 | 10.3 Initialization Setup | 98 |
| 7.2 ESD Ratings | 6 | 11 Power Supply Recommendations | 99 |
| 7.3 Recommended Operating Conditions | 6 | 11.1 Power Supplies | 99 |
| 7.4 Thermal Information | 6 | 11.2 Power Supply Sequencing | 99 |
| 7.5 Electrical Characteristics | 7 | 12 Layout | 100 |
| 7.6 I ² C Timing Requirements | 9 | 12.1 Layout Guidelines | 100 |
| 7.7 SPI Timing Requirements | 9 | 12.2 Layout Example | 101 |
| 7.8 I ² S/LJF/RJF Timing Requirements (Master Mode) .. | 10 | 13 Device and Documentation Support | 102 |
| 7.9 I ² S/LJF/RJF Timing Requirements (Slave Mode) .. | 10 | 13.1 Documentation Support | 102 |
| 7.10 DSP Timing Requirements (Master Mode) | 11 | 13.2 Community Resources | 102 |
| 7.11 DSP Timing Requirements (Slave Mode) | 11 | 13.3 Trademarks | 102 |
| 7.12 Typical Characteristics | 14 | 13.4 Electrostatic Discharge Caution | 102 |
| 8 Parameter Measurement Information | 16 | 13.5 Glossary | 102 |
| 9 Detailed Description | 17 | 14 Mechanical, Packaging, and Orderable Information | 102 |
| 9.1 Overview | 17 | 14.1 Package Dimensions | 102 |
| 9.2 Functional Block Diagram | 18 | | |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2017) to Revision B Page

- Added Boost, Switching, Regulator voltage and Note 2 to the *Absolute Maximum Ratings* table **6**
- Changed C2 Capacitance at 8.5 V derating MIN value From: 7 μ F To: 3.3 μ F in [Table 128](#) **97**

Changes from Original (November 2016) to Revision A Page

- Changed ESD HBM rating from \pm 2500 to \pm 3500 **6**
- Changed Power Consumption values **8**
- Fixed incorrect part number **30**

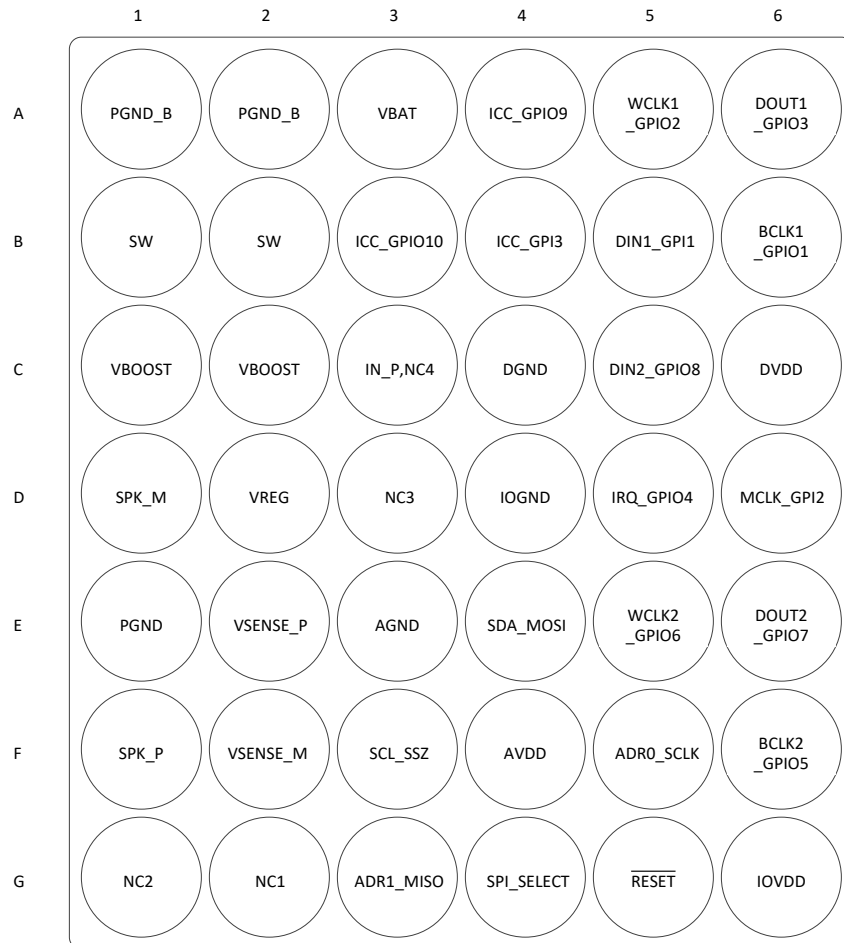
5 Device Comparison Table

| PART NUMBER | CONTROL METHOD | BOOST VOLTAGE | SNR ⁽¹⁾ | ICN | THD+N | BOOST CONTROL | SMART AMP DIGITAL ENGINE |
|-------------|-------------------------|---------------|--------------------|--------------|--------|---------------|-----------------------------------|
| TAS2552 | I ² C | 8.5 V | 94 dB | 130 μ V | -64 dB | Class-G | NO (External Processing Required) |
| TAS2553 | I ² C | 7.5 V | 94 dB | 130 μ V | -64 dB | Class-G | NO (External Processing Required) |
| TAS2555 | I ² C or SPI | 8.5 V | 111 dB | 15.9 μ V | -90 dB | Class-H | YES (Processing on Chip) |
| TAS2557 | I ² C or SPI | 8.5 V | 111 dB | 15.9 μ V | -90 dB | Class-H | YES (Processing on Chip) |
| TAS2559 | I ² C or SPI | 8.5 V | 111 dB | 15.9 μ V | -90 dB | Class-H | YES (Processing on Chip) |
| TAS2560 | I ² C | 8.5 V | 111 dB | 16.2 μ V | -88 dB | Class-H | NO (External Processing Required) |

(1) A-weighted data.

6 Pin Configuration and Functions

**42-Ball DSBGA
YZ Package
(Top View)**



Not to scale

Pin Functions

| PIN | | TYPE | DESCRIPTION |
|----------|-------------|------|--|
| BALL NO. | NAME | | |
| A1,A2 | PGND_B | P | Power ground - connect to high current ground plane. |
| A3 | VBAT | P | Battery power supply - connect to 2.9 V to 5.5 V battery supply. |
| A4 | ICC_GPIO9 | I/O | Stereo inter-chip communication clock or GPIO pin. |
| A5 | WCLK1_GPIO2 | I/O | Audio word clock on ASI#1 or GPIO pin. |
| A6 | DOUT1_GPIO3 | I/O | Audio data output on ASI#1 or GPIO pin. |
| B1,B2 | SW | P | Boost converter switch input . |
| B3 | ICC_GPIO10 | I/O | Stereo inter-chip communication data output or GPIO pin. |
| B4 | ICC_GPI3 | I | Stereo inter-chip communication data input or GPI pin. |
| B5 | DIN1_GPI1 | I | Audio data input to ASI #1 or GPI pin. |
| B6 | BCLK1_GPIO1 | I/O | Audio bit clock on ASI#1 or GPIO pin. |
| C1,C2 | VBOOST | P | Boost converter output. |
| C3 | NC4 | - | Float connection - do not route any signal or supply to or through this pin. |
| C4 | DGND | P | Digital ground pin. |
| C5 | DIN2_GPIO8 | I/O | Audio data input to ASI #2 or GPIO pin. |
| C6 | DVDD | P | 1.8V digital power supply for digital core logic. |

Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|----------|-------------|------|--|
| BALL NO. | NAME | | |
| D1 | SPK_M | O | Inverting Class-D output. |
| D2 | VREG | P | Regulator output. |
| D3 | NC3 | - | Float connection - do not route any signal or supply to or through this pin. |
| D4 | I0GND | P | Digital interface ground pin. |
| D5 | IRQ_GPIO4 | I/O | Active-high interrupt pin or GPIO pin |
| D6 | MCLK_GPIO2 | I | Master clock input or GPI pin. |
| E1 | PGND | P | Power ground - connect to high current ground plane. |
| E2 | VSENSE_P | I | Non-inverting voltage sense input. |
| E3 | AGND | P | Analog ground - connect to low noise ground plane. |
| E4 | SDA_MOSI | I/O | Multi-function digital pin for (SPI_SELECT= 0) : Data Pin for I ² C control bus. For (SPI_SELECT= 1): SPI data input. |
| E5 | WCLK2_GPIO6 | I/O | Audio word-clock on ASI#2 or GPIO pin. |
| E6 | DOUT2_GPIO7 | I/O | Audio data output on ASI#2 or GPIO pin. |
| F1 | SPK_P | O | Non-inverting Class-D output. |
| F2 | VSENSE_M | I | Inverting voltage sense input. |
| F3 | SCL_SSZ | I | Multi-function digital input. For (SPI_SELECT= 0) : Clock Pin for I ² C Control bus. For (SPI_SELECT= 1): SPI chip selection pin. |
| F4 | AVDD | P | 1.8V analog power supply. |
| F5 | ADR0_SCLK | I | Multi-function digital pin. For (SPI_SELECT= 0) : Device I ² C programming address LSB. For (SPI_SELECT= 1): SPI serial bit clock. |
| F6 | BCLK2_GPIO5 | I/O | Audio bit clock on ASI#2 or GPIO pin. |
| G1 | NC2 | - | Float connection - do not route any signal or supply to or through this pin. |
| G2 | NC1 | - | Float connection - do not route any signal or supply to or through this pin. |
| G3 | ADR1_MISO | I/O | Multi-function digital input / output. For (SPI_SELECT= 0) : Device I ² C programming address MSB. For (SPI_SELECT= 1): SPI data output |
| G4 | SPI_SELECT | I | Control interface select. 0: I ² C selected. 1: SPI selected. |
| G5 | RESET | I | Active-low reset. |
| G6 | IOVDD | P | 1.8V or 3.3V digital interface power supply for digital input and output levels. |

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|-------|---|---------------------------|------------------|
| Battery Voltage | VBAT | -0.3 | 6 | V |
| Analog Supply Voltage | AVDD | -0.3 | 2 | V |
| Digital Supply Voltage | DVDD | -0.3 | 2 | V |
| I/O Supply Voltage | IOVDD | -0.3 | 3.9 | V |
| Boost | VBST | -0.3 | 9.2 | V |
| Switching | SW | -0.7 | VBST + 1.5 ⁽²⁾ | V |
| Regulator voltage | VREG | -0.3 | VBST + 5 | V |
| Digital Input Voltage | | -0.3 | IOVDD + 0.3 | V |
| Output Continuous Total Power Dissipation | | See Thermal Information | | NA |
| Storage Temperature, T_{stg} | | -65 | 150 | $^\circ\text{C}$ |

- (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Procedures](#) is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) Cannot exceed 11 V for greater than 10 nS or 10 V continuously.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|------------|------|
| $V_{\text{(ESD)}}$ Electrostatic Discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ± 3500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ± 1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--------------------------------------|-------|--------------------|-----|------|------------------|
| Battery Voltage | VBAT | 2.9 ⁽¹⁾ | 3.6 | 5.5 | V |
| Analog Supply Voltage | AVDD | 1.65 | 1.8 | 1.95 | V |
| Digital Supply Voltage | DVDD | 1.65 | 1.8 | 1.95 | V |
| I/O Supply Voltage 1.8V | IOVDD | 1.62 | 1.8 | 1.98 | V |
| I/O Supply Voltage 3.3V | IOVDD | 3.0 | 3.3 | 3.6 | V |
| T_A Operating Free-Air Temperature | | -40 | | 85 | $^\circ\text{C}$ |
| T_J Operating Junction Temperature | | -40 | | 150 | $^\circ\text{C}$ |

- (1) Device is functional down to 2.7V. See [Battery Tracking AGC](#)

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TAS2557 | UNIT |
|-------------------------------|--|------------|--------------------|
| | | YZ (DSBGA) | |
| | | 42 PINS | |
| $R_{\theta\text{JA}}$ | Junction to Ambient Thermal Resistance | 49.8 | $^\circ\text{C/W}$ |
| $R_{\theta\text{JC(top)}}$ | Junction to Case (top) Thermal Resistance | 0.2 | |
| $R_{\theta\text{JB}}$ | Junction to Board Thermal Resistance | 7.1 | |
| Ψ_{JT} | Junction to Top Characterization Parameter | 0.8 | |
| Ψ_{JB} | Junction to Board Characterization Parameter | 7.1 | |
| $R_{\theta\text{JC(bot)}}$ | Junction to Case (bottom) Thermal Resistance | n/a | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

$V_{BAT} = 3.6V$, $AVDD = DVDD = IOVDD = 1.8V$, $\overline{RESET} = IOVDD$, Gain = 16.4 dB, ERC = 14ns, Boost Inductor = 2.2 μH , $R_L = 8\ \Omega + 33\ \mu H$, 1-kHz input frequency, 48- kHz sample rate for digital input, Class-H Boost Enabled, $T_A = 25^\circ C$, $I_{LIM} = 3A$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|----------|--------|-----|------------|
| BOOST CONVERTER | | | | | |
| Boost Output Voltage | Average voltage (w/o including ripple) | | 8.5 | | V |
| Boost Converter Switching Frequency | | | 1.77 | | MHz |
| Boost Converter Current Limit | | | 3 | | A |
| Boost Converter Max In-Rush Current | High Efficiency Mode: Max inductor inrush and startup current after enable | | 4 | | A |
| | Normal Efficiency Mode: Max inductor inrush and startup current after enable | | 1.5 | | |
| CLASS-D CHANNEL | | | | | |
| Output Voltage for Full-Scale Digital Input | | | 6.6 | | V_{RMS} |
| Load Resistance (Load Spec Resistance) | | 3.6 | 8 | | Ω |
| Class-D Frequency | Avg Frequency in Spread-Spectrum Mode | | 384 | | kHz |
| | Fixed Frequency | 44.1 × 8 | 48 × 8 | | |
| Class-D + Boost Efficiency | $P_{OUT} = 3.5W$ (sinewave) ROM Mode 1 | | 80 | | % |
| | $P_{OUT} = 0.5W$ (sinewave) ROM Mode 1 | | 87 | | |
| Class-D Output Current Limit (Short Circuit Protection) | VBOOST = 8.5 V, OUT– shorted to VBAT, VBOOST, GND | | 6 | | A |
| Class-D Output Offset Voltage in Digital Input Mode | | -2.5 | | 2.5 | mV |
| Programmable Channel Gain Accuracy | | | ±0.5 | | dB |
| Mute Attenuation | Device in shutdown or device in normal operation and muted | | 150 | | dB |
| VBAT Power Supply Rejection Ratio (PSRR) | Ripple of 200 mVpp at 217 Hz | | 110 | | dB |
| AVDD Power Supply Rejection Ratio (PSRR) | Ripple of 200 mVpp at 217 Hz | | 99 | | dB |
| THD+N | 1 kHz, $P_{OUT} = 0.1W$ | | 0.0041 | | % |
| | 1 kHz, $P_o = 0.5W$ | | 0.0036 | | |
| | 1 kHz, $P_o = 1W$ | | 0.0035 | | |
| | 1 kHz, $P_o = 3W$ | | 0.02 | | |
| Output Integrated Noise (20Hz-20kHz) - 8 Ω | A-weighted filter, DAC modulator switching | | 15.9 | | μV |
| Signal-to-Noise Ratio | Referenced to 1% THD+N at output, A-weighted | | 110.6 | | dB |
| Max Output Power, 3-A Current Limit | THD+N=1%, 8- Ω Load | | 3.7 | | W |
| | THD+N=1%, 6- Ω Load | | 4.5 | | |
| | THD+N=1%, 4- Ω Load | | 5 | | |
| Startup Pop | Digital Input, A-weighted output | | 10 | | mV |
| Output Impedance in Shutdown | /RESET = 0 V | | 10 | | k Ω |
| Startup Time | Time taken from end of configuring device in ROM mode1/2 to speaker output signal in SPI mode running at 25 MHz with 48 ksp/s input | | 8 | | mS |
| Shutdown Time | Measured from time when device is programmed in software shutdown mode | | 100 | | μS |

Electrical Characteristics (continued)

$V_{BAT} = 3.6V$, $AVDD = DVDD = IOVDD = 1.8V$, $\overline{RESET} = IOVDD$, Gain = 16.4 dB, ERC = 14ns, Boost Inductor = 2.2 μH , $R_L = 8\ \Omega + 33\ \mu H$, 1-kHz input frequency, 48- kHz sample rate for digital input, Class-H Boost Enabled, $T_A = 25^\circ C$, ILIM = 3 A (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|--------------|-------|------------|---------|
| CURRENT SENSE | | | | | | |
| Current Sense Full Scale | Peak current which will give full scale digital output 8- Ω load | | 1.25 | | A_{PEAK} | |
| | Peak current which will give full scale digital output 6- Ω load | | 1.48 | | | |
| | Peak current which will give full scale digital output 4- Ω load | | 1.76 | | | |
| Current Sense Accuracy | $I_{OUT} = 354\ mA_{RMS}$ (1 W) | | 1 | | % | |
| VOLTAGE SENSE | | | | | | |
| Voltage Sense Full Scale | Peak voltage which will give full scale digital output | | 9.353 | | V_{PEAK} | |
| Voltage Sense Accuracy | $V_{OUT} = 2.83\ V_{rms}$ (1 W) | | 1 | | % | |
| INTERFACE | | | | | | |
| Voltage and Current Sense Data Rate | | TDM/1 ² S | 48 | | kHz | |
| Voltage and Current Sense ADC OSR | | TDM/1 ² S | 64 | | OSR | |
| F_{MCLK} | MCLK frequency | | 0.512 | 49.15 | | MHz |
| POWER CONSUMPTION | | | | | | |
| Power Consumption with Digital Input and Speaker Protection Disabled (ROM MODE 1) | From VBAT, PLL on, no signal | | 3 | | mA | |
| | From AVDD, PLL on, no signal | | 3 | | mA | |
| | From DVDD, PLL on, no signal | | 7.2 | | mA | |
| Power Consumption with Digital Input and Speaker Protection Enabled | From VBAT, PLL on, no signal | | 4 | | mA | |
| | From AVDD, PLL on, no signal | | 5.1 | | mA | |
| | From DVDD, PLL on, no signal | | 22 | | mA | |
| Power Consumption in Hardware Shutdown | From VBAT, /RESET = 0 | | 0.1 | | μA | |
| | From AVDD, /RESET = 0 | | 0.2 | | μA | |
| | From DVDD, /RESET = 0 | | 2 | | μA | |
| Power Consumption in Software Shutdown See Low Power Sleep | From VBAT | | 0.1 | | μA | |
| | From AVDD | | 0.1 | | μA | |
| | From DVDD | | 9.7 | | μA | |
| DIGITAL INPUT / OUTPUT | | | | | | |
| V_{IH} | High-Level Digital Input Voltage | All digital pins except SDA and SCL, IOVDD = 1.8-V operation | 0.65 × IOVDD | | V | |
| V_{IL} | Low-Level Digital input Voltage | | 0.35 × IOVDD | | V | |
| V_{IH} | High-Level Digital Input Voltage | All digital pins except SDA and SCL, IOVDD = 3.3-V operation | 2 | | V | |
| V_{IL} | Low-Level Ddigital Input Voltage | | 0.45 | | V | |
| V_{OH} | High-Level Digital Output Voltage | All digital pins except SDA and SCL, IOVDD = 1.8-V operation For $I_{OL} = 2\ mA$ and $I_{OH} = -2\ mA$ | IOVDD – 0.45 | | V | |
| V_{OL} | Low-Level Digital Output Vvoltage | | 0.45 | | V | |
| V_{OH} | High-Level Digital Output Voltage | All digital pins except SDA and SCL, IOVDD = 3.3-V operation For $I_{OL} = 2\ mA$ and $I_{OH} = -2\ mA$ | 2.4 | | V | |
| V_{OL} | Low-Level Digital Output Voltage | | 0.4 | | V | |
| I_{IH} | High-Level Digital Input Leakage Current | Input = IOVDD | -5 | 0.1 | 5 | μA |
| I_{IL} | Low-Level Digital Input Leakage Current | Input = Ground | -5 | 0.1 | 5 | μA |
| MISCELLANEOUS | | | | | | |
| T_{TRIP} | Thermal Trip Point | | 140 | | $^\circ C$ | |

7.6 I²C Timing Requirements

For I²C interface signals over recommended operating conditions (unless otherwise noted). See [Figure 1](#)⁽¹⁾

| PARAMETER | | STANDARD-MODE | | FAST-MODE | | UNIT |
|---------------------|--|---------------|------|---------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f _{SCL} | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz |
| t _{HD;STA} | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4 | | 0.6 | | μs |
| t _{LOW} | LOW Period of the SCL Clock | 4.7 | | 1.3 | | μs |
| t _{HIGH} | HIGH Period of the SCL Clock | 4 | | 0.6 | | μs |
| t _{SU;STA} | Setup Time for a Repeated START Condition | 4.7 | | 0.6 | | μs |
| t _{HD;DAT} | Data Hold Time: For I ² C Bus Devices | 0 | 3.45 | 0 | 0.9 | μs |
| t _{SU;DAT} | Data Setup Time | 250 | | 100 | | ns |
| t _r | SDA and SCL Rise Time | | 1000 | 20 + 0.1 × Cb | 300 | ns |
| t _f | SDA and SCL Fall Time | | 300 | 20 + 0.1 × Cb | 300 | ns |
| t _{SU;STO} | Setup Time for STOP Condition | 4 | | 0.6 | | μs |
| t _{BUF} | Bus Free Time Between a STOP and START Condition | 4.7 | | 1.3 | | μs |
| C _b | Capacitive Load for Each Bus Line | | 400 | | 400 | pF |

(1) All timing specifications are measured at characterization but not tested at final test.

7.7 SPI Timing Requirements

For SPI interface signals over recommended operating conditions (unless otherwise noted). See [Figure 2](#)⁽¹⁾

| PARAMETER | | IOVDD = 1.8 V | | IOVDD = 3.3 V | | UNIT |
|-----------------------|---------------------------|---------------|-----|---------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t _{sck} | SCLK Period | 40 | | 30 | | ns |
| t _{sckh} | SCLK Pulse Width High | 40 | | 30 | | ns |
| t _{sckl} | SCLK Pulse Width Low | 40 | | 30 | | ns |
| t _{lead} | Enable Lead Time | 40 | | 30 | | ns |
| t _{trail} | Enable Trail Time | 40 | | 30 | | ns |
| t _{d;seqxfr} | Sequential Transfer Delay | 40 | | 30 | | ns |
| t _a | Slave DOUT Access Time | | 35 | | 25 | ns |
| t _{dis} | Slave DOUT Disable Time | | 35 | | 25 | ns |
| t _{su} | DIN Data Setup Time | 8 | | 8 | | ns |
| t _{h;DIN} | DIN Data Hold Time | 8 | | 8 | | ns |
| t _{v;DOUT} | DOUT Data Valid Time | | 35 | | 25 | ns |
| t _r | SCLK Rise Time | | 4 | | 4 | ns |
| t _f | SCLK Fall Time | | 4 | | 4 | ns |

(1) All timing specifications are measured at characterization but not tested at final test.

7.8 I²S/LJF/RJF Timing Requirements (Master Mode)

All specifications at $T_A = -40^{\circ}\text{C}$ to 85°C , IOVDD data sheet limits, V_{IL} and V_{IH} applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted. See [Figure 3](#)⁽¹⁾

| PARAMETER | | | IOVDD = 1.8 V | | IOVDD = 3.3 V | | UNIT |
|-----------------------|--|----------------------------|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| $t_d(\text{WS})$ | BCLK to WCLK delay | 50% of BCLK to 50% of WCLK | | 35 | | 25 | ns |
| $t_d(\text{DO-WS})$ | WCLK to DOUT Delay (For LJF Mode Only) | 50% of WCLK to 50% of DOUT | | 35 | | 25 | ns |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT Delay | 50% of BCLK to 50% of DOUT | | 35 | | 25 | ns |
| $t_s(\text{DI})$ | DIN Setup | | 8 | | 8 | | ns |
| $t_h(\text{DI})$ | DIN Hold | | 8 | | 8 | | ns |
| t_r | Rise Time | 10%-90% Rise Time | | 8 | | 4 | ns |
| t_f | Fall Time | 90%-10% Fall Time | | 8 | | 4 | ns |

(1) All timing specifications are measured at characterization but not tested at final test.

7.9 I²S/LJF/RJF Timing Requirements (Slave Mode)

All specifications at $T_A = -40^{\circ}\text{C}$ to 85°C , IOVDD data sheet limits, V_{IL} and V_{IH} applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted. See [Figure 4](#)⁽¹⁾

| PARAMETER | | | IOVDD = 1.8 V | | IOVDD = 3.3 V | | UNIT |
|-----------------------|--|----------------------------|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| $t_H(\text{BCLK})$ | BCLK High Period | | 40 | | 30 | | ns |
| $t_L(\text{BCLK})$ | BCLK Low Period | | 40 | | 30 | | ns |
| $t_s(\text{WS})$ | (WS) | | 8 | | 8 | | ns |
| $t_h(\text{WS})$ | WCLK Hold | | 8 | | 8 | | ns |
| $t_d(\text{DO-WS})$ | WCLK to DOUT Delay (For LJF Mode Only) | 50% of WCLK to 50% of DOUT | | 35 | | 25 | ns |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT Delay | 50% of BCLK to 50% of DOUT | | 35 | | 25 | ns |
| $t_s(\text{DI})$ | DIN Setup | | 8 | | 8 | | ns |
| $t_h(\text{DI})$ | DIN Hold | | 8 | | 8 | | ns |
| t_r | Rise Time | 10%-90% Rise Time | | 8 | | 4 | ns |
| t_f | Fall Time | 90%-10% Fall Time | | 8 | | 4 | ns |

(1) All timing specifications are measured at characterization but not tested at final test.

7.10 DSP Timing Requirements (Master Mode)

All specifications at $T_A = -40^{\circ}\text{C}$ to 85°C , IOVDD data sheet limits, V_{IL} and V_{IH} applied, V_{OL} and V_{OH} measured at datasheet limits, lumped capacitive load of 20 pF on output pins unless otherwise noted. See Figure 5⁽¹⁾

| PARAMETER | | | IOVDD = 1.8 V | | IOVDD = 3.3 V | | UNIT |
|-----------------------|--------------------|----------------------------|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| $t_d(\text{WS})$ | BCLK to WCLK delay | 50% of BCLK to 50% of WCLK | | 35 | | 25 | ns |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT delay | 50% of BCLK to 50% of DOUT | | 35 | | 25 | ns |
| $t_s(\text{DI})$ | DIN Setup | | 8 | | 8 | | ns |
| $t_h(\text{DI})$ | DIN Hold | | 8 | | 8 | | ns |
| t_r | Rise Time | 10%-90% Rise Time | | 8 | | 4 | ns |
| t_f | Fall Time | 90%-10% Fall Time | | 8 | | 4 | ns |

(1) All timing specifications are measured at characterization but not tested at final test.

7.11 DSP Timing Requirements (Slave Mode)

All specifications at 25°C , IOVDD = 1.8 V. See Figure 6⁽¹⁾

| PARAMETER | | | IOVDD=1.8V | | IOVDD=3.3V | | UNIT |
|-----------------------|--|----------------------|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| $t_H(\text{BCLK})$ | BCLK High Period | | 40 | | 30 | | ns |
| $t_L(\text{BCLK})$ | BCLK Low Period | | 40 | | 30 | | ns |
| $t_s(\text{WS})$ | WCLK setup | | 8 | | 8 | | ns |
| $t_h(\text{WS})$ | WCLK Hold | | 8 | | 8 | | ns |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT Delay (For LJJ Mode Only) | 50% BCLK to 50% DOUT | | 35 | | 25 | ns |
| $t_s(\text{DI})$ | DIN Setup | | 8 | | 8 | | ns |
| $t_h(\text{DI})$ | DIN Hold | | 8 | | 8 | | ns |
| t_r | Rise Time | 10%-90% Rise Time | | 8 | | 4 | ns |
| t_f | Fall Time | 90%-10% Fall Time | | 8 | | 4 | ns |

(1) All timing specifications are measured at characterization but not tested at final test.

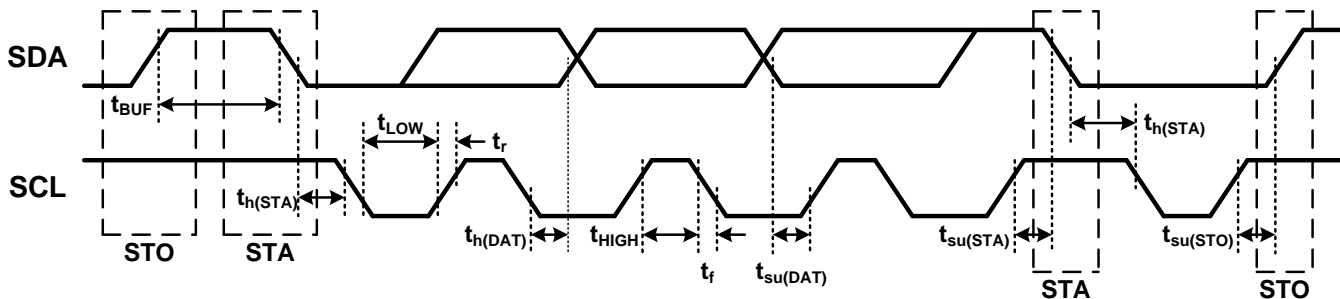
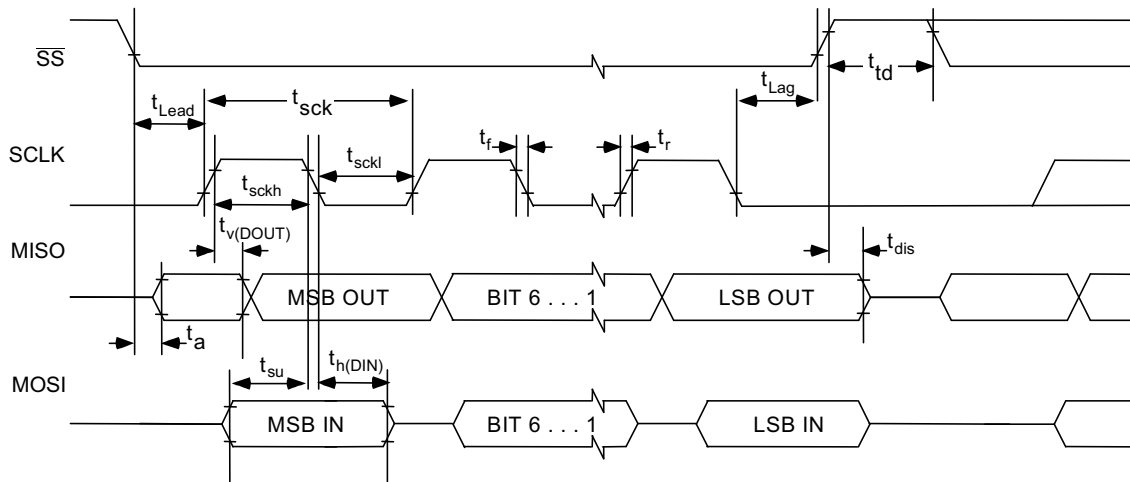
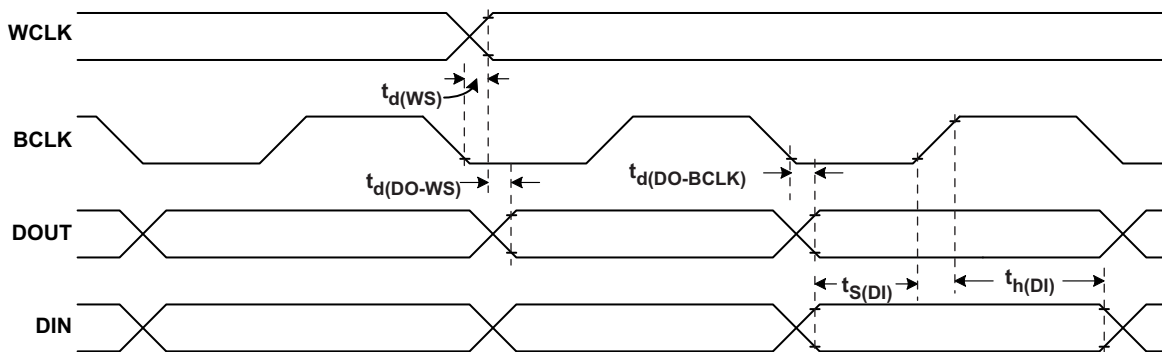
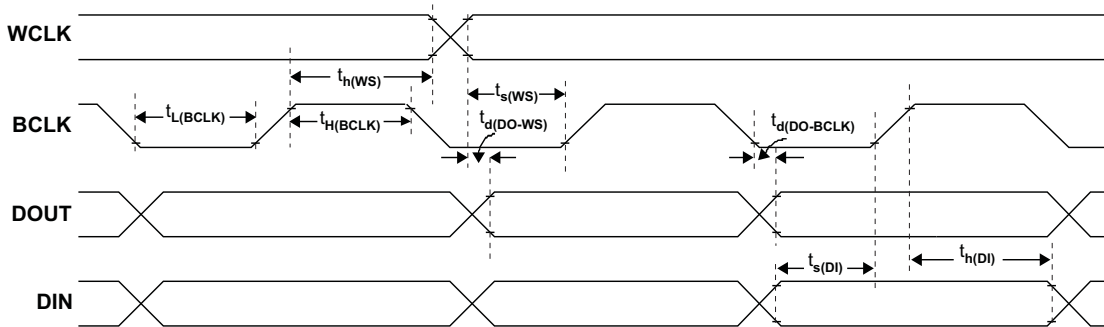


Figure 1. I²C Timing


Figure 2. SPI Interface Timing Diagram

Figure 3. I²S/LJF/RJF Timing in Master Mode

Figure 4. I²S/LJF/RJF Timing in Slave Mode

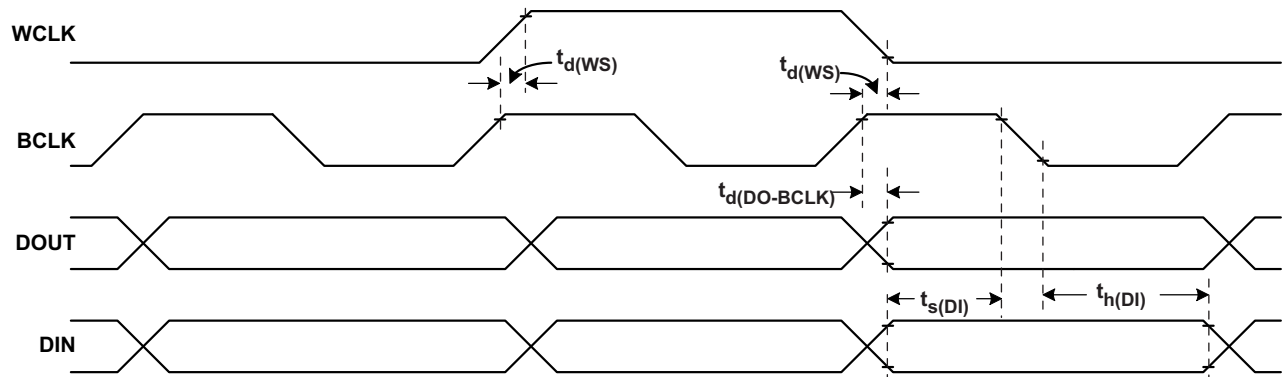


Figure 5. DSP Timing in Master Mode

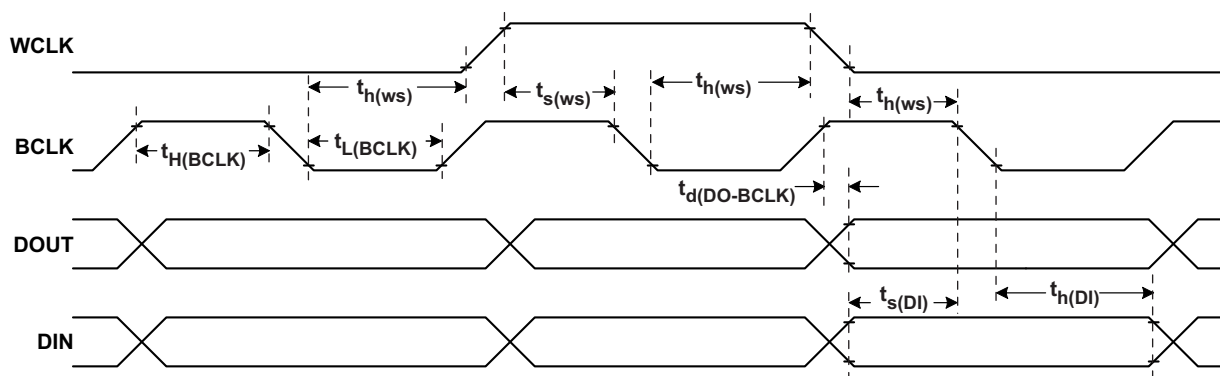


Figure 6. DSP Timing in Slave Mode

7.12 Typical Characteristics

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, $\overline{\text{RESET}}$ = IOVDD, $R_L = 8 \Omega + 33 \mu\text{H}$, I²S Digital Input, ROM Mode 1 (Unless Otherwise Noted).

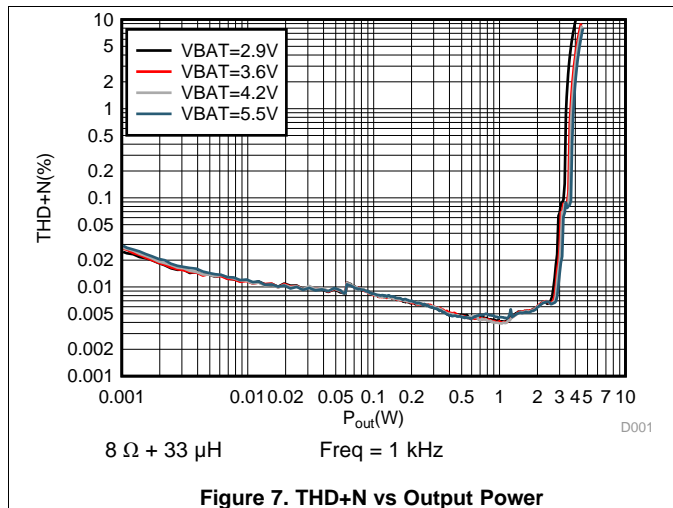


Figure 7. THD+N vs Output Power

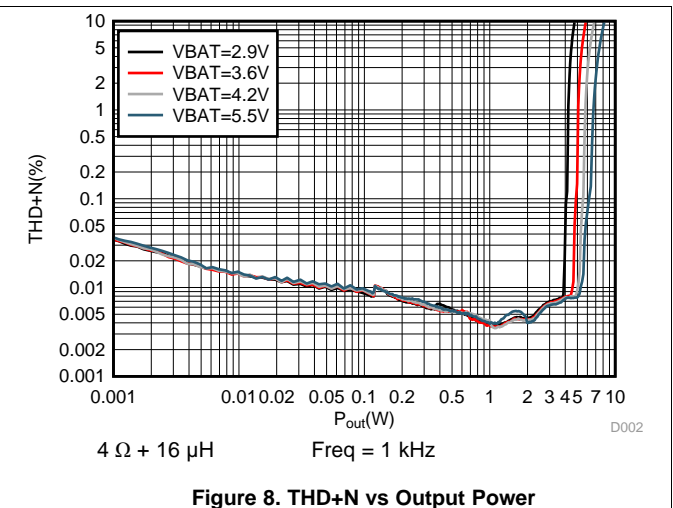


Figure 8. THD+N vs Output Power

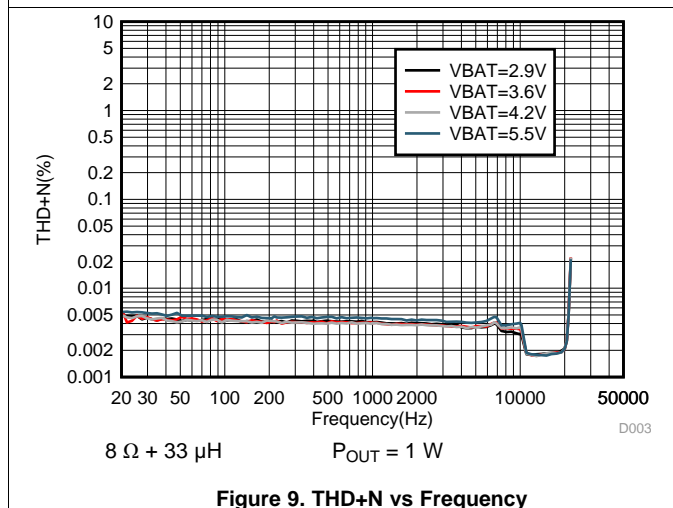


Figure 9. THD+N vs Frequency

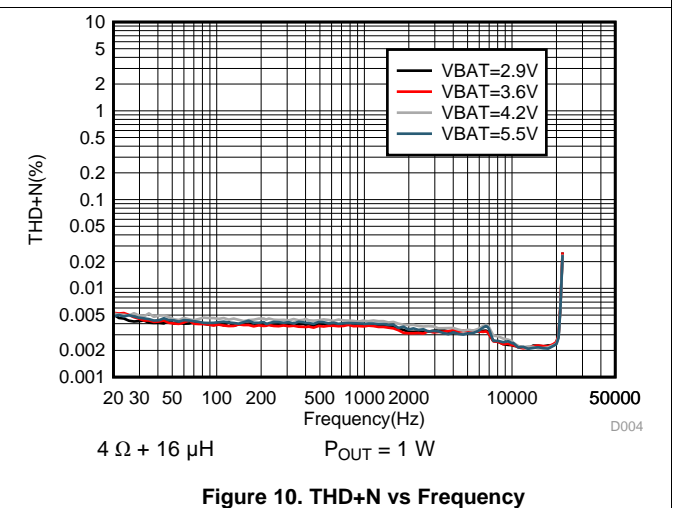


Figure 10. THD+N vs Frequency

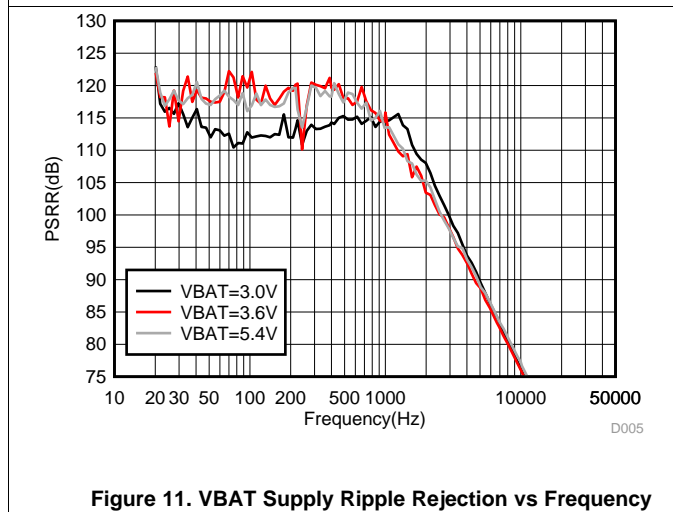


Figure 11. VBAT Supply Ripple Rejection vs Frequency

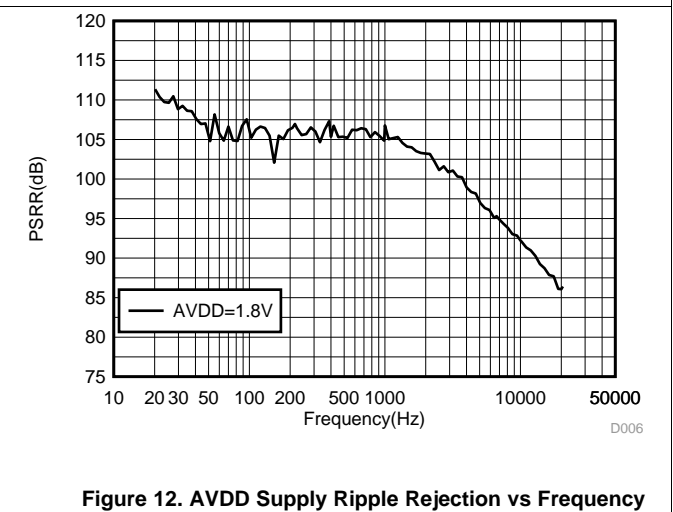


Figure 12. AVDD Supply Ripple Rejection vs Frequency

Typical Characteristics (continued)

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, $\overline{\text{RESET}}$ = IOVDD, $R_L = 8 \Omega + 33 \mu\text{H}$, I²S Digital Input, ROM Mode 1 (Unless Otherwise Noted).

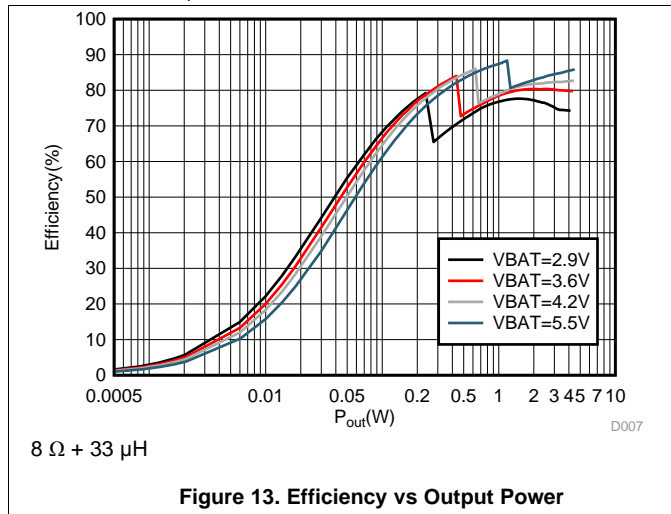


Figure 13. Efficiency vs Output Power

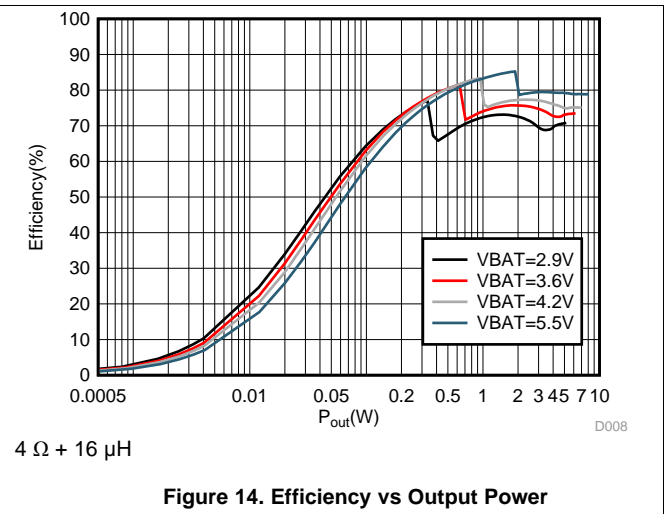


Figure 14. Efficiency vs Output Power

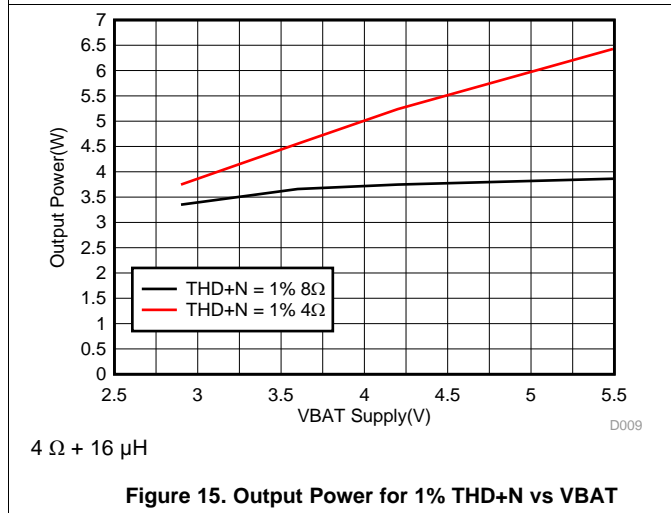


Figure 15. Output Power for 1% THD+N vs VBAT

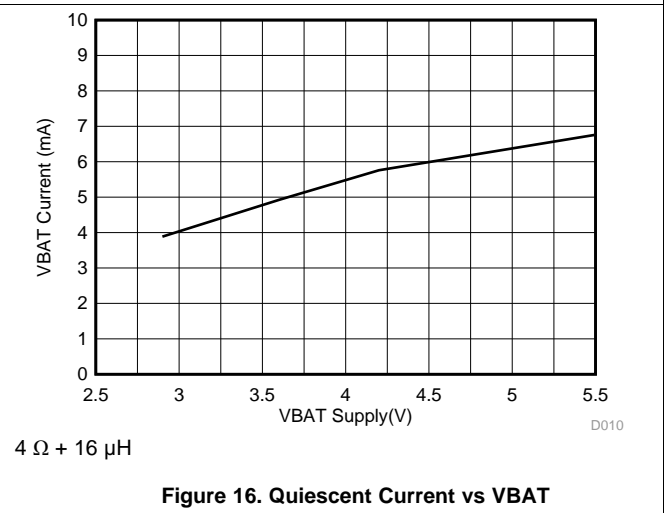


Figure 16. Quiescent Current vs VBAT

8 Parameter Measurement Information

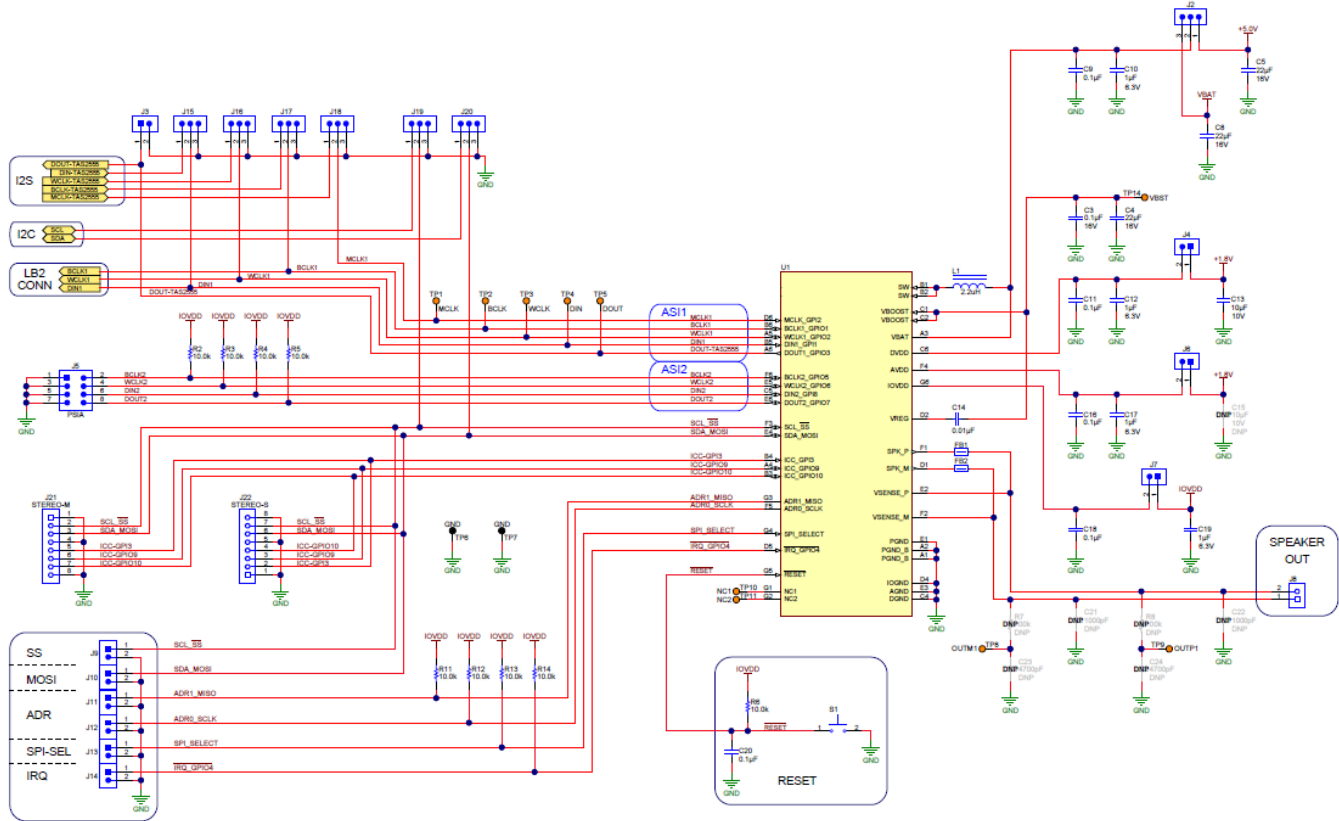


Figure 17. TAS2557 Test Circuit

All typical characteristics for the devices are measured using the bench EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface is used to allow the I²S interface to be driven directly into the SYS-2722. SPEAKER OUT terminal is connected to Audio Precision Analyzer inputs as shown below. There is a differential to single-ended (D2S) filter, with 1st order passive pole at 120 kHz added. This is to ensure high performance Class-D amplifier sees a fully differential matched loading at its outputs and while seeing no measurable degradation in performance due to loading effects of AUX filter on Class-D outputs.

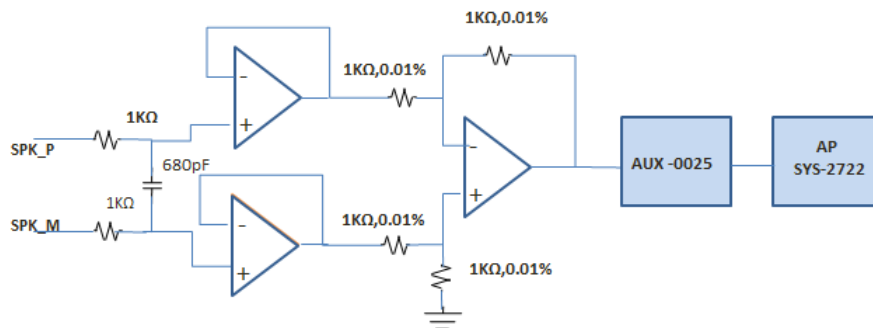


Figure 18. Differential To Single-Ended (D2S) Filter

9 Detailed Description

9.1 Overview

The TAS2557 device is a state-of-the-art Class-D audio amplifier which is a full system on a chip (SoC). The device features a ultra low-noise audio DAC and Class-D power amplifier which incorporates speaker voltage and current sensing feedback. An on-chip, low-latency DSP supports Texas Instruments' Smart Amp speaker protection algorithms to maximize loudness while maintaining safe speaker conditions. A smart integrated multi-level Class-H boost converter maximizes system efficiency at all times by tracking the required output voltage. The TAS2557 drives up to 3.8 W from a 4.2-V supply into an 8- Ω speaker with 1% THD, or up to up 5.7 W into a 4- Ω speaker with 1% THD.

The TAS2557, with final processed digital output, can also be used to increase loudness and clarity in both Noise Canceling / Echo Cancelling speaker phone applications as well as for music or other sound applications. The TAS2557 accepts input audio data rates from 8 kHz to 96 kHz using ROM modes to fully support both speakerphone and music applications. When speaker protection system is running the maximum sampling rate is limited to 48 kHz.

The multi-level Class-H boost converter generates the Class-D amplifier supply rail. When the audio signal requires a output power below VBAT, the boost improves system efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When higher audio output power is required, the boost quickly activates and provides a much louder and clearer signal than can be achieved in any standard amplifier speaker system design approach. A boost inductor of 1 μ H can be used with a slight increase in boost ripple.

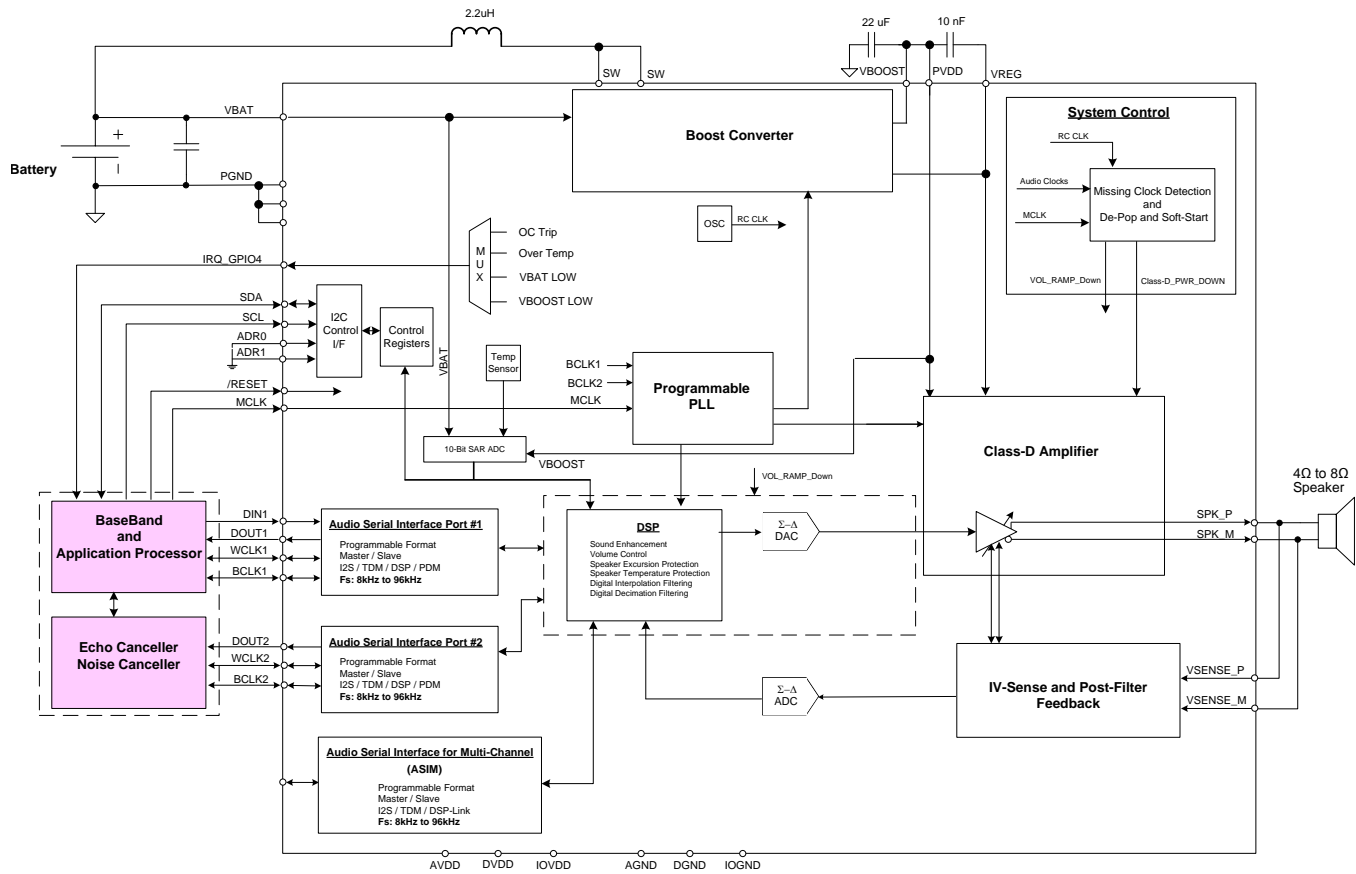
On-chip brownout detection system shutdown down audio at the user configurable threshold to avoid undesired system reset. In addition, an AGC can be selected to minimize clipping events when a lower power supply voltage is provided to the Class-D speaker driver. When this supply voltage drops below the proper level then under-voltage protection will be tripped. All protection statuses are available via register reads.

The Class-D output switching frequency is synchronous with the digital input audio sample rate to avoid left and right PWM frequency differences from beating in stereo applications. PWM Edge rate control and Spread Spectrum features are available if further EMI reduction is desired in the user's system.

The interrupt request pin (IRQ) indicates a device error condition. The interrupt flag condition or conditions are selectable via I²C and include: thermal overload, Class-D over-current, VBAT level low, VBOOST level low, and PLL out-of-lock conditions. The IRQ signal is active-high for an interrupt request and low during normal operation. This behavior can be changed by a register setting to tri-state the pin during normal operation to allow the IRQ pin to be tied in parallel with other active-low interrupt request pins on other devices in the system.

Stereo configuration can be achieved with two TAS2557 devices by using the ADR0_SCLK and ADR1_MISO pins to set different I²C addresses in I²C mode or the SCL_SSZ chip enable pin in SPI mode. Refer to the [General I²C Operation](#) or [General SPI Operation](#) sections for more details.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 General I²C Operation

The TAS2557 operates as an I²C slave over the IOVDD voltage range. It is adjustable to one of four I²C addresses. This allows multiple TAS2557 devices in a system to connect to the same I²C bus. The I²C pins are fail-safe. If the part is not powered or is in shutdown the I²C pins will not impact the I²C bus allowing it to remain functional.

To configure the TAS2557 for I²C operation set the SPI_SELECT pin to ground. The I²C address can then be set using pins ADR0_SCLK and ADR1_MSIO according to Table 1. The pins configure the two LSB bits of the following 7-bit binary address A6-A0 of 10011xx. This permits the I²C address of TAS2557 to be 0x4C(7-bit) through 0x4F(7-bit). For example, if both ADR0_SCLK and ADR1_MSIO are connected to ground the I²C address for the TAS2557 would be 0x4C(7-bit). This is equivalent to 0x98 (8-bit) for writing and 0x99 (8-bit) for reading.

Table 1. I²C Address Selection

| ADR0_SCLK Pin Connection | ADR1_MSIO Pin Connection | I ² C Device Address |
|--------------------------|--------------------------|---------------------------------|
| GND | GND | 0x4C |
| IOVDD | GND | 0x4D |
| GND | IOVDD | 0x4E |
| IOVDD | IOVDD | 0x4F |

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The corresponding pins on the TAS2557 for the two signals are SDA_MOSI and SCL_SSZ. The bus transfers data serially, one bit at a time. The address and data (8-bit) bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 19 shows a typical sequence.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 660 Ω and 4.7 kΩ. Do not allow the SDA and SCL voltages to exceed the device supply voltage, IOVDD.

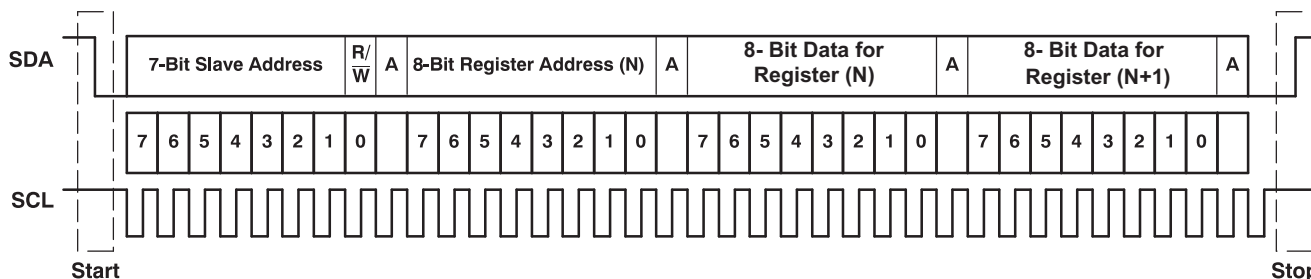


Figure 19. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 19 shows a generic data transfer sequence.

9.3.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2557 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2557 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

9.3.3 Single-Byte Write

As shown in Figure 20, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TAS2557 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

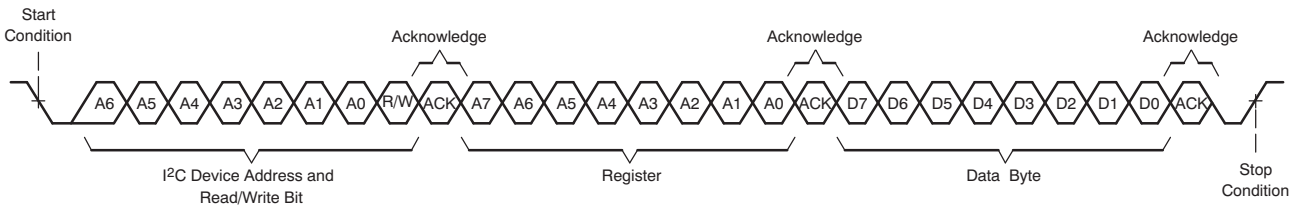


Figure 20. Single-Byte Write Transfer

9.3.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2557 as shown in Figure 21. After receiving each data byte, the device responds with an acknowledge bit.

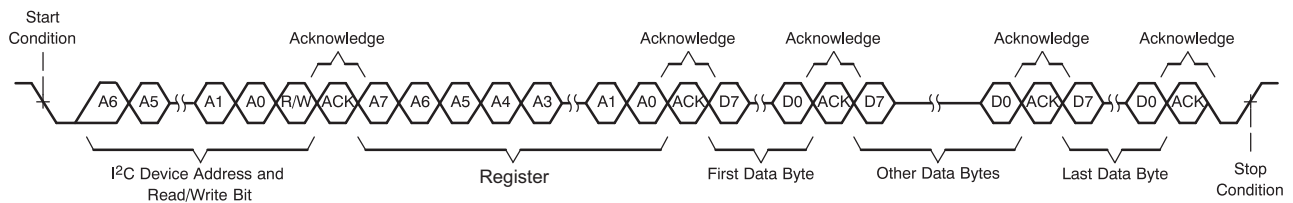


Figure 21. Multiple-Byte Write Transfer

9.3.5 Single-Byte Read

As shown in Figure 22, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2557 address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the TAS2557 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2557 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

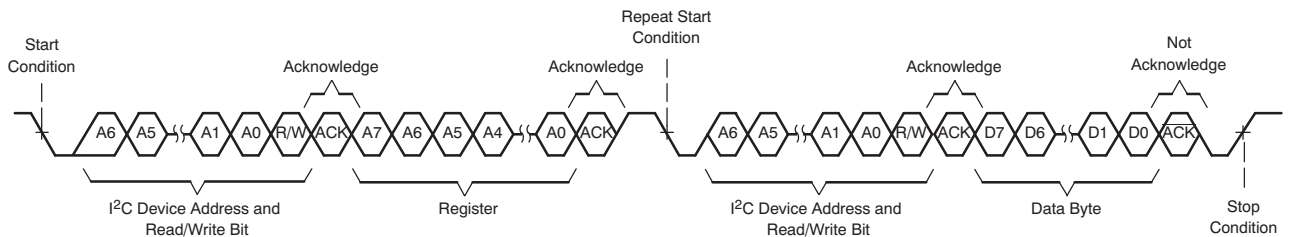


Figure 22. Single-Byte Read Transfer

9.3.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2557 to the master device as shown in Figure 23. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

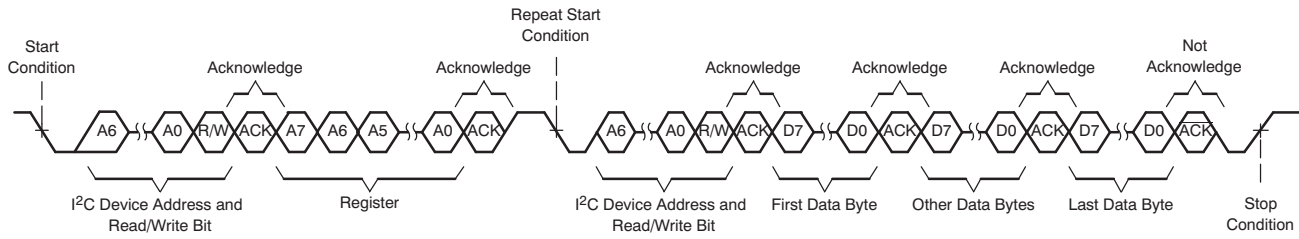


Figure 23. Multiple-Byte Read Transfer

9.3.7 General SPI Operation

The TAS2557 operates as an SPI slave over the IOVDD voltage range.

9.3.8 Class-D Edge Rate Control

The edge rate of the Class-D output is controllable via I²C as shown in Table 2. This allows adjusting the switching edge rate of the Class-D amplifier, trading off efficiency for lower EMI. The default edge rate of 14ns passes EMI testing and is recommend but may be changed if required.

Table 2. Class-D Edge Rate Control

| SPK_GAIN_EDGE[2:0] (EDGE_RATE) | t _R AND t _F (TYPICAL) |
|-----------------------------------|--|
| 000 | Reserved |
| 001 | Reserved |
| 010 | 29 ns |
| 011 | 25 ns |
| 100 | 14 ns (default) |
| 101 | 13 ns |
| 110 | 12 ns |
| 111 | 11 ns |

9.3.9 IV Sense

The TAS2557 provides speaker voltage and current sense for real-time monitoring of loudspeaker behavior. The VSENSE_P and VSENSE_N pins should be connected after any ferrite bead filter (or directly to the SPK_P and SPK_N connections if no EMI filter is used). The V-Sense terminals are used to eliminate IR drop error due to packaging, PCB interconnect, and ferrite bead filter resistance. The V-sense terminals are also used to close the Class-D feedback loop post filter. This Post-Filter Feedback (PFFB) minimizes the THD introduced from the filter-beads used in the system. Any interconnect resistance or non-linearities after the V-Sense terminals connection point will not be corrected for. Therefore, it is advised to connect the sense connections as close to the load as possible.

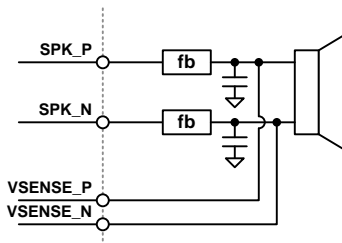


Figure 24. V-Sense Connections

The I-Sense can be configured for three ranges and shown in Table 3. This should be set appropriately based on the DC resistance of the speaker. I-Sense and V-Sense can additionally be powered down as shown in Table 4 and Table 5. When powered down, the device will return null samples for the powered down sense channels.

Table 3. I-Sense Current Range

| SNS_CTRL[2:1] (ISNS_SCALE) | Full Scale Current | Speaker Load Impedance |
|----------------------------|--------------------|------------------------|
| 00 | 1.25 A (default) | 8 Ω |
| 01 | 1.5 A | 6 Ω |
| 10 | 1.75 A | 4 Ω |
| 11 | Reserved | Reserved |

Table 4. I-Sense Mute

| MUTE[1] (MUTE_ISNS) | Setting |
|---------------------|-----------------------------|
| 0 | I-Sense is active (default) |
| 1 | I-Sense channel is muted |

Table 5. V-Sense Mute

| MUTE[0] (MUTE_VSNS) | Setting |
|---------------------|-----------------------------|
| 0 | V-Sense is active (default) |
| 1 | V-Sense channel is muted |

Table 6. I-Sense Power Down

| POWER_2[1] (PWR_ISNS) | Setting |
|-----------------------|-----------------------------|
| 0 | I-Sense is active (default) |
| 1 | I-Sense is powered down |

Table 7. V-Sense Power Down

| POWER_2[0] (PWR_VSNS) | Setting |
|-----------------------|-----------------------------|
| 0 | V-Sense is active (default) |
| 1 | V-Sense is powered down |

9.3.10 Battery Tracking AGC

The TAS2557 monitors the battery voltage and audio signal to automatically decrease gain when the battery voltage is low and audio output power is high. This provides louder audio while preventing early shutdown at end-of-charge battery voltage levels. The battery tracking AGC starts to attenuate the signal once the voltage at the Class-D output exceeds V_{LIM} for a given battery voltage (VBAT). If the Class-D output voltage is below the V_{LIM} value, no attenuation occurs. If the Class-D output exceeds the V_{LIM} value the AGC starts to attack the signal and reduce the gain until the output is reduced to V_{LIM} . Once the signal returns below V_{LIM} plus some hysteresis the gain reduction decays. The V_{LIM} is constant above the user configurable inflection point. Below the inflection point the V_{LIM} is reduced by a user configurable slope in relation to the battery voltage. The attack time, decay time, inflection point and $V_{LIM}/VBAT$ slope below the inflection point are user configurable. The parameters for the battery tracking AGC are part of the DSP core and can be set using the [PurePath™ Console 3 Software TAS2557 Application](#) software for the TAS2557 part under the Device Control Tab. Below a VBAT level of 2.9 V, the boost will turn on to ensure correct operation but results in increased current consumption. The device is functional until the set brownout level is reached and the device shuts down. The minimum brownout voltage is 2.7 V.

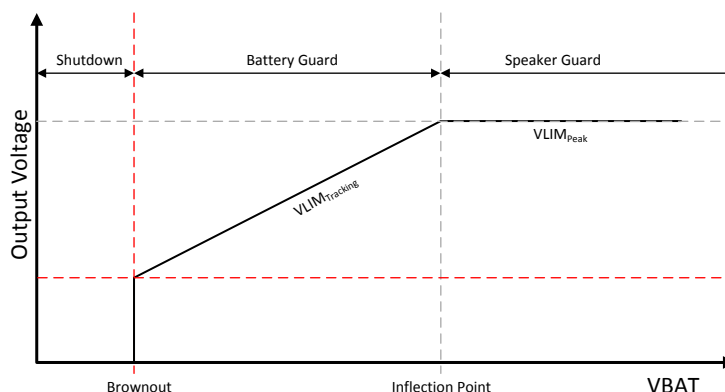


Figure 25. VLIM versus Supply Voltage (VBAT)

9.3.11 Boost Control

9.3.11.1 Boost Mode

The TAS2557 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using [Table 8](#).

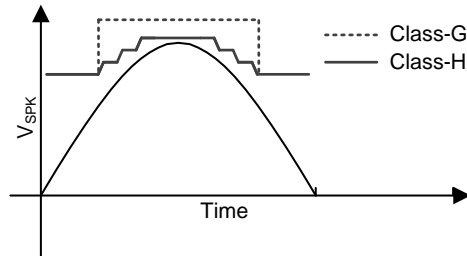


Figure 26. Boost Mode Signal Tracking Example

Table 8. Boost Mode

| SPK_CTRL[4] (BST_MODE) | Boost Mode |
|------------------------|---------------------------------|
| 0 | Class-H - High efficiency |
| 1 | Class-G - Low in-rush (default) |

9.3.11.2 Configurable Boost Current Limit (ILIM)

The TAS2557 device has a configurable boost current limit (ILIM). The default current limit is 3 A but this limit may be set lower based on selection of passive components connected to the boost. The TAS2557 device supports 4 different boost limits.

Table 9. Current Limit Settings

| BOOST_CTRL_2[1:0] (BST_ILM) | BOOST CURRENT LIMIT (A) |
|-----------------------------|-------------------------|
| 00 | 1.5 |
| 01 | 2.0 |
| 10 | 2.5 |
| 11 | 3.0 (default) |

9.3.12 Thermal Fold-back

The TAS2557 monitors the die temperature and prevents it from going over a set limit. When enabled, an internal controller will automatically adjust the signal path gain to prevent the die temperature from exceeding this limit. This allows instantaneous peak power to be delivered to the speaker while limiting the continuous power to prevent thermal shutdown. The configuration parameters for the thermal fold-back are part of the DSP core and can be set using the [PurePath™ Console 3 Software TAS2557 Application](#) software for the TAS2557 part under the Device Control Tab.

9.3.13 Fault Protection

The TAS2557 has several protection blocks to prevent damage. Use of these blocks including how to resume from a fault are presented in this section.

9.3.13.1 Speaker Over-Current

The TAS2557 has an integrated over-current protection that is enabled once the Class-D is powered up. Large currents in the range of 3-5 A on the Class-D output will trigger an over-current fault. Once the fault is detected, the TAS2557 disables the audio channel and powers down the Class-D amplifier. When an over-current event occurs, a status flag INT_OC is set. This register is sticky, and the bit remains high until the bit is read or the device is reset. The over-current event can also be used to generate an interrupt if required. Refer to [IRQs and Flags](#) section for more details. To re-enable the audio channel after a fault the Class-D, the device must be hardware or software reset and configuration must be re-loaded.

9.3.13.2 Analog Under-Voltage

The TAS2557 has integrated undervoltage protection on the analog power supply lines AVDD and VBAT. The undervoltage limit fault is triggered when AVDD is less than 1.5 V or when VBAT is less than 2.4 V. Once the fault is detected the TAS2557 will disable the audio channel and power down the Class-D amplifier. When an under-voltage event occurs, a status flag INT_UV is set. This register is sticky and the bit will remain high until the bit is read or the device is reset. The undervoltage event can also be used to generate an interrupt if required. Refer to [IRQs and Flags](#) section for more details. To re-enable the audio channel after a fault, the Class-D must be re-enabled by setting PWR_SPK high. All other configurations are preserved and the audio channel will power up with the last configured settings.

9.3.13.3 Die Over-Temperature

The TAS2557 has an integrated over-temperature protection that is enabled once the Class-D is powered up. If the device internal junction temperature exceeds the safe operating region it will trigger the over-temperature fault. Once the fault is detected the TAS2557 disables the audio channel and powers down the Class-D amplifier. The device waits until the user reads the over-temperature flag INT_OT to re-enable the Class-D amplifier if the junction temperature returns into a safe operating region. When an over-temperature event occurs, a status flag INT_OT is set. This register is sticky and the bit will remain high for as long as it is not read, or the device is not reset. The over-temperature event can also be used to generate an interrupt if required. Refer to [IRQs and Flags](#) section for more details. The over-temperature automatic re-enable can be disabled by setting OT_RT signal. If the automatic re-enable is disabled, the Class-D must be re-enabled by setting PWR_SPK high after the over-temperature fault. All other configurations are preserved and the audio channel will power up with the last configured settings.

9.3.13.4 Clocking Faults

The TAS2557 has two clock error detection blocks. The first is on the Audio Serial Interfaces (ASI). If a clock error is detected on the ASI interfaces, audio artifacts can occur at the Class-D output. When enabled, the ASI clock error detection can mute the device and shutdown the Class-D and DSP core. The clock error detection block is enabled by setting register signal CE1_EN. The ASI1 or ASI2 clocks can be routed to the block for detection using register CE1_IC. Additionally, the clock error can be routed to an interrupt pin, and the sticky bit INT_CLK1 indicates whether the clock error occurred. The second clock error detection block can monitor the DAC, ADC, and PLL clocks. When a clock error is detected, the output is soft-muted and the Class-D powered down. This clock error detection is enabled using bit signal CE2_EN and can be routed to the interrupt pin. It is indicated in the sticky bit INT_CLK2.

When a clocking error occurs, the following sequence should be performed to restart the device.

- Clear the clock error interrupts by reading the sticky flags at registers INT_STICKY_2 and INT_STICKY_2
- Clear the power error signal PWR_ERR in register POWER_1

9.3.14 Brownout

The TAS2557 has an integrated brownout system to shutdown the device when the battery voltage drops to an insufficient level. This user configurable level can be set under Device Control in the [PurePath™ Console 3 Software TAS2557 Application](#). When brownout event occurs a status flag INT_BO is set. This register is sticky, and the bit remains high until the bit is read or the device is reset. The brownout event can also be used to generate an interrupt if required. Refer to [IRQs and Flags](#) section for more details. Once the battery voltage drops below the defined threshold, the following actions occur.

- The audio playback is muted in a soft-stepping manner
- DSP, clock dividers, and analog blocks are powered down

- Sticky bit INT_BO is set

Once the host is aware of the brownout, it should set PWR_ERR register signal low to put the TAS2557 device in software shutdown and enters low power mode. Once the battery supply is stable above the defined brownout threshold the host can re-enable the device using the power control registers POWER_1 and POWER_2.

9.3.15 Spread Spectrum vs Synchronized

The Class-D switching frequency can be selected to work in two different modes of operations. This configuration needs to be done before powering up the audio channel. The first is a synchronized mode where the Class-D frequency is synchronized to the audio input sample rate. This is the default mode of operation and should be used in stereo applications to avoid inter-modulation beating of the Class-D frequency from multiple chips. The Class-D switching frequency in this mode can be configured as 384 kHz or 352.8 kHz. The 384 kHz frequency is the default mode of operation and can be used for input signals running on clock rates of 48 kHz or its sub-multiples. For input signals running on clock rate of 44.1 kHz and its sub-multiples, the switching frequency can be selected as 352.8 kHz using [Table 10](#).

The second mode uses the internal oscillator to generate the ramp clock. This is enabled using [Table 11](#). This mode is generally used with [Table 12](#) enabled for spread-spectrum. Spread-spectrum is used to reduce wideband spectral content improving EMI emissions radiated by the speaker. In this mode, the Class-D switching frequency can varies $\pm 5\%$ or $\pm 10\%$ as set by [Table 13](#) about the set frequency [Table 10](#).

The configuration for this block should be set using the [PurePath™ Console 3 Software TAS2557 Application](#) software for the TAS2557 part under the Device Control Tab.

Table 10. Ramp Clock Frequency

| RAMP_CTRL[5:4] (RAMP_FREQ) | Setting |
|----------------------------|-------------------|
| 00 | 384 kHz (default) |
| 01 | 352.8 kHz |
| 10 | Reserved |
| 11 | Reserved |

Table 11. Ramp Clock Source

| RAMP_DSP[7] (RAMP_SRC) | Setting |
|------------------------|---|
| 0 | Sync Mode - ramp generated from digital audio clock (default) |
| 1 | Fixed Frequency Mode(FFM) - ramp generated from internal oscillator |

Table 12. Ramp Clock SSM

| SSM_CTRL[0] (SSM_EN) | Setting |
|----------------------|------------------------------------|
| 0 | SSM mode is disabled |
| 1 | SSM mode is enabled ⁽¹⁾ |

(1) Ramp clock source must be from internal oscillator

Table 13. Ramp SSM Mode

| RAMP_CTRL[1:0] (RAMP_FREQMOD) | Setting |
|-------------------------------|--|
| 00 | Reserved |
| 01 | SSM mode enabled with ramp frequency modulated for $\pm 5\%$ (default) |
| 10 | SSM mode enabled with ramp frequency modulated for $\pm 10\%$ |
| 11 | Reserved |

9.3.16 IRQs and Flags

Internal device flags such as over-current, under-voltage, etc. can be routed as interrupts. The device has 4 interrupts (INT1 - INT4) that can be routed to any of the 10 GPIO pins. If more than one flag is assigned to the same interrupt, the interrupt output is the logical OR-ing of all flags. If multiple flag's are assigned to the same interrupt, the host should then query the flags sticky register to determine which event triggered the interrupt. The 10 GPIO pins can be configured for any interrupt and can be configured using GPIOx_PIN registers.

Table 14. Interrupt Registers

| Flag Description | Sticky Register Bit | Register to Route Flag to Interrupt |
|------------------|------------------------|-------------------------------------|
| Over-Current | INT_DET_1[7] (INT_OC) | INT_GEN_1[6:4] (INT_GEN_OC) |
| Under-Voltage | INT_DET_1[6] (INT_UV) | INT_GEN_1[2:0] (INT_GEN_OV) |
| Over-Temperature | INT_DET_1[4] (INT_OT) | INT_GEN_2[2:0] (INT_GEN_OT) |
| Brownout | INT_DET_1[3] (INT_BO) | INT_GEN_3[6:4] (INT_GEN_BO) |
| Clock Lost | INT_DET_1[2] (INT_CL) | INT_GEN_4[2:0] (INT_GEN_CL) |
| SAR Complete | INT_DET_1[1] (INT_SC) | INT_GEN_4[6:4] (INT_GEN_SC) |
| Clock Error 1 | INT_DET_2[3] (INT_CE1) | INT_GEN_2[6:4] (INT_GEN_CE1) |
| Clock Error 2 | INT_DET_2[2] (INT_CE2) | INT_GEN_3[3:0] (INT_GEN_CE2) |

For example, to route the brownout and under-voltage flags to GPIO5 (Pin IRQ_GPIO5) the following register settings would be used. The brownout flag would be routed to INT1 by setting INT_GEN_BO=001, and under-voltage flag would also be routed to INT1 by setting INT_GEN_OV=001. The pin IRQ_GPIO4 would be set to use INT1 by setting GP4_OUT=0x07

9.3.17 Software Reset

The TAS2557 internal logic must be initialized to a known condition for proper device function by doing a software reset. Performing software reset after a hardware reset is mandatory for reliable device boot up. To perform software reset, write high register signal RESET. After reset, all registers are initialized with default values as listed in the [Register Map](#), and no register read/write should be performed within 100us.

9.3.18 PurePath™ Console 3 Software TAS2557 Application

The TAS2557 contains an integrated DSP engine for speaker protection. PurePath™ Console 3 (PPC3) is the software tool used to setup most device configurations and tuning features. Once the software is downloaded and installed from the TI website, the TAS2557 application can be download from within the software. This datasheet refers to options that can be configured using the PPC3 software tool.

PurePath Console 3 is an intuitive graphical user interface (GUI) for characterizing and tuning speakers. Step-by-step wizards guide developers through speaker characterization and system calibration. After characterization, the PPC3 provides visual representations of speaker capabilities and frequency response. Easy to use, real-time tuning information supported via mouse-over and complete process walk-throughs. PPC3 has full access to device registers and is the simplest way to modify device settings, EVM and learning board configuration. From speaker assessment to production, PPC3 is your simple, single development tool.

9.3.19 Operational Modes

9.3.19.1 Hardware Shutdown

The device enters hardware shutdown mode if the RESETZ pin is asserted low. In hardware shutdown mode, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers loose state in this mode and I²C communication is disabled.

If RESETZ is asserted low while audio is playing, the device immediately stops operation and enters hardware shutdown mode. This may result in pops or clicks. It is recommend to first enter software shutdown before entering hardware shutdown.

When RESETZ is released, the device will enter software shutdown. A power up sequence such as with the appropriate mode selected should be executed to exit shutdown in the desired mode of operation.

9.3.19.2 Software Shutdown

Software shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to lose register state. Software shutdown is enabled by following [Device Power Up and Unmute Sequence](#).

9.3.19.3 Low Power Sleep

The device has a low power sleep ([Table 15](#)) mode option to reduce the power consumption on analog supply VBAT. In order to use this operating mode, the VBAT and AVDD supply should remain powered up when in this mode. This mode disables the Power-on Reset connected to the VBAT supply reducing current consumption.

Table 15. Low Power Sleep

| LOW_PWR[7] (VBAT_POR) | Low Power Sleep Mode |
|-----------------------|-----------------------------|
| 0 | Disabled (default) |
| 1 | Enabled - VBAT POR shutdown |

9.3.19.4 Software Reset

The TAS2557 internal logic must be initialized to a known condition for proper device function by doing a software reset. Performing software reset after a hardware reset is mandatory for reliable device boot up. A software reset can be accomplished by asserting RESET bit in [Table 16](#), which is self clearing. This will restore all registers to their default values. After software reset is performed, no register read/write should be performed within 100us while initialization sequence occurs.

Table 16. Software Reset

| RESET[0] (RESET) | Action |
|------------------|-----------------------|
| 0 | Don't reset (default) |
| 1 | Reset(Self clearing) |

9.3.19.5 Device Processing Modes

The TAS2557 DSP can be initialized into one of three modes. The advanced processing features in these modes, such as battery guard, thermal fold-back, brownout, and boost are configured using [PurePath™ Console 3 Software TAS2557 Application](#)

Table 17. Device Power Mode

| BOOT_MODE[3:0] (DSP_MODE) | Operating Mode |
|---------------------------|--|
| 0000 | Reserved |
| 0001 | Mode 1 - PCM input playback only (default) |
| 0010 | Mode 2 - PCM input playback + PCM IVsense output |
| 0011 | Mode 3 - Smart Amp Mode |

9.3.19.5.1 Mode 1 - PCM input playback only

ROM mode 1 provides the quickest initialization for the TAS2557 power up and is the lowest power mode. This mode can be used to play a known power up audio sequence before the rest of the audio system software is loaded. The mode provides fault protection, brownout protection, volume control, and Class-H controller. The EQ and Battery Guard can be enabled with minimal additional configuration. The speaker protection algorithm is not running in this mode and the I/V sense ADCs are powered down to minimize power consumption. The PLL can be disabled for even lower power consumption if the MCLK supplied is at least 12.288MHz for any fs which is multiple or sub-multiple of 48kHz, or 11.2896 MHz for Fs of 44.1kHz. This mode should be used to characterize the electrical performance on the TAS2557 without any influence from the protection algorithm present in other modes.

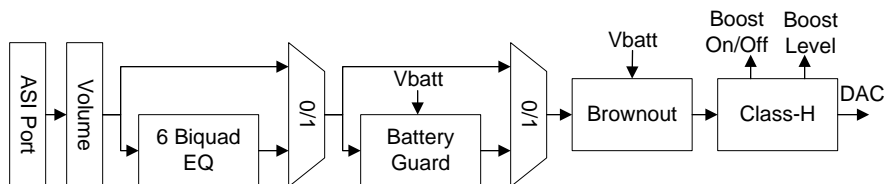


Figure 27. ROM Mode 1 Processing Block Diagram

9.3.19.5.2 Mode 2 - PCM input playback + PCM IVsense output

ROM mode 2 is similar to ROM mode 1 except the I/V sense ADCs are powered up and the data is routed back on the L/R return channels of the ASI port. This mode can be used to return the I/V data to the host and perform alternate computations on the speaker I/V measurements.

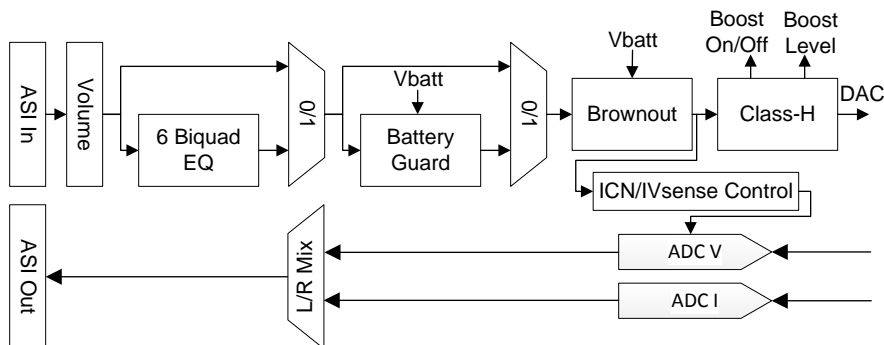


Figure 28. ROM Mode 2 Processing Block Diagram

9.3.19.5.3 Mode 3 - Smart Amp Mode

Smart Amp Mode is used to run the TI Smart Amp algorithm on the built in DSP. This mode involves loading larger output files generated from the [PurePath™ Console 3 Software TAS2557 Application](#). The generated files contain the speaker models, equalization, and additional configuration parameters in a format to load over the I²C or SPI interface. TI's Smart Amp provides thermal and excursion protection using initial speaker models and the current and voltage feedback. This allows TAS2557 to determine exact coil temperature and update the initial model due to variations in speaker and ambient conditions. More information about this mode can be found in the [PurePath™ Console 3 Software TAS2557 Application](#).

9.4 Device Functional Modes

9.4.1 Audio Digital I/O Interface

Audio data is transferred between the host processor and the TAS2557 via the digital audio serial interface (ASI), or audio bus. The ASI buses (ASI1 and ASI2) can be configured for left or right-justified, I2S, DSP, or TDM modes of operation. Standard telephony PCM interfaces are supported within the TDM mode.. These modes are all MSB-first, with data width programmable to 16, 20, 24, or 32 bits. In addition, the WCLK and BCLK can be independently configured in either master or slave mode for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

Table 18. ASI PCM Mode

| ASI1_FORMAT[4:2] (ASI1_MODE) | ASI2_FORMAT[4:2] (ASI2_MODE) | ASI Function Mode |
|------------------------------|------------------------------|---------------------------------|
| 000 | 000 | I ² S Mode (default) |
| 001 | 001 | DSP Mode |
| 010 | 010 | Right-Justified Mode (RJF) |

Table 18. ASI PCM Mode (continued)

| ASI1_FORMAT[4:2] (ASI1_MODE) | ASI2_FORMAT[4:2] (ASI2_MODE) | ASI Function Mode |
|---------------------------------|---------------------------------|---|
| 011 | 011 | Left-Justified Mode (LJF) |
| 100 | 100 | Mono PCM Mode |

Table 19. ASI PCM Input Word Length

| ASI1_FORMAT[1:0] (ASI1_LENGTH) | ASI2_FORMAT[1:0] (ASI2_LENGTH) | Word Length |
|-----------------------------------|-----------------------------------|-------------------|
| 00 | 00 | 16 bits |
| 01 | 01 | 20 bits |
| 10 | 10 | 24 bits (default) |
| 11 | 11 | 32 bits |

The bit clock (BCLK) is used to clock in and clock out the digital audio data across the serial bus. This signal can be programmed to generate variable clock pulses by controlling the BCLK multiply-divide factor in Registers 0x08 through 0x10. The number of BCLK pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TAS2557 devices may share the same audio bus.

The TAS2557 also includes a feature to offset the position of start of data transfer with respect to the wordclock (WCLK). This offset is specified in number of BCLKs. This can be used in cases where there is a non-zero bit-clock delay from WCLK edge or to support TDM modes of operation. The TAS2557 can place the DOUT line into a Hi-Z (tri-state) condition during all BCLKs when valid data is not being sent. TDM mode is useable with I²S, LJF, RJF, and DSP interface modes and is required for stereo applications when more than one TAS2557 part is used. The TAS2557 also has a bus keeper circuit that can be enabled in tri-state mode. The bus-keeper is a weak internal latch that will hold the data line state without the need for external pull-up or pull-down resistors while signal lines are in the Hi-Z or non-driven state.

Table 20. ASI OFFSET1

| ASI1_OFFSET_1 (ASI_OFFSET1) | ASI2_OFFSET_1 (ASI2_OFFSET1) | BCLKs from WCLK edge for data channel |
|--------------------------------|---------------------------------|---------------------------------------|
| 0x00 | 0x00 | 0 (default) |
| 0x01 | 0x01 | 1 |
| 0x02 | 0x02 | 2 |
| ... | ... | ... |
| 0xFF | 0xFF | 255 |

Table 21. ASI Tri-state

| ASI1_FORMAT[0] (ASI1_TRISTATE) | ASI2_FORMAT[0] (ASI2_TRISTATE) | Tri-state DOUT for extra BCLK cycles after frame is complete |
|-----------------------------------|-----------------------------------|--|
| 0 | 0 | disabled (default) |
| 1 | 1 | enabled |

Table 22. ASI Bus-keeper

| ASI1_BUSKEEP[7] (ASI1_BKP) | ASI2_BUSKEEP[7] (ASI2_BKP) | Tri-state DOUT for extra BCLK cycles after frame is complete |
|----------------------------|----------------------------|--|
| 0 | 0 | disabled (default) |
| 1 | 1 | enabled |

Additional configuration options for the ASI1 and ASI2 interface can be found in the [Register Map](#). It is recommended to use the [PurePath™ Console 3 Software TAS2557 Application](#) software for TAS2557 to configure the ASI interfaces.

9.4.1.1 I²S Mode

In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

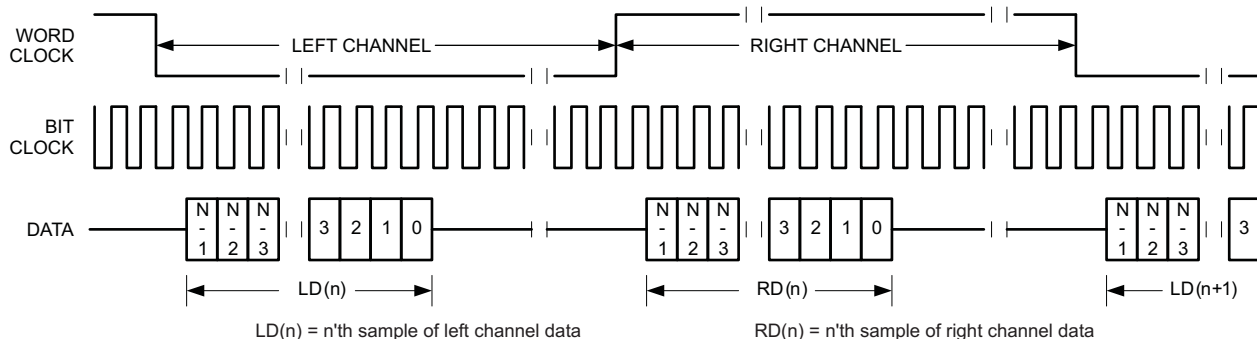


Figure 29. Timing Diagram for I²S Mode

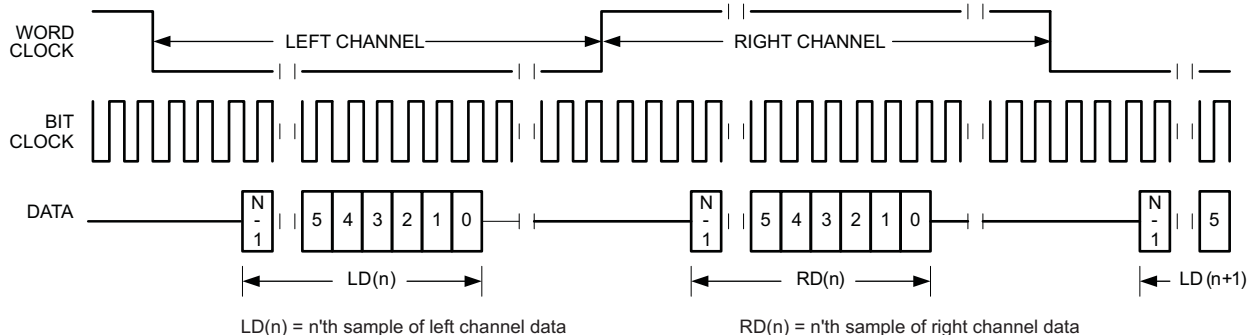


Figure 30. Timing Diagram for I²S Mode with ASI_OFFSET1 = 2

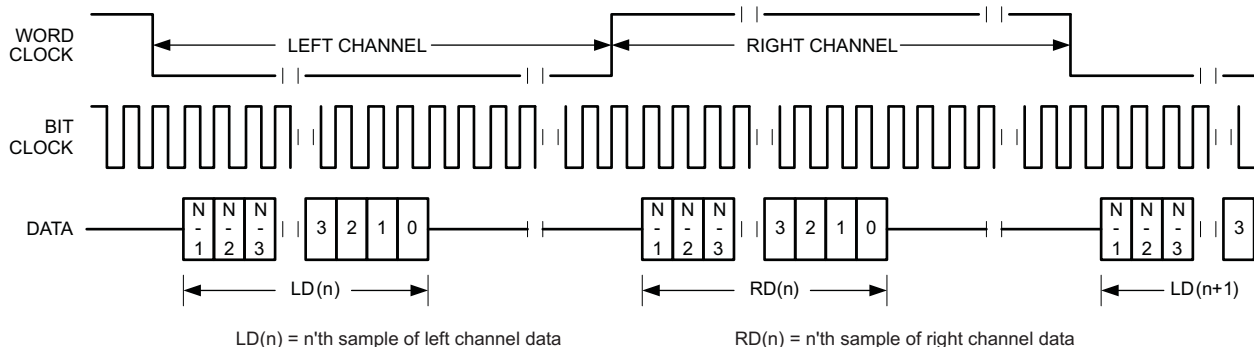


Figure 31. Timing Diagram for I²S Mode with ASI_OFFSET1 = 0 and Inverted Bit Clock

For I²S mode, the number of bit-clcks per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

9.4.1.2 DSP Mode

In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

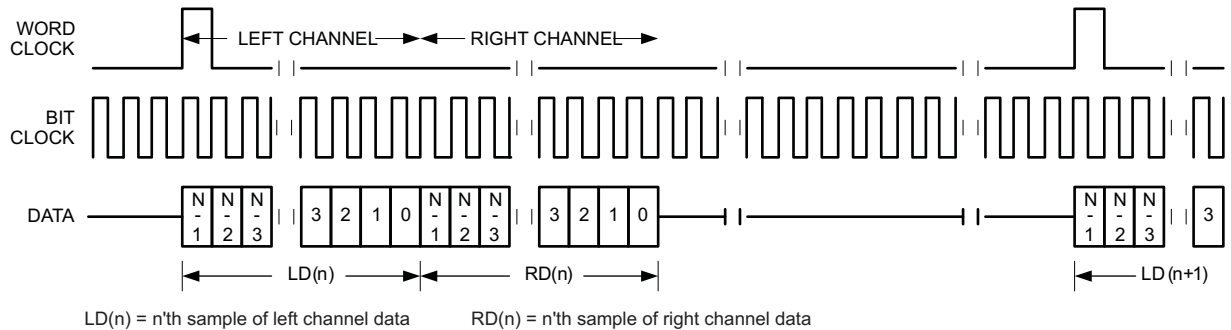


Figure 32. Timing Diagram for DSP Mode

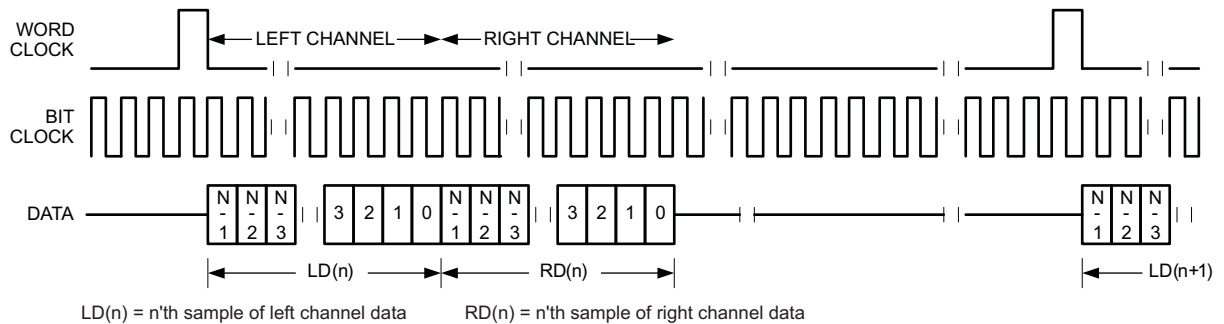


Figure 33. Timing Diagram for DSP Mode with ASI_OFFSET1=1

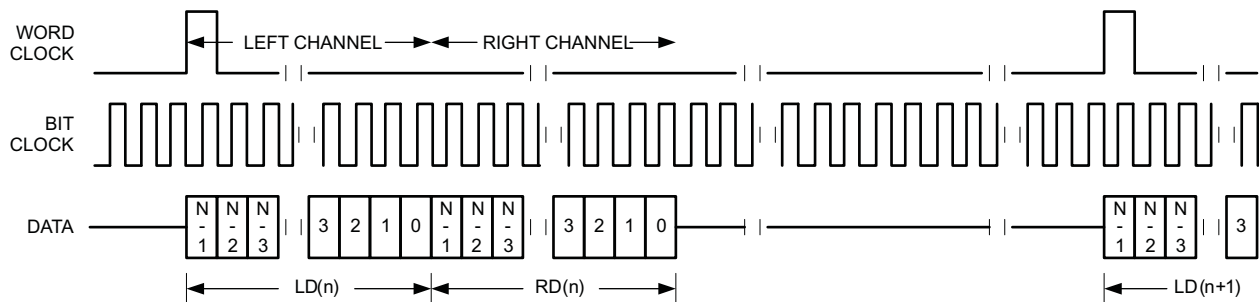


Figure 34. Timing Diagram for DSP Mode with ASI_OFFSET1=0 and Inverted Bit Clock

For DSP mode, the number of bit-clcks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

9.4.1.3 Right-Justified Mode (RJF)

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

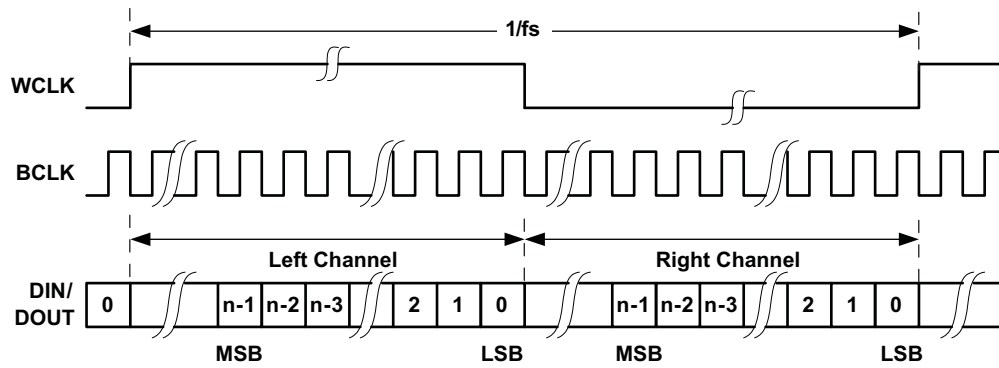


Figure 35. Timing Diagram for Right-Justified Mode

For right-justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

9.4.1.4 Left-Justified Mode (LJF)

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

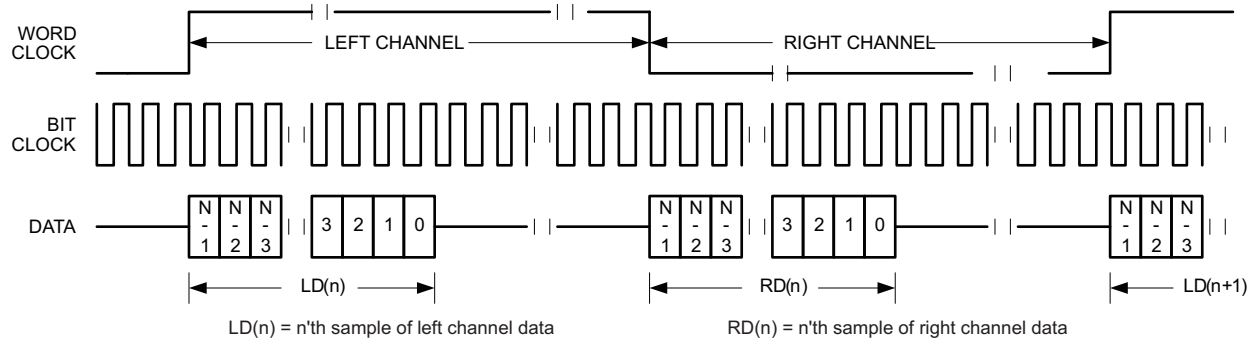


Figure 36. Timing Diagram for Left-Justified Mode

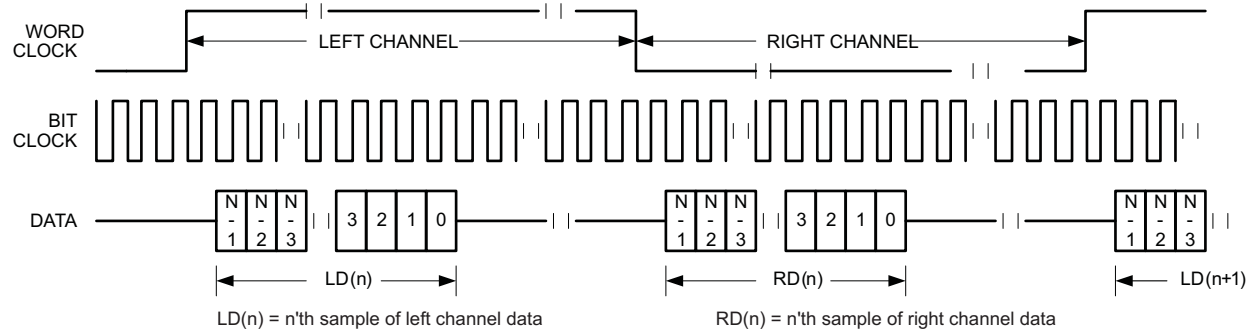


Figure 37. Timing Diagram for Light-Left Mode with ASI_OFFSET1 = 1

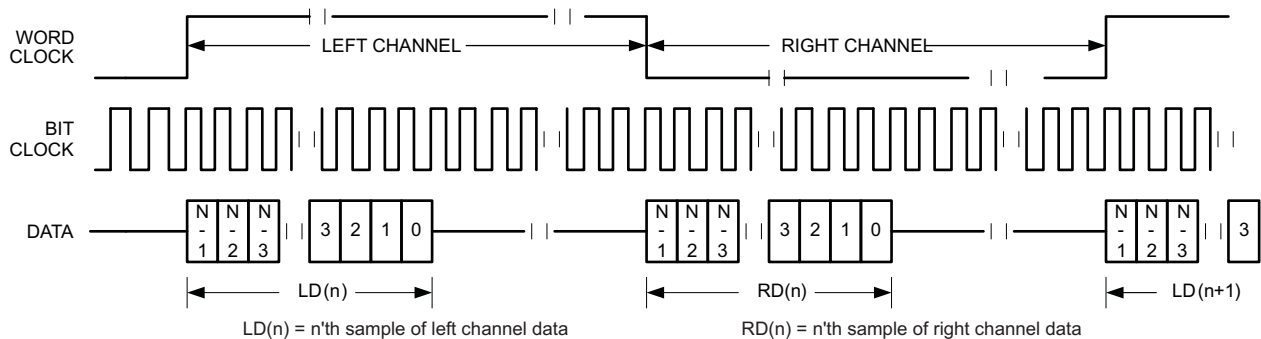


Figure 38. Timing Diagram for Left-Justified Mode with ASI_OFFSET1 = 0 and Inverted Bit Clock

For left-justified mode, the number of bit-clcks per frame should be greater than twice the programmed word-length of the data. Also, the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

9.4.2 Mono PCM Mode

In mono PCM mode, the rising edge of the word clock starts the data transfer of the single channel of data. Each data bit is valid on the falling edge of the bit clock.

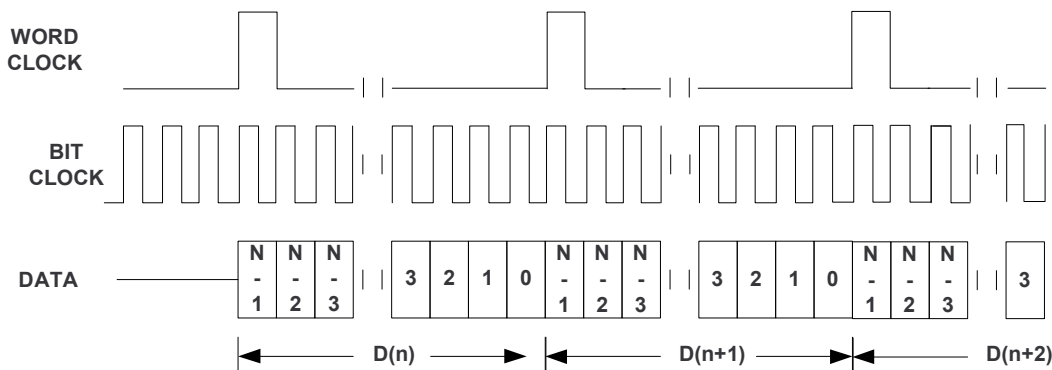


Figure 39. Timing Diagram for Mono PCM Mode

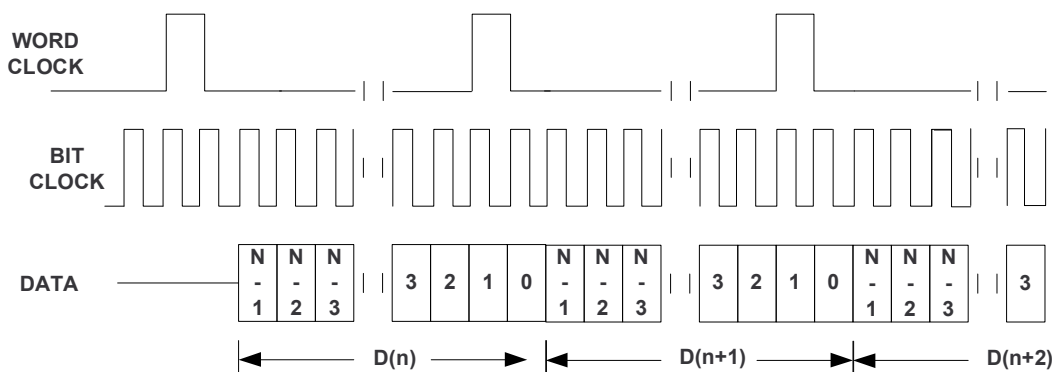


Figure 40. Timing Diagram for Mono PCM Mode with ASI_OFFSET1=2

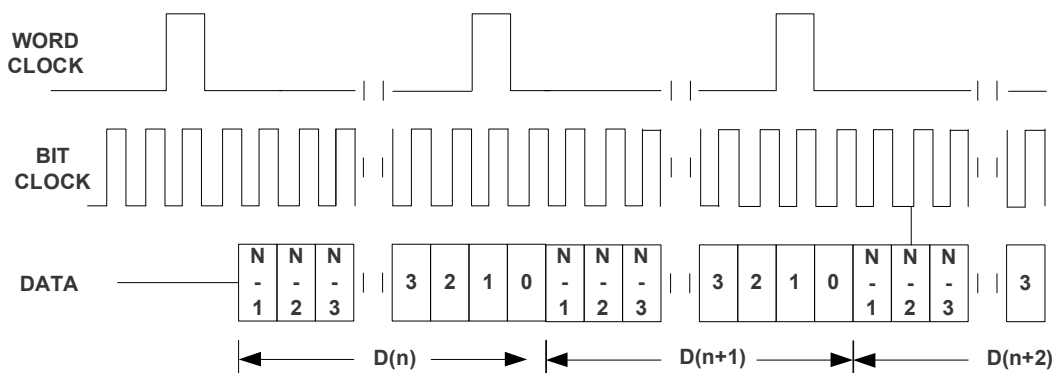


Figure 41. Timing Diagram for Mono PCM Mode with ASI_OFFSET1=2 and Bit Clock Inverted

For mono PCM mode, the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

9.4.3 Stereo Application Example - TDM Mode

Time-division multiplexing (TDM) is required for two or more devices to share a common DIN connection and a common DOUT connection. Using TDM mode, all devices transmit their DOUT data in user-specified sub-frames within one WCLK period. When one device transmits its DOUT information, the other devices place their DOUT terminals in a high impedance tri-state mode. The host processor can operate in I²S mode while the TAS2557 is running in I²S TDM mode to support sharing of the same DOUT line.

TDM mode is useable with I²S, LJF, RJF, and DSP interface modes. Refer to the respective sections for a description of how to set the TAS2557 into those modes.

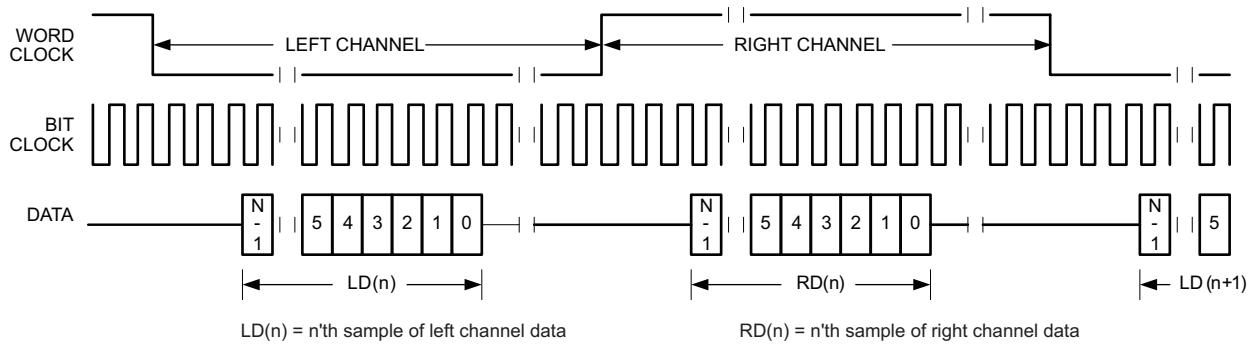


Figure 42. Timing Diagram for I²S in TDM Mode with ASI_OFFSET1=2

For TDM mode, the number of bit-clcks per frame should be less than the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

9.5 Programming

While the below scripts are provided as configuration examples, it is recommended to use [PurePath™ Console 3 Software TAS2557 Application](#) software to generate the device configuration files. This software contains configuration checks to ensure proper settings are used in the device for various cases and loaded the needed fixed-function DSP patches.

9.5.1 Code Loading and CRC check

The TI Smart Amp software is loaded into program ram (PRAM) through writes to mapped memory registers. The encrypted binary software is downloaded and decoded on chip. Therefore read-back of the PRAM is disabled. However an 8-bit CRC checksum is provided to the customer to verify the code was correctly written to PRAM error-free. Once the software download is complete, the calculated 8-bit CRC checksum can be read from register CRC_CHECKSUM. If this value matches the checksum supplied with the program, the load to PRAM was successful. If new PRAM code is loaded the TAS2557 device should first be software or hardware reset to clear the CRC checksum register so that a proper checksum from the new code to be loaded.

Programming (continued)

The following is an example script used to load the DSP software and verify the CRC checksum.

```
#####
#This script is a demo for downloading the PRAM code and checking CRC checksum
i i2cstd
#mclk expected is 24.576 MHz
#configuring device registers for 8 ohm speaker load
##### DEVICE INIT SEQ START#####
w 98 00 00 #Page-0
w 98 7f 00 #Book-0
w 98 01 01 #Software reset
d 1 # wait 100us time for OTP-One Time Programmable memory values to be transferred to device

##### INIT SECTION START
w 98 7f 64 # book 100
w 98 46 01 # IRAM boot
w 98 7f 00 # book 0
##### INIT SECTION END

##### DSP PROG SETTING START
w 98 7f 64
w 98 00 01
#add writes for download to PRAM here
w 98 00 00
w 98 7f 00
##### DSP PROG SETTING END

##### DEVICE INIT SEQ END #####

r 98 20 1 # reading the CRC checksum for the PRAM download , if read = CRC checksum provided to
customer => PRAM download success

##### CHANNEL POWER UP #####
w 98 05 A3 # Power up Analog Blocks
w 98 04 B8 # Power up DSP and clock dividers
w 98 07 00 # Unmute Analog Blocks
w 98 7f 64 # switch to book100
w 98 07 00 # Soft stepped unmute of audio playback
#####

##### DSP coeff update START
# d 1
# DSP filter coefficient update if required
##### DSP coeff update END

#####device powered up and running#####

##### CHANNEL POWER DOWN #####
w 98 07 01 # Soft stepped mute of audio playback
d 10 # wait for DSP to mute classD after soft step down of audio
# instead of delay alternatively status flag B120_P15_R120_R121_R122_R123 polling can be done and wait
till R122_D0 = '1'.
w 98 7f 00 # switch to book0
w 98 07 03 # Mute Analog Blocks
w 98 04 20 # Power down DSP and clock dividers (except Ndivider)
w 98 05 00 # Power down Analog Blocks
w 98 00 00 # NOP
w 98 04 00 # Power down Ndivider
#####
#optional(ending the script in B0_P0)
w 98 00 00 # page 0
w 98 7f 00 # book 0
#####
```

Programming (continued)

9.5.2 Device Power Up and Unmute Sequence

The following code example provide the correct sequence to power up and unmute the device. The [PurePath™ Console 3 Software TAS2557 Application](#) software will create output files with these commands. The following is a example of powering up the part in DSP Mode 2 with proper sequencing.

```

Example script (ROM Mode 2):
#####
i i2cstd
#mclk expected is 24.576 MHz
#configuring device registers for 8 ohm speaker load
##### DEVICE INIT SEQ START#####
w 98 00 00 #Page-0
w 98 7f 00 #Book-0
w 98 01 01 #Software reset
d 1      # wait 100us time for OTP-One Time Programmable memory values to be transferred to device

##### DSP PROG SETTING START
w 98 22 22 # use default coefficients and operate DSP in rom mode 2
##### DSP PROG SETTING END

##### DEVICE INIT SEQ END #####

##### CHANNEL POWER UP #####
w 98 05 A3 # Power up Analog Blocks
w 98 04 B8 # Power up DSP and clock dividers
w 98 07 00 # Unmute Analog Blocks
w 98 7f 64 # switch to book100
w 98 07 00 # Soft stepped unmute of audio playback
#####

##### DSP coeff update START
# d 1
# DSP filter coefficient update if required
##### DSP coeff update END

b #####device powered up and running#####

```

Programming (continued)

9.5.3 Device Mute and Power Down Sequence

The following code example provide the correct sequence to mute and power down the device. The [PurePath™ Console 3 Software TAS2557 Application](#) software will create output files with these commands.

```

Example script (ROM Mode 2):
#####
i i2cstd
##### CHANNEL POWER DOWN #####
w 98 07 01 # Soft stepped mute of audio playback
d 10 # wait for DSP to mute classD after soft step down of audio
# instead of delay alternatively status flag B120_P15_R120_R121_R122_R123 polling can be done and wait
till R122_D0 = '1'.
w 98 7f 00 # switch to book0
w 98 07 03 # Mute Analog Blocks
w 98 04 20 # Power down DSP and clock dividers (except Ndivider)
w 98 05 00 # Power down Analog Blocks
w 98 00 00 # NOP
w 98 04 00 # Power down Ndivider
#####
#optional(ending the script in B0_P0)
w 98 00 00 # page 0
w 98 7f 00 # book 0
#####
    
```

9.6 Register Map

See the General I²C Operation section for more details on addressing. Register settings should be set based on the files generated from the PPC3 GUI. Because the TAS2557 is a complex system including the internal software, changes made in the TAS2557 registers not known in the PPC3 generated configurations can result in the speaker protection not operating correctly. Changes should be made from within [PurePath™ Console 3 Software TAS2557 Application](#) instead of manually changing registers when possible. Configuration files with needed options can be generated from PPC3 to prevent invalid configurations.

9.6.1 Register Map Summary

9.6.1.1 Register Summary Table Book=0x00 Page=0x00

| Addr | Register | Description | Section |
|------|---------------|-------------------------------|---|
| 0x00 | PAGE | Page Select | PAGE (book=0x00 page=0x02 address=0x00) [reset=1h] |
| 0x01 | RESET | Software Reset | RESET (book=0x00 page=0x00 address=0x01) [reset=0h] |
| 0x04 | POWER_1 | Power Up 1 | POWER_1 (book=0x00 page=0x00 address=0x04) [reset=0h] |
| 0x05 | POWER_2 | Power Up 2 | POWER_2 (book=0x00 page=0x00 address=0x05) [reset=0h] |
| 0x06 | SPK_GAIN_EDGE | Class-D Speaker Configuration | SPK_GAIN_EDGE (book=0x00 page=0x00 address=0x06) [reset=0h] |
| 0x07 | MUTE | Mute Configuration | MUTE (book=0x00 page=0x00 address=0x07) [reset=0h] |
| 0x08 | SNS_CTRL | Sense Channel Control | SNS_CTRL (book=0x00 page=0x00 address=0x08) [reset=0h] |
| 0x09 | BOOST_CTRL_1 | Boost Control 1 | BOOST_CTRL_1 (book=0x00 page=0x00 address=0x09) [reset=0h] |
| 0x14 | SAR_CTRL_2 | SAR Control 2 | SAR_CTRL_2 (book=0x00 page=0x00 address=0x14) [reset=32h] |
| 0x15 | SAR_CTRL_3 | SAR Control 3 | SAR_CTRL_3 (book=0x00 page=0x00 address=0x15) [reset=4h] |
| 0x16 | SAR_VBAT_MSB | SAR VBAT Readback | SAR_VBAT_MSB (book=0x00 page=0x00 address=0x16) [reset=0h] |
| 0x17 | SAR_VBAT_LSB | SAR VBAT Readback | SAR_VBAT_LSB (book=0x00 page=0x00 address=0x17) [reset=0h] |
| 0x18 | SAR_VBST_MSB | SAR VBOOST Readback | SAR_VBST_MSB (book=0x00 page=0x00 address=0x18) [reset=0h] |
| 0x19 | SAR_VBST_LSB | SAR VBOOST Readback | SAR_VBST_LSB (book=0x00 page=0x00 address=0x19) [reset=0h] |
| 0x1A | SAR_TMP1_MSB | SAR TEMP1 Readback | SAR_TMP1_MSB (book=0x00 page=0x00 address=0x1A) [reset=0h] |

Register Map (continued)

| | | | |
|------|-----------------|-------------------------|---|
| 0x1B | SAR_TMP1_LSB | SAR TEMP1 Readback | SAR_TMP1_LSB (book=0x00 page=0x00 address=0x1B) [reset=0h] |
| 0x1C | SAR_TMP2_MSB | SAR TEMP2 Readback | SAR_TMP2_MSB (book=0x00 page=0x00 address=0x1C) [reset=0h] |
| 0x1D | SAR_TMP2_LSB | SAR TEMP2 Readback | SAR_TMP2_LSB (book=0x00 page=0x00 address=0x1D) [reset=0h] |
| 0x20 | CRC_CHECKSUM | Checksum | CRC_CHECKSUM (book=0x00 page=0x00 address=0x20) [reset=0h] |
| 0x21 | CRC_RESET | Checksum Reset | CRC_RESET (book=0x00 page=0x00 address=0x21) [reset=0h] |
| 0x22 | DSP_CTRL | DSP Control | DSP_CTRL (book=0x00 page=0x00 address=0x22) [reset=1h] |
| 0x28 | SSM_CTRL | Spread-Spectrum Control | SSM_CTRL (book=0x00 page=0x00 address=0x28) [reset=0h] |
| 0x2A | ASI_CTRL_1 | ASI Control 1 | ASI_CTRL_1 (book=0x00 page=0x00 address=0x2A) [reset=0h] |
| 0x2B | BOOST_CTRL_2 | Boost Control 1 | BOOST_CTRL_2 (book=0x00 page=0x00 address=0x2B) [reset=3h] |
| 0x2C | CLOCK_CTRL_1 | Clock Control 1 | CLOCK_CTRL_1 (book=0x00 page=0x00 address=0x2C) [reset=0h] |
| 0x2D | CLOCK_CTRL_2 | Clock Control 2 | CLOCK_CTRL_2 (book=0x00 page=0x00 address=0x2D) [reset=17h] |
| 0x2E | CLOCK_CTRL_3 | Clock Control 3 | CLOCK_CTRL_3 (book=0x00 page=0x00 address=0x2E) [reset=0h] |
| 0x2F | ASI_CTRL_2 | ASI Control 2 | ASI_CTRL_2 (book=0x00 page=0x00 address=0x2F) [reset=0h] |
| 0x32 | CLOCK_CTRL_4 | Clock Control 4 | CLOCK_CTRL_4 (book=0x00 page=0x00 address=0x32) [reset=0h] |
| 0x35 | DEBUG_1 | Debug Register 1 | DEBUG_1 (book=0x00 page=0x00 address=0x35) [reset=0h] |
| 0x64 | POWER_STATUS | Power Up Status | POWER_STATUS (book=0x00 page=0x00 address=0x64) [reset=0h] |
| 0x65 | DSP_BOOT_STATUS | DSP Boost Status | DSP_BOOT_STATUS (book=0x00 page=0x00 address=0x65) [reset=0h] |
| 0x68 | INT_DET_1 | Interrupt Detected 1 | INT_DET_1 (book=0x00 page=0x00 address=0x68) [reset=0h] |
| 0x6C | INT_DET_2 | Interrupt Detected 2 | INT_DET_2 (book=0x00 page=0x00 address=0x6C) [reset=0h] |
| 0x79 | LOW_POWER | Lower Power Shutdown | LOW_POWER (book=0x00 page=0x00 address=0x79) [reset=0h] |
| 0x7F | BOOK | Book Selection | BOOK (book=0x00 page=0x00 address=0x7F) [reset=0h] |

9.6.1.2 Register Summary Table Book=0x00 Page=0x01

| Addr | Register | Description | Section |
|------|-----------------|-------------------------|--|
| 0x00 | PAGE | Page Select | PAGE (book=0x00 page=0x02 address=0x00) [reset=1h] |
| 0x01 | ASI1_FORMAT | ASI1 Format | ASI1_FORMAT (book=0x00 page=0x01 address=0x01) [reset=10h] |
| 0x03 | ASI1_OFFSET_1 | ASI1 Offset | ASI1_OFFSET_1 (book=0x00 page=0x01 address=0x03) [reset=0h] |
| 0x04 | ASI1_OFFSET_2 | ASI1 Offset Second Slot | |
| 0x05 | ASI1_BUSKEEP | ASI1 Buskeeper | ASI1_BUSKEEP (book=0x00 page=0x01 address=0x05) [reset=0h] |
| 0x08 | ASI1_BCLK | ASI1 BCLK | ASI1_BCLK (book=0x00 page=0x01 address=0x08) [reset=0h] |
| 0x09 | ASI1_WCLK | ASI1 WCLK | ASI1_WCLK (book=0x00 page=0x01 address=0x09) [reset=8h] |
| 0x0C | ASI1_DIN_DOUT | ASI1 DIN/DOUT | ASI1_DIN_DOUT (book=0x00 page=0x01 address=0x0C) [reset=0h] |
| 0x0D | ASI1_BDIV_CLK | ASI1 BDIV Clock | ASI1_BDIV_CLK (book=0x00 page=0x01 address=0x0D) [reset=1h] |
| 0x0E | ASI1_BDIV_RATIO | ASI1 BDIV Ratio | ASI1_BDIV_RATIO (book=0x00 page=0x01 address=0x0E) [reset=2h] |
| 0x0F | ASI1_WDIV_RATIO | ASI1 WDIV Ratio | ASI1_WDIV_RATIO (book=0x00 page=0x01 address=0x0F) [reset=20h] |

| | | | |
|------|-----------------|-------------------------|--|
| 0x10 | ASI1_CLK_OUT | ASI1 Clock Source | ASI1_CLK_OUT (book=0x00 page=0x01 address=0x10) [reset=0h] |
| 0x15 | ASI2_FORMAT | ASI2 Format | ASI2_FORMAT (book=0x00 page=0x01 address=0x15) [reset=10h] |
| 0x17 | ASI2_OFFSET_1 | ASI2 Offset | ASI2_OFFSET_1 (book=0x00 page=0x01 address=0x17) [reset=0h] |
| 0x18 | ASI2_OFFSET_2 | ASI2 Offset Second Slot | |
| 0x19 | ASI2_BUSKEEP | ASI2 Buskeeper | ASI2_BUSKEEP (book=0x00 page=0x01 address=0x19) [reset=0h] |
| 0x1C | ASI2_BCLK | ASI2 BCLK | ASI2_BCLK (book=0x00 page=0x01 address=0x1C) [reset=20h] |
| 0x1D | ASI2_WCLK | ASI2 WCLK | ASI2_WCLK (book=0x00 page=0x01 address=0x1D) [reset=28h] |
| 0x20 | ASI2_DIN_DOUT | ASI2 DIN/DOUT | ASI2_DIN_DOUT (book=0x00 page=0x01 address=0x20) [reset=38h] |
| 0x21 | ASI2_BDIV_CLK | ASI2 BDIV Clock | ASI2_BDIV_CLK (book=0x00 page=0x01 address=0x21) [reset=1h] |
| 0x22 | ASI2_BDIV_RATIO | ASI2 BDIV Ratio | ASI2_BDIV_RATIO (book=0x00 page=0x01 address=0x22) [reset=2h] |
| 0x23 | ASI2_WDIV_RATIO | ASI2 WDIV Ratio | ASI2_WDIV_RATIO (book=0x00 page=0x01 address=0x23) [reset=20h] |
| 0x24 | ASI2_CLK_OUT | ASI2 Clock Source | ASI2_CLK_OUT (book=0x00 page=0x01 address=0x24) [reset=33h] |
| 0x3D | GPIO1_PIN | GPIO1 | GPIO1_PIN (book=0x00 page=0x01 address=0x3D) [reset=1h] |
| 0x3E | GPIO2_PIN | GPIO2 | GPIO2_PIN (book=0x00 page=0x01 address=0x3E) [reset=1h] |
| 0x3F | GPIO3_PIN | GPIO3 | GPIO3_PIN (book=0x00 page=0x01 address=0x3F) [reset=10h] |
| 0x40 | GPIO4_PIN | GPIO4 | GPIO4_PIN (book=0x00 page=0x01 address=0x40) [reset=7h] |
| 0x41 | GPIO5_PIN | GPIO5 | GPIO5_PIN (book=0x00 page=0x01 address=0x41) [reset=0h] |
| 0x42 | GPIO6_PIN | GPIO6 | GPIO6_PIN (book=0x00 page=0x01 address=0x42) [reset=0h] |
| 0x43 | GPIO7_PIN | GPIO7 | GPIO7_PIN (book=0x00 page=0x01 address=0x43) [reset=0h] |
| 0x44 | GPIO8_PIN | GPIO8 | GPIO8_PIN (book=0x00 page=0x01 address=0x44) [reset=0h] |
| 0x45 | GPIO9_PIN | GPIO9 | GPIO9_PIN (book=0x00 page=0x01 address=0x45) [reset=0h] |
| 0x46 | GPIO10_PIN | GPIO10 | GPIO10_PIN (book=0x00 page=0x01 address=0x46) [reset=0h] |
| 0x4D | GPI_PIN | GPI Pin Mode | GPI_PIN (book=0x00 page=0x01 address=0x4D) [reset=0h] |
| 0x4F | GPIO_HIZ_1 | GPIO HiZ 1 | GPIO_HIZ_1 (book=0x00 page=0x01 address=0x4F) [reset=0h] |
| 0x50 | GPIO_HIZ_2 | GPIO HiZ 2 | GPIO_HIZ_2 (book=0x00 page=0x01 address=0x50) [reset=0h] |
| 0x51 | GPIO_HIZ_3 | GPIO HiZ 3 | GPIO_HIZ_3 (book=0x00 page=0x01 address=0x51) [reset=0h] |
| 0x52 | GPIO_HIZ_4 | GPIO HiZ 4 | GPIO_HIZ_4 (book=0x00 page=0x01 address=0x52) [reset=0h] |
| 0x53 | GPIO_HIZ_5 | GPIO HiZ 5 | GPIO_HIZ_5 (book=0x00 page=0x01 address=0x53) [reset=0h] |
| 0x58 | BIT_BANG_OUT1 | Bit Bang Output 1 | BIT_BANG_OUT1 (book=0x00 page=0x01 address=0x58) [reset=0h] |
| 0x59 | BIT_BANG_OUT2 | Bit Bang Output 2 | BIT_BANG_OUT2 (book=0x00 page=0x01 address=0x59) [reset=0h] |
| 0x5A | BIT_BANG_IN1 | Bit Bang Input 1 | BIT_BANG_IN1 (book=0x00 page=0x01 address=0x5A) [reset=0h] |
| 0x5B | BIT_BANG_IN2 | Bit Bang Input 2 | BIT_BANG_IN2 (book=0x00 page=0x01 address=0x5B) [reset=0h] |
| 0x5C | BIT_BANG_IN3 | Bit Bang Input 3 | BIT_BANG_IN3 (book=0x00 page=0x01 address=0x5C) [reset=0h] |
| 0x60 | ASIM_BUSKEEP | ASIM Buskeeper | ASIM_BUSKEEP (book=0x00 page=0x01 address=0x60) [reset=0h] |
| 0x61 | ASIM_MODE | ASIM Mode | ASIM_MODE (book=0x00 page=0x01 address=0x61) [reset=8h] |
| 0x62 | ASIM_NUM_DEV | ASIM Number Devices | ASIM_NUM_DEV (book=0x00 page=0x01 address=0x62) [reset=0h] |

| | | | |
|------|-------------------|---------------------------|--|
| 0x63 | ASIM_FORMAT | ASIM Format | ASIM_FORMAT (book=0x00 page=0x01 address=0x63) [reset=10h] |
| 0x64 | ASIM_BDIV_CLK | ASIM BDIV Clock | ASIM_BDIV_CLK (book=0x00 page=0x01 address=0x64) [reset=1h] |
| 0x65 | ASIM_BDIV_RATIO | ASIM BDIV Ratio | ASIM_BDIV_RATIO (book=0x00 page=0x01 address=0x65) [reset=2h] |
| 0x66 | ASIM_WDIV_RATIO_1 | ASIM WDIV Ratio | ASIM_WDIV_RATIO_1 (book=0x00 page=0x01 address=0x66) [reset=0h] |
| 0x67 | ASIM_WDIV_RATIO_2 | ASIM WDIV Ratio | ASIM_WDIV_RATIO_2 (book=0x00 page=0x01 address=0x67) [reset=20h] |
| 0x68 | ASIM_BCLK | ASI1 BCLK | ASIM_BCLK (book=0x00 page=0x01 address=0x68) [reset=40h] |
| 0x69 | ASIM_WCLK | ASI1 WCLK | ASIM_WCLK (book=0x00 page=0x01 address=0x69) [reset=38h] |
| 0x6A | ASIM_DIN | ASI1 DIN | ASIM_DIN (book=0x00 page=0x01 address=0x6A) [reset=70h] |
| 0x6C | INT_GEN_1 | Interrupt Generation 1 | INT_GEN_1 (book=0x00 page=0x01 address=0x6C) [reset=0h] |
| 0x6D | INT_GEN_2 | Interrupt Generation 2 | INT_GEN_2 (book=0x00 page=0x01 address=0x6D) [reset=0h] |
| 0x6E | INT_GEN_3 | Interrupt Generation 3 | INT_GEN_3 (book=0x00 page=0x01 address=0x6E) [reset=0h] |
| 0x6F | INT_GEN_4 | Interrupt Generation 4 | INT_GEN_4 (book=0x00 page=0x01 address=0x6F) [reset=0h] |
| 0x70 | INT_GEN_5 | Interrupt Generation 5 | INT_GEN_5 (book=0x00 page=0x01 address=0x70) [reset=0h] |
| 0x71 | INT_GEN_6 | Interrupt Generation 6 | INT_GEN_6 (book=0x00 page=0x01 address=0x71) [reset=0h] |
| 0x72 | INT_IND_MODE | Interrupt Indication Mode | INT_IND_MODE (book=0x00 page=0x01 address=0x72) [reset=0h] |
| 0x73 | MAIN_CLK_PIN | Main Clock Source | MAIN_CLK_PIN (book=0x00 page=0x01 address=0x73) [reset=Dh] |
| 0x74 | PLL_CLK_PIN | PLL Clock Source | PLL_CLK_PIN (book=0x00 page=0x01 address=0x74) [reset=Dh] |
| 0x75 | CLKOUT_MUX | CDIV_CLKIN Clock Source | CLKOUT_MUX (book=0x00 page=0x01 address=0x75) [reset=Dh] |
| 0x76 | CLKOUT_CDIV_RATIO | CLKOUT CDIV Ratio | CLKOUT_CDIV_RATIO (book=0x00 page=0x01 address=0x76) [reset=1h] |
| 0x7C | I2C_MISC | I2C Misc | I2C_MISC (book=0x00 page=0x01 address=0x7C) [reset=0h] |
| 0x7D | DEVICE_ID | Device ID | DEVICE_ID (book=0x00 page=0x01 address=0x7D) [reset=12h] |

9.6.1.3 Register Summary Table Book=0x00 Page=0x02

| Addr | Register | Description | Section |
|------|----------------|--|--|
| 0x00 | PAGE | Page Select | PAGE (book=0x00 page=0x02 address=0x00) [reset=1h] |
| 0x06 | RAMP_CTRL | Class-D Ramp Control | RAMP_CTRL (book=0x00 page=0x02 address=0x06) [reset=0h] |
| 0x09 | PROTECTION_CFG | Configures the Devices Protection Blocks | PROTECTION_CFG (book=0x00 page=0x02 address=0x09) [reset=3h] |

9.6.2 Register Maps

9.6.2.1 PAGE (book=0x00 page=0x00 address=0x00) [reset=0h]

Selects the page for the next read or write.

Figure 43. PAGE Register Address: 0x00

| | | | | | | | |
|-----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAGE[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Page Select Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-0 | PAGE[7:0] | RW | 0h | Selects the Register Page for the next read or write command |

9.6.2.2 RESET (book=0x00 page=0x00 address=0x01) [reset=0h]

Controls the software reset

Figure 44. RESET Register Address: 0x01

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|-------|
| Reserved | | | | | | | RESET |
| R-0h | | | | | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Software Reset Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-1 | Reserved | R | 0h | Reserved |
| 0 | RESET | RW | 0h | 0 = Don't care 1 = Self clearing software reset |

9.6.2.3 POWER_1 (book=0x00 page=0x00 address=0x04) [reset=0h]

This register controls device power up

Figure 45. POWER_1 Register Address: 0x04

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|----------|----------|----------|----------|----------|---------|
| PWR_DSP | PWR_PLL | PWR_NDIV | PWR_MDAC | PWR_MADC | Reserved | Reserved | PWR_ERR |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Power Up 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | PWR_DSP | RW | 0h | DSP is 0 = Powered-down 1 = Powered-up |
| 6 | PWR_PLL | RW | 0h | PLL is 0 = Powered-down 1 = Powered-up |
| 5 | PWR_NDIV | RW | 0h | NDIV is 0 = Powered-down 1 = Powered-up |
| 4 | PWR_MDAC | RW | 0h | MDAC is 0 = Powered-down 1 = Powered-up |
| 3 | PWR_MADC | RW | 0h | MADC is 0 = Powered-down 1 = Powered-up |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | Reserved | RW | 0h | Reserved |
| 0 | PWR_ERR | RW | 0h | Reports when a VBAT brownout or clock halt condition was detected. When this is detected several internal blocks are powered down. This register must be cleared first before re-power device. Reason for error is indicated in interrupt register. 0 = No error condition 1 = Error condition detected |

9.6.2.4 POWER_2 (book=0x00 page=0x00 address=0x05) [reset=0h]

This register controls device power up

Figure 46. POWER_2 Register Address: 0x05

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|-----------|----------|---|---|----------|----------|
| PWR_SPK | Reserved | PWR_BOOST | Reserved | | | PWR_ISNS | PWR_VSNS |
| RW-0h | RW-0h | RW-0h | RW-0h | | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Power Up 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | PWR_SPK | RW | 0h | Class-D output is 0 = Powered-down 1 = Powered-up |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | PWR_BOOST | RW | 0h | Boost is 0 = Powered-down 1 = Powered-up |
| 4-2 | Reserved | RW | 0h | Reserved |
| 1 | PWR_ISNS | RW | 0h | Current-sense ADC is 0 = Powered-down 1 = Powered-up |
| 0 | PWR_VSNS | RW | 0h | Voltage-sense ADC is 0 = Powered-down 1 = Powered-up |

9.6.2.5 SPK_GAIN_EDGE (book=0x00 page=0x00 address=0x06) [reset=0h]

This register controls the DAC gain and edge rate control.

Figure 47. SPK_GAIN_EDGE Register Address: 0x06

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------------|---|---|---|----------------|---|---|
| Reserved | DAC_GAIN[3:0] | | | | EDGE_RATE[2:0] | | |
| RW-0h | RW-0h | | | | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Class-D Speaker Configuration Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | DAC_GAIN[3:0] | RW | 0h | DAC gain is 0 = 0db 1 = 1db 2 = 2db ... 14 = 14db 15 = 15db |
| 2-0 | EDGE_RATE[2:0] | RW | 0h | Class-D output edge rate control is 0 = 50ns 1 = 40ns 2 = 29ns 3 = 25ns 4 = 14ns 5 = 13ns 6 = 12ns 7 = 11ns |

9.6.2.6 MUTE (book=0x00 page=0x00 address=0x07) [reset=0h]

This register controls muting of various system blocks.

Figure 48. MUTE Register Address: 0x07

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|---|----------|-----------|-----------|
| Reserved | Reserved | Reserved | Reserved | | Reserved | MUTE_ISNS | MUTE_VSNS |
| RW-0h | RW-0h | RW-0h | RW-0h | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Mute Configuration Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 0h | Reserved |
| 4-3 | Reserved | RW | 0h | Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | MUTE_ISNS | RW | 0h | Current-sense is 0 = Unmuted 1 = Muted |
| 0 | MUTE_VSNS | RW | 0h | Voltage-sense is 0 = Unmuted 1 = Muted |

9.6.2.7 SNS_CTRL (book=0x00 page=0x00 address=0x08) [reset=0h]

This register controls the full scale values of current and voltage sense channels.

Figure 49. SNS_CTRL Register Address: 0x08

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------|---|----------|-----------------|---|----------|
| Reserved | | Reserved | | Reserved | ISNS_SCALE[1:0] | | Reserved |
| RW-0h | | RW-0h | | RW-0h | RW-0h | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Sense Channel Control Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5-4 | Reserved | RW | 0h | Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-1 | ISNS_SCALE[1:0] | RW | 0h | Sets the current and voltage sense input range for various speaker loads. Select the value closest to the nominal load. 0 = 8 ohm load, i-sense full-scale: 1.25A 1 = 6 ohm load, i-sense full-scale: 1.5A 2 = 4 ohm load, i-sense full-scale: 1.75A |
| 0 | Reserved | RW | 0h | Reserved |

9.6.2.8 BOOST_CTRL_1 (book=0x00 page=0x00 address=0x09) [reset=0h]

This register controls the boost operation.

Figure 50. BOOST_CTRL_1 Register Address: 0x09

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------|---|----------|---|----------|----------|
| Reserved | | Reserved | | Reserved | | Reserved | BST_MODE |
| RW-0h | | RW-0h | | RW-0h | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Boost Control 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5-4 | Reserved | RW | 0h | Reserved |
| 3-2 | Reserved | RW | 0h | Reserved |
| 1 | Reserved | RW | 0h | Reserved |
| 0 | BST_MODE | RW | 0h | Controls the boost operation mode. 0 = Class-H operation using multi-levels. 1 = Class-G operation using one level turned on and off as needed. |

9.6.2.9 SAR_CTRL_2 (book=0x00 page=0x00 address=0x14) [reset=32h]

This register controls the SAR ADC repeat interval, readback register halt, mode, and power state.

Figure 51. SAR_CTRL_2 Register Address: 0x14

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------------|---|---|---------|---------------|---|---------|
| Reserved | SAR_RPT[2:0] | | | SAR_RBH | SAR_MODE[1:0] | | SAR_PWR |
| RW-0h | RW-3h | | | RW-0h | RW-1h | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. SAR Control 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | SAR_RPT[2:0] | RW | 3h | The SAR ADC repeat interval is 0 = 0 us 1 = 50 us 2 = 250 us 3 = 1 ms 4 = 5 ms 5 = 25 ms 6 = 100 ms 7 = 1 s |
| 3 | SAR_RBH | RW | 0h | Updates to SAR readback registers halt. The readback registers should be halted while read to avoid data corruptions issues from new SAR conversions. 0 = SAR updates readback registers 1 = SAR updates halted |
| 2-1 | SAR_MODE[1:0] | RW | 1h | Configures the SAR ADC mode of operation 0 = One-shot mode 1 = Repeated scan mode 2 = DSP triggered mode 3 = Reserved |
| 0 | SAR_PWR | RW | 0h | SAR ADC is 0 = Powered-down 1 = Powered-up |

9.6.2.10 SAR_CTRL_3 (book=0x00 page=0x00 address=0x15) [reset=4h]

This register controls the SAR ADC inputs.

Figure 52. SAR_CTRL_3 Register Address: 0x15

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|----------|-----------|-----------|-----------|
| Reserved | | | | Reserved | SAR_INVBT | SAR_INVBO | SAR_INTMP |
| RW-0h | | | | RW-0h | RW-1h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. SAR Control 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7-4 | Reserved | RW | 0h | Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2 | SAR_INVBT | RW | 1h | SAR VBAT measurement is 0 = disabled 1 = enabled |
| 1 | SAR_INVBO | RW | 0h | SAR VBOOST measurement is 0 = disabled 1 = enabled |
| 0 | SAR_INTMP | RW | 0h | SAR temperature measurement is 0 = disabled 1 = enabled |

9.6.2.11 SAR_VBAT_MSB (book=0x00 page=0x00 address=0x16) [reset=0h]

This register contains the VBAT measurement.

Figure 53. SAR_VBAT_MSB Register Address: 0x16

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|---|---|---|---|
| SR_VBAT[9:2] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. SAR VBAT Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|------------------------------------|
| 7--2 | SR_VBAT[9:0] | R | 0h | VBAT Measured data by SAR ADC[9:2] |

9.6.2.12 SAR_VBAT_LSB (book=0x00 page=0x00 address=0x17) [reset=0h]

This register contains the VBAT measurement.

Figure 54. SAR_VBAT_LSB Register Address: 0x17

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|----------|---|---|---|---|---|
| SR_VBAT[1:0] | | Reserved | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. SAR VBAT Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|------------------------------------|
| 7-6 | SR_VBAT[1:0] | R | 0h | VBAT Measured data by SAR ADC[1:0] |
| 5-0 | Reserved | R | 0h | Reserved |

9.6.2.13 SAR_VBST_MSB (book=0x00 page=0x00 address=0x18) [reset=0h]

This register contains the VBOOST measurement.

Figure 55. SAR_VBST_MSB Register Address: 0x18

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|---|---|---|---|
| SR_VBST[9:2] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. SAR VBOOST Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--------------------------------------|
| 7--2 | SR_VBST[9:0] | R | 0h | VBOOST Measured data by SAR ADC[9:2] |

9.6.2.14 SAR_VBST_LSB (book=0x00 page=0x00 address=0x19) [reset=0h]

This register contains the VBOOST measurement.

Figure 56. SAR_VBST_LSB Register Address: 0x19

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|----------|---|---|---|---|---|
| SR_VBST[1:0] | | Reserved | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. SAR VBOOST Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--------------------------------------|
| 7-6 | SR_VBST[1:0] | R | 0h | VBOOST Measured data by SAR ADC[1:0] |
| 5-0 | Reserved | R | 0h | Reserved |

9.6.2.15 SAR_TMP1_MSB (book=0x00 page=0x00 address=0x1A) [reset=0h]

This register contains the TEMP1 measurement.

Figure 57. SAR_TMP1_MSB Register Address: 0x1A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|---|---|---|---|
| SR_TMP1[9:2] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. SAR TEMP1 Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|-------------------------------------|
| 7--2 | SR_TMP1[9:0] | R | 0h | TEMP1 Measured data by SAR ADC[9:2] |

9.6.2.16 SAR_TMP1_LSB (book=0x00 page=0x00 address=0x1B) [reset=0h]

This register contains the TEMP1 measurement.

Figure 58. SAR_TMP1_LSB Register Address: 0x1B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|----------|---|---|---|---|---|
| SR_TMP1[1:0] | | Reserved | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. SAR TEMP1 Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-------------------------------------|
| 7-6 | SR_TMP1[1:0] | R | 0h | TEMP1 Measured data by SAR ADC[1:0] |
| 5-0 | Reserved | R | 0h | Reserved |

9.6.2.17 SAR_TMP2_MSB (book=0x00 page=0x00 address=0x1C) [reset=0h]

This register contains the TEMP2 measurement.

Figure 59. SAR_TMP2_MSB Register Address: 0x1C

| | | | | | | | |
|--------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SR_TMP2[9:2] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. SAR TEMP2 Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|-------------------------------------|
| 7--2 | SR_TMP2[9:0] | R | 0h | TEMP2 Measured data by SAR ADC[9:2] |

9.6.2.18 SAR_TMP2_LSB (book=0x00 page=0x00 address=0x1D) [reset=0h]

This register contains the TEMP2 measurement.

Figure 60. SAR_TMP2_LSB Register Address: 0x1D

| | | | | | | | |
|--------------|---|----------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SR_TMP2[1:0] | | Reserved | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. SAR TEMP2 Readback Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-------------------------------------|
| 7-6 | SR_TMP2[1:0] | R | 0h | TEMP2 Measured data by SAR ADC[1:0] |
| 5-0 | Reserved | R | 0h | Reserved |

9.6.2.19 CRC_CHECKSUM (book=0x00 page=0x00 address=0x20) [reset=0h]

Hold the running CRC8 checksum of I2C transactions

Figure 61. CRC_CHECKSUM Register Address: 0x20

| | | | | | | | |
|--------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC_VAL[7:0] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. Checksum Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-0 | CRC_VAL[7:0] | R | 0h | Current CRC value of all I2C transactions |

9.6.2.20 CRC_RESET (book=0x00 page=0x00 address=0x21) [reset=0h]

This register is used to reset the CRC checksum.

Figure 62. CRC_RESET Register Address: 0x21

| | | | | | | | |
|----------|---|---|---|---|---|---|---------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | CRC_RST |
| RW-0h | | | | | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Checksum Reset Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-1 | Reserved | RW | 0h | Reserved |
| 0 | CRC_RST | RW | 0h | This self clearing bit is used to reset the CRC checksum. This is recommended to be done before PRAM code download. After download the checksum value can be read to confirm download process had any errors or was successful. 0 = normal CRC operation 1 = reset CRC and clear |

9.6.2.21 DSP_CTRL (book=0x00 page=0x00 address=0x22) [reset=1h]

This controls the booting mode of the DSP

Figure 63. DSP_CTRL Register Address: 0x22

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------|----------|---------------|---|---|---|
| Reserved | | Reserved | Reserved | DSP_MODE[3:0] | | | |
| RW-0h | | RW-0h | RW-0h | RW-1h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. DSP Control Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 0h | Reserved |
| 4 | Reserved | RW | 0h | Reserved |
| 3-0 | DSP_MODE[3:0] | RW | 1h | DSP boot in mode 0 = Reserved 1 = PCM input playback only 2 = PCM input playback and IV-sense output 3 = Smart Amp 4 = Smart Amp w/ voice on ASI2 5-15 = Reserved |

9.6.2.22 SSM_CTRL (book=0x00 page=0x00 address=0x28) [reset=0h]

This enables spread-spectrum mode.

Figure 64. SSM_CTRL Register Address: 0x28

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|--------|
| Reserved | | | | | | | SSM_EN |
| RW-0h | | | | | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. Spread-Spectrum Control Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-1 | Reserved | RW | 0h | Reserved |
| 0 | SSM_EN | RW | 0h | Enables spread-spectrum mode of the modulator. Ramp clock must be using internal clock not sync mode. This is set in B100_P0_R40 0 = disabled 1 = enabled |

9.6.2.23 ASI_CTRL_1 (book=0x00 page=0x00 address=0x2A) [reset=0h]

This register configures the ASI stereo input modes and soft stepping for mute.

Figure 65. ASI_CTRL_1 Register Address: 0x2A

| | | | | | | | |
|----------|---|---|--------------|---|--------------|---|---------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | ASI2_CH[1:0] | | ASI1_CH[1:0] | | MUTE_SS |
| RW-0h | | | RW-0h | | RW-0h | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. ASI Control 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-5 | Reserved | RW | 0h | Reserved |
| 4-3 | ASI2_CH[1:0] | RW | 0h | Configures the ASI2 input to use 0 = left channel 1 = right channel 2 = (left + right) / 2 3 = monoPCM |
| 2-1 | ASI1_CH[1:0] | RW | 0h | Configures the ASI1 input to use 0 = left channel 1 = right channel 2 = (left + right) / 2 3 = monoPCM |
| 0 | MUTE_SS | RW | 0h | When muting and un-muting the channel the audio playback is soft stepped. 0 = enable 1 = disable |

9.6.2.24 BOOST_CTRL_2 (book=0x00 page=0x00 address=0x2B) [reset=3h]

This register controls the boost operation.

Figure 66. BOOST_CTRL_2 Register Address: 0x2B

| | | | | | | | |
|----------|---|---|---|----------|----------|---------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | Reserved | Reserved | BST_ILIM[1:0] | |
| RW-0h | | | | RW-0h | RW-0h | RW-3h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. Boost Control 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-4 | Reserved | RW | 0h | Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1-0 | BST_ILIM[1:0] | RW | 3h | Boost current limit 0 = 1.5A 1 = 2.0A 2 = 2.5A 3 = 3.0A |

9.6.2.25 CLOCK_CTRL_1 (book=0x00 page=0x00 address=0x2C) [reset=0h]

Configures the clock error detection handling

Figure 67. CLOCK_CTRL_1 Register Address: 0x2C

| | | | | | | | |
|----------|----------|--------|--------|-------------|---|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DSP_RSTM | Reserved | CE1_SM | CE1_IC | CE2_IC[1:0] | | CE1_EN | CE2_EN |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. Clock Control 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | DSP_RSTM | RW | 0h | 0 = Reserved |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | CE1_SM | RW | 0h | When clock error1 is detected do soft mute using 0 = hardware mute sequence 1 = DSP mute sequence |
| 4 | CE1_IC | RW | 0h | Clock error detection block 1 input clock is 0 = ASI1 1 = ASI2 |
| 3-2 | CE2_IC[1:0] | RW | 0h | Clock error detection block 2 input clock is 0 = DAC modulator clock 1 = ADC modulator clock 2 = PLL clock 3 = reserved |
| 1 | CE1_EN | RW | 0h | Clock error detection block 1 is 0 = disabled 1 = enabled |
| 0 | CE2_EN | RW | 0h | Clock error detection block 2 is 0 = disabled 1 = enabled |

9.6.2.26 CLOCK_CTRL_2 (book=0x00 page=0x00 address=0x2D) [reset=17h]

Configures the clock error detection timeouts

Figure 68. CLOCK_CTRL_2 Register Address: 0x2D

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|---|---|--------------|---|---|
| Reserved | Reserved | Reserved | | | CE1_STO[2:0] | | |
| RW-0h | RW-0h | RW-2h | | | RW-7h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. Clock Control 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | Reserved | RW | 0h | Reserved |
| 5-3 | Reserved | RW | 2h | Reserved |
| 2-0 | CE1_STO[2:0] | RW | 7h | Clock error detection block 1 will shutdown the device and set signal PWR_ERR if a clock input does not occur for 0 = 2.73 ms 1 = 22 ms 2 = 44 ms 3 = 87ms 4 = 174 ms 5 = 350 ms 6 = 700 ms 7 = 1.4s |

9.6.2.27 CLOCK_CTRL_3 (book=0x00 page=0x00 address=0x2E) [reset=0h]

Configures the clock error detection timeouts

Figure 69. CLOCK_CTRL_3 Register Address: 0x2E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|----------|---|---|--------------|---|---|
| CE2_DRR[1:0] | | Reserved | | | CE2_STO[2:0] | | |
| RW-0h | | RW-0h | | | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. Clock Control 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-6 | CE2_DRR[1:0] | RW | 0h | For clock error detection block 2 gain ramp-down for DAC channel is 0 = 15 us per dB 1 = 30 us per dB 2 = 60 us per dB 3 = 120 us per dB |
| 5-3 | Reserved | RW | 0h | Reserved |
| 2-0 | CE2_STO[2:0] | RW | 0h | Clock error detection block 2 will shutdown the device and set signal PWR_ERR if a clock input does not occur for 0 = 2.73 ms 1 = 22 ms 2 = 44 ms 3 = 87ms 4 = 174 ms 5 = 350 ms 6 = 700 ms 7 = 1.4s |

9.6.2.28 ASI_CTRL_2 (book=0x00 page=0x00 address=0x2F) [reset=0h]

This register sets the PCM sampling rate.

Figure 70. ASI_CTRL_2 Register Address: 0x2F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|----------|-------------|---|
| Reserved | | | | | Reserved | ASI_SR[1:0] | |
| RW-0h | | | | | RW-0h | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. ASI Control 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7-3 | Reserved | RW | 0h | Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1-0 | ASI_SR[1:0] | RW | 0h | Sets the sampling rate of the ASI input data in PCM mode to 0 = 8kHz 1 = 16kHz 2 = 48 kHz 3 = 96kHz |

9.6.2.29 CLOCK_CTRL_4 (book=0x00 page=0x00 address=0x32) [reset=0h]

Configures the clock error detection recovery

Figure 71. CLOCK_CTRL_4 Register Address: 0x32

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|--------|--------|
| Reserved | | | | | | CE2_RM | CE1_RM |
| RW-0h | | | | | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. Clock Control 4 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-2 | Reserved | RW | 0h | Reserved |
| 1 | CE2_RM | RW | 0h | Device automatic recovery when clock error occurs on clock error block 2 0 = enabled 1 = disabled |

Table 51. Clock Control 4 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 0 | CE1_RM | RW | 0h | Device automatic recovery when clock error occurs on clock error block 1 0 = enabled 1 = disabled |

9.6.2.30 DEBUG_1 (book=0x00 page=0x00 address=0x35) [reset=0h]

Debug Register 1

Figure 72. DEBUG_1 Register Address: 0x35

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---------|--------|----------|
| Reserved | | | | | DPU_FRC | TM_I2V | INTG1_EN |
| RW-0h | | | | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 52. Debug Register 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-3 | Reserved | RW | 0h | Reserved |
| 2 | DPU_FRC | RW | 0h | 0 = don't force power down of dummy power up 1 = force power down of dummy power up (use this if dummy power up scheme is going to a hang state) |
| 1 | TM_I2V | RW | 0h | cont_tm_i2v_startup_en |
| 0 | INTG1_EN | RW | 0h | enz_intg1_clamping |

9.6.2.31 POWER_STATUS (book=0x00 page=0x00 address=0x64) [reset=0h]

This reports the blocks power state

Figure 73. POWER_STATUS Register Address: 0x64

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|----------|----------|----------|---|
| PUS_DAC | PUS_SPK | PUS_BST | PUS_BPT | PUS_ISNS | PUS_VSNS | Reserved | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 53. Power Up Status Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | PUS_DAC | R | 0h | DAC is 0 = powered down 1 = powered up |
| 6 | PUS_SPK | R | 0h | Class-D output is 0 = powered down 1 = powered up |
| 5 | PUS_BST | R | 0h | Boost is 0 = powered down 1 = powered up |
| 4 | PUS_BPT | R | 0h | Boost pass-thru is 0 = disabled 1 = enabled |
| 3 | PUS_ISNS | R | 0h | Current-sense ADC is 0 = powered down 1 = powered up |
| 2 | PUS_VSNS | R | 0h | Voltage-sense ADC is 0 = powered down 1 = powered up |
| 1-0 | Reserved | RW | 0h | Reserved |

9.6.2.32 DSP_BOOT_STATUS (book=0x00 page=0x00 address=0x65) [reset=0h]

Reports the status of the DSP booting.

Figure 74. DSP_BOOT_STATUS Register Address: 0x65

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------|---|--------|---|---|---|
| Reserved | | Reserved | | DSP_BS | | | |
| R-0h | | R-0h | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. DSP Boost Status Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-3 | Reserved | R | 0h | Reserved |
| 2 | DSP_BS | R | 0h | The DSP booting is 0 = completed; Host can write coefficient memories 0 = in progress ; Host cannot write coefficient memories |
| 1-0 | Reserved | R | 0h | Reserved |

9.6.2.33 INT_DET_1 (book=0x00 page=0x00 address=0x68) [reset=0h]

Sticky register used to indicate the source of an interrupt trigger. Register is cleared once read.

Figure 75. INT_DET_1 Register Address: 0x68

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|----------|--------|--------|--------|--------|----------|
| INT_OC | INT_UV | Reserved | INT_OT | INT_BO | INT_CL | INT_SC | Reserved |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. Interrupt Detected 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | INT_OC | R | 0h | Sticky bit indicating that speaker over current condition 0 = did not occurred since last read 1 = occurred since last read |
| 6 | INT_UV | R | 0h | Sticky bit indicating that analog under voltage condition 0 = did not occurred since last read 1 = occurred since last read |
| 5 | Reserved | R | 0h | Reserved |
| 4 | INT_OT | R | 0h | Sticky bit indicating that die over-temperature condition 0 = did not occurred since last read 1 = occurred since last read |
| 3 | INT_BO | R | 0h | Sticky bit indicating that brownout condition 0 = did not occurred since last read 1 = occurred since last read |
| 2 | INT_CL | R | 0h | Sticky bit indicating that the clock is lost condition 0 = did not occurred since last read 1 = occurred since last read |
| 1 | INT_SC | R | 0h | Sticky bit indicating that the SAR complete condition 0 = did not occurred since last read 1 = occurred since last read |
| 0 | Reserved | RW | 0h | Reserved |

9.6.2.34 INT_DET_2 (book=0x00 page=0x00 address=0x6C) [reset=0h]

Sticky register used to indicate the source of an interrupt trigger. Register is cleared once read.

Figure 76. INT_DET_2 Register Address: 0x6C

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | Reserved | INT_CLK1 | INT_CLK2 | Reserved | Reserved |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. Interrupt Detected 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | R | 0h | Reserved |
| 6 | Reserved | R | 0h | Reserved |
| 5 | Reserved | R | 0h | Reserved |
| 4 | Reserved | R | 0h | Reserved |
| 3 | INT_CLK1 | R | 0h | Sticky bit indicating that clock error 1 condition 0 = did not occurred since last read 1 = occurred since last read |
| 2 | INT_CLK2 | R | 0h | Sticky bit indicating that the clock error 2 condition 0 = did not occurred since last read 1 = occurred since last read |
| 1 | Reserved | R | 0h | Reserved |
| 0 | Reserved | R | 0h | Reserved |

9.6.2.35 LOW_POWER (book=0x00 page=0x00 address=0x79) [reset=0h]

Configures the low power shutdown mode.

Figure 77. LOW_POWER Register Address: 0x79

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBAT_POR | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. Lower Power Shutdown Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | VBAT_POR | RW | 0h | Disable POR and enter lower power mode. The AVDD and VBATT must be present when this mode is used. Low power is 0 = disabled 1 = enabled |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 0h | Reserved |
| 4 | Reserved | RW | 0h | Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | Reserved | RW | 0h | Reserved |
| 0 | Reserved | RW | 0h | Reserved |

9.6.2.36 BOOK (book=0x00 page=0x00 address=0x7F) [reset=0h]

Book Selection

Figure 78. BOOK Register Address: 0x7F

| | | | | | | | |
|-----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BOOK[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 58. Book Selection Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-0 | BOOK[7:0] | RW | 0h | Set the device book 0 = Book 0 1 = Book 1 ... 255 = Book 255 |

9.6.2.37 PAGE (book=0x00 page=0x01 address=0x00) [reset=1h]

Selects the page for the next read or write.

Figure 79. PAGE Register Address: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| PAGE[7:0] | | | | | | | |
| RW-1h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 59. Page Select Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-0 | PAGE[7:0] | RW | 1h | Selects the Register Page for the next read or write command |

9.6.2.38 ASI1_FORMAT (book=0x00 page=0x01 address=0x01) [reset=10h]

Configures the ASI1 format, wordlength, and tristate.

Figure 80. ASI1_FORMAT Register Address: 0x01

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|------------------|---|----------|---|---------------|
| ASI1_MODE[2:0] | | | ASI1_LENGTH[1:0] | | Reserved | | ASI1_TRISTATE |
| RW-0h | | | RW-2h | | RW-0h | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. ASI1 Format Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7-5 | ASI1_MODE[2:0] | RW | 0h | The ASI1 Input mode format is set to 0 = I2S 1 = DSP 2 = RJF , For non-zero values of ASI1_OFFSET1, LJF is preferred 3 = LJF 4 = MonoPCM 5-15 = Reserved |
| 4-3 | ASI1_LENGTH[1:0] | RW | 2h | Sets the ASI1 input word-length to 0 = 16bits 1 = 20bits 2 = 24bits 3 = 32bits |
| 2-1 | Reserved | RW | 0h | Reserved |
| 0 | ASI1_TRISTATE | RW | 0h | Tri-stating of DOUT for the extra ASI1_BCLK cycles after Data Transfer is over for a frame is 0 = Disabled 1 = Enabled |

9.6.2.39 ASI1_OFFSET_1 (book=0x00 page=0x01 address=0x03) [reset=0h]

Configures the ASI input offset. Offset is measured with respect to WCLK-rising edge in DSP Mode. Offset is not supported for RJF mode

Figure 81. ASI1_OFFSET_1 Register Address: 0x03

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASI1_OFFSET1[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. ASI1 Offset Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|-------------------|
| 7-0 | ASI1_OFFSET1[7:0] | RW | 0h | ASI1_OFFSET1[7:0] |

9.6.2.40 ASI1_BUSKEEP (book=0x00 page=0x01 address=0x05) [reset=0h]

Configures the buskeeper operation.

Figure 82. ASI1_BUSKEEP Register Address: 0x05

| | | | | | | | |
|----------|----------|-------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASI1_BKP | Reserved | | | | | | |
| RW-0h | | RW-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. ASI1 Buskeeper Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | ASI1_BKP | RW | 0h | Bus keep power down when DOUT is tri-stated to save IO power is 0 = disabled 1 = enabled |
| 6-0 | Reserved | RW | 0h | Reserved |

9.6.2.41 ASI1_BCLK (book=0x00 page=0x01 address=0x08) [reset=0h]

Configures the bit clock pin, timing, and free running mode

Figure 83. ASI1_BCLK Register Address: 0x08

| | | | | | | | | |
|----------|----------------|-------|---|---|----------|----------|----------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reserved | ASI1_BCLK[3:0] | | | | Reserved | ASI1_BCT | ASI1_FRM | |
| RW-0h | | RW-0h | | | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 63. ASI1 BCLK Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASI1_BCLK[3:0] | RW | 0h | ASI1 BCLK input is from 0 = GPIO1 (Preferred pin usage) 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2 | Reserved | RW | 0h | Reserved |

Table 63. ASI1 BCLK Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 1 | ASI1_BCT | RW | 0h | ASI1 BCLK timing as per timing protocol is 0 = normal 1 = inverted |
| 0 | ASI1_FRM | RW | 0h | ASI1 BCLK and WCLK are 0 = active in output modes only when ASI1 is active and codec is powered up 1 = is free-running |

9.6.2.42 ASI1_WCLK (book=0x00 page=0x01 address=0x09) [reset=8h]

Configures the word clock pin and timing

Figure 84. ASI1_WCLK Register Address: 0x09

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------------|---|---|---|----------|----------|----------|
| Reserved | ASI1_WCLK[3:0] | | | | Reserved | ASI1_WCT | Reserved |
| RW-0h | RW-1h | | | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. ASI1 WCLK Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASI1_WCLK[3:0] | RW | 1h | ASI1 WCLK input is from 0 = GPIO1 1 = GPIO2 (Preferred pin usage) 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | ASI1_WCT | RW | 0h | ASI1 WCLK timing as per timing protocol is 0 = normal 1 = inverted |
| 0 | Reserved | RW | 0h | Reserved |

9.6.2.43 ASI1_DIN_DOUT (book=0x00 page=0x01 address=0x0C) [reset=0h]

Configures the digital input and output ports.

Figure 85. ASI1_DIN_DOUT Register Address: 0x0C

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------------|---|---|---|----------|----------------|---|
| Reserved | ASI1_DIN[3:0] | | | | Reserved | ASI1_DOUT[1:0] | |
| RW-0h | RW-0h | | | | RW-0h | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 65. ASI1 DIN/DOUT Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASI1_DIN[3:0] | RW | 0h | ASI1 DIN input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 (Preferred pin usage) 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1-0 | ASI1_DOUT[1:0] | RW | 0h | ASI1 DOUT output is 0 = DOUT path, output buffer enabled only if i-sense is powered up 1 = ASI1_DIN, loopback 2 = ASI2_DIN, loopback 3 = DOUT path, output buffer enable controlled only based on ASI1 configuration |

9.6.2.44 ASI1_BDIV_CLK (book=0x00 page=0x01 address=0x0D) [reset=1h]

Selects the BDIV clock source

Figure 86. ASI1_BDIV_CLK Register Address: 0x0D

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|--------------------|---|---|
| Reserved | | | | | ASI1_BDIV_SRC[2:0] | | |
| RW-0h | | | | | RW-1h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 66. ASI1 BDIV Clock Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7-3 | Reserved | RW | 0h | Reserved |
| 2-0 | ASI1_BDIV_SRC[2:0] | RW | 1h | ASI1 bit clock divider (BDIV) source is 0 = NDIV_CLK (Generated On-Chip) 1 = DAC_MOD_CLK (Generated On-Chip) 2 = Reserved 3 = ADC_MOD_CLK (Generated On-Chip) 4 = ASI1_DAC_BCLK (at pin) 5 = Reserved 6 = ASI2_DAC_BCLK (at pin) 7 = Reserved |

9.6.2.45 ASI1_BDIV_RATIO (book=0x00 page=0x01 address=0x0E) [reset=2h]

Configure the BDIV ratio and power.

Figure 87. ASI1_BDIV_RATIO Register Address: 0x0E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|--------------------|---|---|---|---|---|---|
| ASI1_BDIV_P WR | ASI1_BDIV_RTO[6:0] | | | | | | |
| RW-0h | RW-2h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 67. ASI1 BDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | ASI1_BDIV_PWR | RW | 0h | The ASI1 BDIV divider is 0 = powered down 1 = powered up |
| 6-0 | ASI1_BDIV_RTO[6:0] | RW | 2h | The ASI1 BDIV ratio is 0 = 128 1 = 1 2 = 2 ... 126 = 126 127 = 127 |

9.6.2.46 ASI1_WDIV_RATIO (book=0x00 page=0x01 address=0x0F) [reset=20h]

Configure the WDIV ratio and power.

Figure 88. ASI1_WDIV_RATIO Register Address: 0x0F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|--------------------|---|---|---|---|---|---|
| ASI1_WDIV_P WR | ASI1_WDIV_RTO[6:0] | | | | | | |
| RW-0h | RW-20h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 68. ASI1 WDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | ASI1_WDIV_PWR | RW | 0h | The ASI1 WDIV divider is 0 = powered down 1 = powered up |
| 6-0 | ASI1_WDIV_RTO[6:0] | RW | 20h | The ASI1 WDIV ratio is 0 = 128 1 = 1 2 = 2 ... 126 = 126 127 = 127 |

9.6.2.47 ASI1_CLK_OUT (book=0x00 page=0x01 address=0x10) [reset=0h]

Configures the clock source for BCLK and WCLK

Figure 89. ASI1_CLK_OUT Register Address: 0x10

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|----------|-----------------|---|---|
| Reserved | ASI1_BCLKS[2:0] | | | Reserved | ASI1_WCLKS[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 69. ASI1 Clock Source Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | ASI1_BCLKS[2:0] | RW | 0h | ASI1 bit clock(BCLK) output source is 0 = ASI1 BDIV divider output 1 = ASI1 DAC clock 2 = Reserved 3 = ASI2 BDIV divider output 4 = ASI2 DAC clock 5=15 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |

Table 69. ASI1 Clock Source Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 2-0 | ASI1_WCLKS[2:0] | RW | 0h | ASI1 bit clock(WCLK) output source is 0 = ASI1 WDIV divider output 1 = ASI1 DAC clock 2 = Reserved 3 = ASI2 WDIV divider output 4 = ASI2 DAC clock 5=15 = Reserved |

9.6.2.48 ASI2_FORMAT (book=0x00 page=0x01 address=0x15) [reset=10h]

Configures the ASI2 format, wordlength, and tristate.

Figure 90. ASI2_FORMAT Register Address: 0x15

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|------------------|---|----------|---|---------------|
| ASI2_MODE[2:0] | | | ASI2_LENGTH[1:0] | | Reserved | | ASI2_TRISTATE |
| RW-0h | | | RW-2h | | RW-0h | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 70. ASI2 Format Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7-5 | ASI2_MODE[2:0] | RW | 0h | The ASI1 Input mode format is set to 0 = I2S 1 = DSP 2 = RJF , For non-zero values of ASI2_OFFSET1, LJF is preferred 3 = LJF 4 = MonoPCM 5-15 = Reserved |
| 4-3 | ASI2_LENGTH[1:0] | RW | 2h | Sets the ASI2 input word-length to 0 = 16bits 1 = 20bits 2 = 24bits 3 = 32bits |
| 2-1 | Reserved | RW | 0h | Reserved |
| 0 | ASI2_TRISTATE | RW | 0h | Tri-stating of DOUT for the extra ASI2_BCLK cycles after Data Transfer is over for a frame is 0 = Disabled 1 = Enabled |

9.6.2.49 ASI2_OFFSET_1 (book=0x00 page=0x01 address=0x17) [reset=0h]

Configures the ASI input offset. Offset is measured with respect to WCLK-rising edge in DSP Mode. Offset is not supported for RJF mode

Figure 91. ASI2_OFFSET_1 Register Address: 0x17

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|---|---|---|
| ASI2_OFFSET1[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. ASI2 Offset Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|-------------------|
| 7-0 | ASI2_OFFSET1[7:0] | RW | 0h | ASI2_OFFSET1[7:0] |

9.6.2.50 ASI2_BUSKEEP (book=0x00 page=0x01 address=0x19) [reset=0h]

Configures the buskeeper operation.

Figure 92. ASI2_BUSKEEP Register Address: 0x19

| | | | | | | | |
|----------|----------|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASI2_BKP | Reserved | | | | | | |
| RW-0h | RW-0h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. ASI2 Buskeeper Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | ASI2_BKP | RW | 0h | Bus keep power down when DOUT is tri-stated to save IO power is 0 = disabled 1 = enabled |
| 6-0 | Reserved | RW | 0h | Reserved |

9.6.2.51 ASI2_BCLK (book=0x00 page=0x01 address=0x1C) [reset=20h]

Configures the bit clock pin, timing, and free running mode

Figure 93. ASI2_BCLK Register Address: 0x1C

| | | | | | | | |
|----------|----------------|---|---|---|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | ASI2_BCLK[3:0] | | | | Reserved | ASI2_BCT | ASI2_FRM |
| RW-0h | RW-4h | | | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 73. ASI2 BCLK Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASI2_BCLK[3:0] | RW | 4h | ASI2 BCLK input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 (Preferred pin usage) 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | ASI2_BCT | RW | 0h | ASI2 BCLK timing as per timing protocol is 0 = normal 1 = inverted |
| 0 | ASI2_FRM | RW | 0h | ASI2 BCLK and WCLK are 0 = active in output modes only when ASI2 is active and codec is powered up 1 = is free-running |

9.6.2.52 ASI2_WCLK (book=0x00 page=0x01 address=0x1D) [reset=28h]

Configures the word clock pin and timing

Figure 94. ASI2_WCLK Register Address: 0x1D

| | | | | | | | |
|----------|----------------|---|---|---|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | ASI2_WCLK[3:0] | | | | Reserved | ASI2_WCT | Reserved |
| RW-0h | RW-5h | | | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 74. ASI2 WCLK Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASI2_WCLK[3:0] | RW | 5h | ASI2 WCLK input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 (Preferred pin usage) 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | ASI2_WCT | RW | 0h | ASI2 WCLK timing as per timing protocol is 0 = normal 1 = inverted |
| 0 | Reserved | RW | 0h | Reserved |

9.6.2.53 ASI2_DIN_DOUT (book=0x00 page=0x01 address=0x20) [reset=38h]

Configures the digital input and output ports.

Figure 95. ASI2_DIN_DOUT Register Address: 0x20

| | | | | | | | |
|----------|---------------|---|---|---|----------|----------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | ASI2_DIN[3:0] | | | | Reserved | ASI2_DOUT[1:0] | |
| RW-0h | RW-7h | | | | RW-0h | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 75. ASI2 DIN/DOUT Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASI2_DIN[3:0] | RW | 7h | ASI2 DIN input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 (Preferred pin usage) 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2 | Reserved | RW | 0h | Reserved |

Table 75. ASI2 DIN/DOUT Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 1-0 | ASI2_DOUT[1:0] | RW | 0h | ASI2 DOUT output is 0 = DOUT path, output buffer enabled only if i-sense is powered up 1 = ASI1_DIN, loopback 2 = ASI2_DIN, loopback 3 = DOUT path, output buffer enable controlled only based on ASI1 configuration |

9.6.2.54 ASI2_BDIV_CLK (book=0x00 page=0x01 address=0x21) [reset=1h]

Selects the BDIV clock source

Figure 96. ASI2_BDIV_CLK Register Address: 0x21

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|--------------------|---|---|
| Reserved | | | | | ASI2_BDIV_SRC[2:0] | | |
| RW-0h | | | | | RW-1h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. ASI2 BDIV Clock Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7-3 | Reserved | RW | 0h | Reserved |
| 2-0 | ASI2_BDIV_SRC[2:0] | RW | 1h | ASI1 bit clock divider (BDIV) source is 0 = NDIV_CLK (Generated On-Chip) 1 = DAC_MOD_CLK (Generated On-Chip) 2 = Reserved 3 = ADC_MOD_CLK (Generated On-Chip) 4 = ASI1_DAC_BCLK (at pin) 5 = Reserved 6 = ASI2_DAC_BCLK (at pin) 7 = Reserved |

9.6.2.55 ASI2_BDIV_RATIO (book=0x00 page=0x01 address=0x22) [reset=2h]

Configure the BDIV ratio and power.

Figure 97. ASI2_BDIV_RATIO Register Address: 0x22

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|--------------------|---|---|---|---|---|---|
| ASI2_BDIV_P WR | ASI2_BDIV_RTO[6:0] | | | | | | |
| RW-0h | RW-2h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. ASI2 BDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | ASI2_BDIV_PWR | RW | 0h | The ASI2 BDIV divider is 0 = powered down 1 = powered up |
| 6-0 | ASI2_BDIV_RTO[6:0] | RW | 2h | The ASI2 BDIV ratio is 0 = 128 1 = 1 2 = 2 ... 126 = 126 127 = 127 |

9.6.2.56 ASI2_WDIV_RATIO (book=0x00 page=0x01 address=0x23) [reset=20h]

Configure the WDIV ratio and power.

Figure 98. ASI2_WDIV_RATIO Register Address: 0x23

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|--------------------|---|---|---|---|---|---|
| ASI2_WDIV_P WR | ASI2_WDIV_RTO[6:0] | | | | | | |
| RW-0h | RW-20h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 78. ASI2 WDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | ASI2_WDIV_PWR | RW | 0h | The ASI2 WDIV divider is 0 = powered down 1 = powered up |
| 6-0 | ASI2_WDIV_RTO[6:0] | RW | 20h | The ASI2 WDIV ratio is 0 = 128 1 = 1 2 = 2 ... 126 = 126 127 = 127 |

9.6.2.57 ASI2_CLK_OUT (book=0x00 page=0x01 address=0x24) [reset=33h]

Configures the clock source for BCLK and WCLK

Figure 99. ASI2_CLK_OUT Register Address: 0x24

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|----------|-----------------|---|---|
| Reserved | ASI2_BCLKS[2:0] | | | Reserved | ASI2_WCLKS[2:0] | | |
| RW-0h | RW-3h | | | RW-0h | RW-3h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 79. ASI2 Clock Source Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | ASI2_BCLKS[2:0] | RW | 3h | ASI2 bit clock(BCLK) output source is 0 = ASI1 BDIV divider output 1 = ASI1 DAC clock 2 = Reserved 3 = ASI2 BDIV divider output 4 = ASI2 DAC clock 5=15 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | ASI2_WCLKS[2:0] | RW | 3h | ASI2 bit clock(WCLK) output source is 0 = ASI1 WDIV divider output 1 = ASI1 DAC clock 2 = Reserved 3 = ASI2 WDIV divider output 4 = ASI2 DAC clock 5=15 = Reserved |

9.6.2.58 GPIO1_PIN (book=0x00 page=0x01 address=0x3D) [reset=1h]

Configures BCLK1_GPIO1 pin.

Figure 100. GPIO1_PIN Register Address: 0x3D

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|----------|--------------|---|---|---|---|
| Reserved | GP1_VAL | Reserved | GP1_OUT[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-1h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 80. GPIO1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP1_VAL | RW | 0h | When value GP1_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |
| 4-0 | GP1_OUT[4:0] | RW | 1h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP1_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.59 GPIO2_PIN (book=0x00 page=0x01 address=0x3E) [reset=1h]

Configures WCLK1_GPIO2 pin.

Figure 101. GPIO2_PIN Register Address: 0x3E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|----------|--------------|---|---|---|---|
| Reserved | GP2_VAL | Reserved | GP2_OUT[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-1h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. GPIO2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP2_VAL | RW | 0h | When value GP2_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 81. GPIO2 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP2_OUT[4:0] | RW | 1h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP2_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.60 GPIO3_PIN (book=0x00 page=0x01 address=0x3F) [reset=10h]

Configures DOUT1_GPIO3 pin.

Figure 102. GPIO3_PIN Register Address: 0x3F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|----------|---------|----------|--------------|---|---|---|---|--|
| Reserved | GP3_VAL | Reserved | GP3_OUT[4:0] | | | | | |
| RW-0h | RW-0h | RW-0h | RW-10h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 82. GPIO3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP3_VAL | RW | 0h | When value GP3_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 82. GPIO3 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP3_OUT[4:0] | RW | 10h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP3_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.61 GPIO4_PIN (book=0x00 page=0x01 address=0x40) [reset=7h]

Configures IRQ_GPIO4 pin.

Figure 103. GPIO4_PIN Register Address: 0x40

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|----------|--------------|---|---|---|---|
| Reserved | GP4_VAL | Reserved | GP4_OUT[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-7h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 83. GPIO4 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP4_VAL | RW | 0h | When value GP4_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 83. GPIO4 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP4_OUT[4:0] | RW | 7h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP4_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.62 GPIO5_PIN (book=0x00 page=0x01 address=0x41) [reset=0h]

Configures BCLK2_GPIO5 pin.

Figure 104. GPIO5_PIN Register Address: 0x41

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|----------|--------------|---|---|---|---|
| Reserved | GP5_VAL | Reserved | GP5_OUT[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. GPIO5 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP5_VAL | RW | 0h | When value GP5_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 84. GPIO5 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP5_OUT[4:0] | RW | 0h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP5_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.63 GPIO6_PIN (book=0x00 page=0x01 address=0x42) [reset=0h]

Configures WCLK2_GPIO6 pin.

Figure 105. GPIO6_PIN Register Address: 0x42

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|----------|--------------|---|---|---|---|
| Reserved | GP6_VAL | Reserved | GP6_OUT[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. GPIO6 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP6_VAL | RW | 0h | When value GP6_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 85. GPIO6 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP6_OUT[4:0] | RW | 0h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP6_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.64 GPIO7_PIN (book=0x00 page=0x01 address=0x43) [reset=0h]

Configures DOUT2_GPIO7 pin.

Figure 106. GPIO7_PIN Register Address: 0x43

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|----------|---------|----------|--------------|---|---|---|---|--|
| Reserved | GP7_VAL | Reserved | GP7_OUT[4:0] | | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 86. GPIO7 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP7_VAL | RW | 0h | When value GP7_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 86. GPIO7 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP7_OUT[4:0] | RW | 0h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP7_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.65 GPIO8_PIN (book=0x00 page=0x01 address=0x44) [reset=0h]

Configures DIN2_GPIO8 pin.

Figure 107. GPIO8_PIN Register Address: 0x44

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|----------|---------|----------|--------------|---|---|---|---|--|
| Reserved | GP8_VAL | Reserved | GP8_OUT[4:0] | | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. GPIO8 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP8_VAL | RW | 0h | When value GP8_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 87. GPIO8 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP8_OUT[4:0] | RW | 0h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP8_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.66 GPIO9_PIN (book=0x00 page=0x01 address=0x45) [reset=0h]

Configures ICC_CLK_GPIO9 pin.

Figure 108. GPIO9_PIN Register Address: 0x45

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|----------|--------------|---|---|---|---|
| Reserved | GP9_VAL | Reserved | GP9_OUT[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. GPIO9 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP9_VAL | RW | 0h | When value GP9_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 88. GPIO9 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 4-0 | GP9_OUT[4:0] | RW | 0h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP9_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.67 GPIO10_PIN (book=0x00 page=0x01 address=0x46) [reset=0h]

Configures ICC_DOUT_GPIO10 pin.

Figure 109. GPIO10_PIN Register Address: 0x46

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|----------|----------|----------|---------------|---|---|---|---|--|
| Reserved | GP10_VAL | Reserved | GP10_OUT[4:0] | | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 89. GPIO10 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | GP10_VAL | RW | 0h | When value GP10_OUT=3, configure pin output to 0 = Low 1 = High |
| 5 | Reserved | RW | 0h | Reserved |

Table 89. GPIO10 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 4-0 | GP10_OUT[4:0] | RW | 0h | Pin is configured to 0 = disabled, buffers powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = output, use GP10_VAL to set value 4 = output, use GPBB_VAL to set value 5 = output, PDM clk output for PDM data input 6 = output, CLKOUT output 7 = output, INT1 interrupt 8 = output, INT2 interrupt 9 = output, INT3 interrupt 10 = output, INT4 interrupt 11 = Reserved 12 = output, ASI1_WCLK_OUT 13 = output, ASI1_BCLK_OUT 14-15 = Reserved 16 = ASI1_DOUT 17 = ASI1_WCLK_OUT 18 = ASI2_BCLK_OUT 19-20 = Reserved 21 = ASI2_DOUT 22-26 = Reserved 27 = ASIM_WCLK_OUT 28 = ASIM_BCLK_OUT 29 = ASIM_DOUT 30-31 = Reserved |

9.6.2.68 GPI_PIN (book=0x00 page=0x01 address=0x4D) [reset=0h]

Configures the GPI pins

Figure 110. GPI_PIN Register Address: 0x4D

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------------|---|----------------|---|----------------|---|
| Reserved | | GPI3_MODE[1:0] | | GPI2_MODE[1:0] | | GPI1_MODE[1:0] | |
| RW-0h | | RW-0h | | RW-0h | | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 90. GPI Pin Mode Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5-4 | GPI3_MODE[1:0] | RW | 0h | Pin GPI3 mode is 0 = disabled, powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = Reserved |
| 3-2 | GPI2_MODE[1:0] | RW | 0h | Pin GPI2 mode is 0 = disabled, powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = Reserved |
| 1-0 | GPI1_MODE[1:0] | RW | 0h | Pin GPI1 mode is 0 = disabled, powered down 1 = input, use input MUX for relevant function 2 = Reserved 3 = Reserved |

9.6.2.69 GPIO_HIZ_1 (book=0x00 page=0x01 address=0x4F) [reset=0h]

Configures high-Z state of GPIO1 and GPIO2

Figure 111. GPIO_HIZ_1 Register Address: 0x4F

| | | | | | | | |
|----------|--------------|---|---|----------|--------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | GP2_HIZ[2:0] | | | Reserved | GP1_HIZ[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. GPIO HiZ 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | GP2_HIZ[2:0] | RW | 0h | Pin GPIO2 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | GP1_HIZ[2:0] | RW | 0h | Pin GPIO1 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |

9.6.2.70 GPIO_HIZ_2 (book=0x00 page=0x01 address=0x50) [reset=0h]

Configures high-Z state of GPIO3 and GPIO4

Figure 112. GPIO_HIZ_2 Register Address: 0x50

| | | | | | | | |
|----------|--------------|---|---|----------|--------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | GP4_HIZ[2:0] | | | Reserved | GP3_HIZ[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. GPIO HiZ 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | GP4_HIZ[2:0] | RW | 0h | Pin GPIO4 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |

Table 92. GPIO HiZ 2 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 2-0 | GP3_HIZ[2:0] | RW | 0h | Pin GPIO3 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |

9.6.2.71 GPIO_HIZ_3 (book=0x00 page=0x01 address=0x51) [reset=0h]

Configures high-Z state of GPIO5 and GPIO6

Figure 113. GPIO_HIZ_3 Register Address: 0x51

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------------|---|---|----------|--------------|---|---|
| Reserved | GP6_HIZ[2:0] | | | Reserved | GP5_HIZ[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. GPIO HiZ 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | GP6_HIZ[2:0] | RW | 0h | Pin GPIO6 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | GP5_HIZ[2:0] | RW | 0h | Pin GPIO5 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |

9.6.2.72 GPIO_HIZ_4 (book=0x00 page=0x01 address=0x52) [reset=0h]

Configures high-Z state of GPIO7 and GPIO8

Figure 114. GPIO_HIZ_4 Register Address: 0x52

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------------|---|---|----------|--------------|---|---|
| Reserved | GP8_HIZ[2:0] | | | Reserved | GP7_HIZ[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. GPIO HiZ 4 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | GP8_HIZ[2:0] | RW | 0h | Pin GPIO8 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | GP7_HIZ[2:0] | RW | 0h | Pin GPIO7 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |

9.6.2.73 GPIO_HIZ_5 (book=0x00 page=0x01 address=0x53) [reset=0h]

Configures high-Z state of GPIO9 and GPIO10

Figure 115. GPIO_HIZ_5 Register Address: 0x53

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------------|---|---|----------|--------------|---|---|
| Reserved | GP10_HIZ[2:0] | | | Reserved | GP9_HIZ[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. GPIO HiZ 5 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | GP10_HIZ[2:0] | RW | 0h | Pin GPIO10 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | GP9_HIZ[2:0] | RW | 0h | Pin GPIO9 output is 0 = driven both LO/HI 1 = driven both LO/HI with buskeeper for use with outputs needing tri-stated 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Reserved |

9.6.2.74 BIT_BANG_OUT1 (book=0x00 page=0x01 address=0x58) [reset=0h]

GPIO pin state when using bit-bang output.

Figure 116. BIT_BANG_OUT1 Register Address: 0x58

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| BBO_GP8 | BBO_GP7 | BBO_GP6 | BBO_GP5 | BBO_GP4 | BBO_GP3 | BBO_GP2 | BBO_GP1 |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. Bit Bang Output 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 7 | BBO_GP8 | RW | 0h | GPIO8 pin output is 0 = low 1 = high |
| 6 | BBO_GP7 | RW | 0h | GPIO7 pin output is 0 = low 1 = high |
| 5 | BBO_GP6 | RW | 0h | GPIO6 pin output is 0 = low 1 = high |
| 4 | BBO_GP5 | RW | 0h | GPIO5 pin output is 0 = low 1 = high |
| 3 | BBO_GP4 | RW | 0h | GPIO4 pin output is 0 = low 1 = high |
| 2 | BBO_GP3 | RW | 0h | GPIO3 pin output is 0 = low 1 = high |
| 1 | BBO_GP2 | RW | 0h | GPIO2 pin output is 0 = low 1 = high |
| 0 | BBO_GP1 | RW | 0h | GPIO1 pin output is 0 = low 1 = high |

9.6.2.75 BIT_BANG_OUT2 (book=0x00 page=0x01 address=0x59) [reset=0h]

GPIO pin state when using pin as bit-bang output.

Figure 117. BIT_BANG_OUT2 Register Address: 0x59

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|----------|---------|
| Reserved | | | | | | BBO_GP10 | BBO_GP9 |
| RW-0h | | | | | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 97. Bit Bang Output 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-2 | Reserved | RW | 0h | Reserved |
| 1 | BBO_GP10 | RW | 0h | GPIO10 pin output is 0 = low 1 = high |
| 0 | BBO_GP9 | RW | 0h | GPIO9 pin output is 0 = low 1 = high |

9.6.2.76 BIT_BANG_IN1 (book=0x00 page=0x01 address=0x5A) [reset=0h]

GPIO pin value when used as bit-bang input.

Figure 118. BIT_BANG_IN1 Register Address: 0x5A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| BBI_GP8 | BBI_GP7 | BBI_GP6 | BBI_GP5 | BBI_GP4 | BBI_GP3 | BBI_GP2 | BBI_GP1 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. Bit Bang Input 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 7 | BBI_GP8 | R | 0h | GPIO8 pin input is 0 = low 1 = high |
| 6 | BBI_GP7 | R | 0h | GPIO7 pin input is 0 = low 1 = high |
| 5 | BBI_GP6 | R | 0h | GPIO6 pin input is 0 = low 1 = high |
| 4 | BBI_GP5 | R | 0h | GPIO5 pin input is 0 = low 1 = high |
| 3 | BBI_GP4 | R | 0h | GPIO4 pin input is 0 = low 1 = high |
| 2 | BBI_GP3 | R | 0h | GPIO3 pin input is 0 = low 1 = high |
| 1 | BBI_GP2 | R | 0h | GPIO2 pin input is 0 = low 1 = high |
| 0 | BBI_GP1 | R | 0h | GPIO1 pin input is 0 = low 1 = high |

9.6.2.77 BIT_BANG_IN2 (book=0x00 page=0x01 address=0x5B) [reset=0h]

GPIO pin value when used as bit-bang input.

Figure 119. BIT_BANG_IN2 Register Address: 0x5B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|----------|---------|
| Reserved | | | | | | BBI_GP10 | BBI_GP9 |
| RW-0h | | | | | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 99. Bit Bang Input 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-2 | Reserved | RW | 0h | Reserved |
| 1 | BBI_GP10 | RW | 0h | GPIO10 pin input is 0 = low 1 = high |
| 0 | BBI_GP9 | RW | 0h | GPIO9 pin input is 0 = low 1 = high |

9.6.2.78 BIT_BANG_IN3 (book=0x00 page=0x01 address=0x5C) [reset=0h]

GPI pin value when used as bit-bang input.

Figure 120. BIT_BANG_IN3 Register Address: 0x5C

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|----------|----------|----------|
| Reserved | | | | | BBI_GPI3 | BBI_GPI2 | BBI_GPI1 |
| RW-0h | | | | | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 100. Bit Bang Input 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-3 | Reserved | RW | 0h | Reserved |
| 2 | BBI_GPI3 | RW | 0h | GPI3 pin input is 0 = low 1 = high |
| 1 | BBI_GPI2 | RW | 0h | GPI2 pin input is 0 = low 1 = high |
| 0 | BBI_GPI1 | RW | 0h | GPI1 pin input is 0 = low 1 = high |

9.6.2.79 ASIM_BUSKEEP (book=0x00 page=0x01 address=0x60) [reset=0h]

Configures the buskeeper operation.

Figure 121. ASIM_BUSKEEP Register Address: 0x60

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|---|---|---|---|---|---|
| ASIM_BKP | Reserved | | | | | | |
| RW-0h | RW-0h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 101. ASIM Buskeeper Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | ASIM_BKP | RW | 0h | Bus keep power down when DOUT is tri-stated to save IO power is 0 = disabled 1 = enabled |
| 6-0 | Reserved | RW | 0h | Reserved |

9.6.2.80 ASIM_MODE (book=0x00 page=0x01 address=0x61) [reset=8h]

specifies the format and slots for the Interchip Communication (ICC) Interface

Figure 122. ASIM_MODE Register Address: 0x61

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------------|---|---|---|---------|---------|
| ASIM_INT | Reserved | ASIM_WCNT[3:0] | | | | ASIM_RS | ASIM_WS |
| RW-0h | RW-0h | RW-2h | | | | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 102. ASIM Mode Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | ASIM_INT | RW | 0h | ASIM interface is 0 = Non-ICC set by ASIM_FORMAT 1 = ICC interface for multichip |
| 6 | Reserved | RW | 0h | Reserved |

Table 102. ASIM Mode Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 5-2 | ASIM_WCNT[3:0] | RW | 2h | The number of words(32-bit samples) in one frame of the ICC. The total number of bit transmitted is (1+words)*33 0 = Reserved 1 = 1 word 2 = 2 words ... 13 = 13 words 14 = 14 words 15 = Reserved |
| 1 | ASIM_RS | RW | 0h | The device will read the following ICC slots and transfer data to DSP 0 = only it own slot 1 = all slots |
| 0 | ASIM_WS | RW | 0h | The device will write the following ICC slots and transfer data to DSP 0 = only it own slot 1 = all slots |

9.6.2.81 ASIM_NUM_DEV (book=0x00 page=0x01 address=0x62) [reset=0h]

specifies the number of devices on the Interchip Communication (ICC) Interface

Figure 123. ASIM_NUM_DEV Register Address: 0x62

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------------|---|---|----------|--------------|---|---|
| Reserved | ASIM_TND[2:0] | | | Reserved | ASIM_DN[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 103. ASIM Number Devices Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | ASIM_TND[2:0] | RW | 0h | Total number of devices on the ICC interface bus 0 = 8 1 = 1 2 = 2 ... 6 = 6 7 = 7 |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | ASIM_DN[2:0] | RW | 0h | The device number for this device on the ICC interface bus 0 = 1 1 = 2 ... 6 = 7 7 = 8 |

9.6.2.82 ASIM_FORMAT (book=0x00 page=0x01 address=0x63) [reset=10h]

Configures the ASI2 format, wordlength, and tristate.

Figure 124. ASIM_FORMAT Register Address: 0x63

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|------------------|---|----------|---|---------------|
| ASIM_MODE[2:0] | | | ASI2_LENGTH[1:0] | | Reserved | | ASI2_TRISTATE |
| RW-0h | | | RW-2h | | RW-0h | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 104. ASIM Format Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7-5 | ASIM_MODE[2:0] | RW | 0h | The ASIM Input mode format is set to 0 = I2S 1 = DSP 2 = RJF , For non-zero values of ASIM_OFFSET1, LJF is preferred 3 = LJF 4 = MonoPCM 5-15 = Reserved |
| 4-3 | ASI2_LENGTH[1:0] | RW | 2h | Sets the ASIM input word-length to 0 = 16bits 1 = 20bits 2 = 24bits 3 = 32bits |
| 2-1 | Reserved | RW | 0h | Reserved |
| 0 | ASI2_TRISTATE | RW | 0h | Tri-stating of DOUT for the extra ASIM_BCLK cycles after Data Transfer is over for a frame is 0 = Disabled 1 = Enabled |

9.6.2.83 ASIM_BDIV_CLK (book=0x00 page=0x01 address=0x64) [reset=1h]

Selects the BDIV clock source and input/output mode for WCLK/BCLK.

Figure 125. ASIM_BDIV_CLK Register Address: 0x64

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|---|---|--------------------|---|---|
| ASIM_BCD | ASIM_WCD | Reserved | | | ASIM_BDIV_SRC[2:0] | | |
| RW-0h | RW-0h | RW-0h | | | RW-1h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 105. ASIM BDIV Clock Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7 | ASIM_BCD | RW | 0h | ASIM BCLK is 0 = input 1 = output; use only in ICC mode if device number is 1 |
| 6 | ASIM_WCD | RW | 0h | ASIM WCLK is 0 = input 1 = output |
| 5-3 | Reserved | RW | 0h | Reserved |
| 2-0 | ASIM_BDIV_SRC[2:0] | RW | 1h | ASIM bit clock divider (BDIV) source is 0 = NDIV_CLK (Generated On-Chip) 1 = DAC_MOD_CLK (Generated On-Chip) 2 = Reserved 3 = ADC_MOD_CLK (Generated On-Chip) 4 = ASI1_DAC_BCLK (at pin) 5 = ASI1_ADC_BCLK (at pin) 6 = ASI2_DAC_BCLK (at pin) 7 = ASI2_ADC_BCLK (at pin) |

9.6.2.84 ASIM_BDIV_RATIO (book=0x00 page=0x01 address=0x65) [reset=2h]

Configure the BDIV ratio and power.

Figure 126. ASIM_BDIV_RATIO Register Address: 0x65

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|--------------------|---|---|---|---|---|---|
| ASIM_BDIV_P WR | ASIM_BDIV_RTO[6:0] | | | | | | |
| RW-0h | RW-2h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 106. ASIM BDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | ASIM_BDIV_PWR | RW | 0h | The ASIM BDIV divider is 0 = powered down 1 = powered up |
| 6-0 | ASIM_BDIV_RTO[6:0] | RW | 2h | The ASIM BDIV ratio is 0 = 128 1 = 1 2 = 2 ... 126 = 126 127 = 127 |

9.6.2.85 ASIM_WDIV_RATIO_1 (book=0x00 page=0x01 address=0x66) [reset=0h]

Configure the WDIV ratio and power.

Figure 127. ASIM_WDIV_RATIO_1 Register Address: 0x66

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----------|---|---|---|---|--------------------|---|
| ASIM_WDIV_PWR | Reserved | | | | | ASIM_WDIV_RTO[9:8] | |
| RW-0h | RW-0h | | | | | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 107. ASIM WDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 7 | ASIM_WDIV_PWR | RW | 0h | The ASIM WDIV divider is 0 = powered down 1 = powered up |
| 6-2 | Reserved | RW | 0h | Reserved |
| 1--8 | ASIM_WDIV_RTO[9:0] | RW | 0h | MSB for ASIM WDIV divider |

9.6.2.86 ASIM_WDIV_RATIO_2 (book=0x00 page=0x01 address=0x67) [reset=20h]

Configure the WDIV ratio.

Figure 128. ASIM_WDIV_RATIO_2 Register Address: 0x67

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---|---|---|---|---|---|---|
| ASIM_WDIV_RTO[7:0] | | | | | | | |
| RW-20h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 108. ASIM WDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7-0 | ASIM_WDIV_RTO[7:0] | RW | 20h | LSB for ASIM WDIV. Number for ASIM_BDIV clock cycles in on ASIM_WCLK frame 0 = 1024 1 = 1 2 = 2 ... 1022 = 1022 1023 = 1023 |

9.6.2.87 ASIM_BCLK (book=0x00 page=0x01 address=0x68) [reset=40h]

Configures the bit clock pin.

Figure 129. ASIM_BCLK Register Address: 0x68

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------------|---|---|---|----------|---|---|
| Reserved | ASIM_BCLK[3:0] | | | | Reserved | | |
| RW-0h | RW-8h | | | | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 109. ASIM BCLK Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASIM_BCLK[3:0] | RW | 8h | ASIM BCLK input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 (Preferred pin usage) 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2-0 | Reserved | RW | 0h | Reserved |

9.6.2.88 ASIM_WCLK (book=0x00 page=0x01 address=0x69) [reset=38h]

Configures the word clock pin.

Figure 130. ASIM_WCLK Register Address: 0x69

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------------|---|---|---|----------|---|---|
| Reserved | ASIM_WCLK[3:0] | | | | Reserved | | |
| RW-0h | RW-7h | | | | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 110. ASIM WCLK Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASIM_WCLK[3:0] | RW | 7h | ASIM BCLK input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 (Preferred pin usage) 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 15-31 = Reserved |
| 2-0 | Reserved | RW | 0h | Reserved |

9.6.2.89 ASIM_DIN (book=0x00 page=0x01 address=0x6A) [reset=70h]

Configures the ASIM data input pin and clock detection 2 interrupt generation.

Figure 131. ASIM_DIN Register Address: 0x6A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------------|---|---|------------------|---|---|---|
| Reserved | ASIM_DIN[3:0] | | | INT_GEN_CH2[2:0] | | | |
| RW-0h | RW-Eh | | | RW-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 111. ASI1 DIN Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-3 | ASIM_DIN[3:0] | RW | Eh | ASIM BCLK input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 14 = GPI3 (Preferred pin usage) 15-31 = Reserved |
| 2-0 | INT_GEN_CH2[2:0] | RW | 0h | Clock halt detection 2 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.90 INT_GEN_1 (book=0x00 page=0x01 address=0x6C) [reset=0h]

Assign speaker over-current and device over-voltage to specific interrupt

Figure 132. INT_GEN_1 Register Address: 0x6C

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|----------|-----------------|---|---|
| Reserved | INT_GEN_OC[2:0] | | | Reserved | INT_GEN_OV[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 112. Interrupt Generation 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | INT_GEN_OC[2:0] | RW | 0h | Speaker over current is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |

Table 112. Interrupt Generation 1 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 2-0 | INT_GEN_OV[2:0] | RW | 0h | Device over voltage is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.91 INT_GEN_2 (book=0x00 page=0x01 address=0x6D) [reset=0h]

Assign clock error deteciton 1 and die over temperature to specific interrupt

Figure 133. INT_GEN_2 Register Address: 0x6D

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------------------|---|---|----------|-----------------|---|---|
| Reserved | INT_GEN_CE1[2:0] | | | Reserved | INT_GEN_OT[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 113. Interrupt Generation 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | INT_GEN_CE1[2:0] | RW | 0h | Clock error detection 1 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | INT_GEN_OT[2:0] | RW | 0h | Die over-temperature is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.92 INT_GEN_3 (book=0x00 page=0x01 address=0x6E) [reset=0h]

Assign clock error deteciton 2 and brownout to specific interrupt

Figure 134. INT_GEN_3 Register Address: 0x6E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|----------|------------------|---|---|
| Reserved | INT_GEN_BO[2:0] | | | Reserved | INT_GEN_CE2[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 114. Interrupt Generation 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | INT_GEN_BO[2:0] | RW | 0h | Device brownout is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

Table 114. Interrupt Generation 3 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | INT_GEN_CE2[2:0] | RW | 0h | Clock error detection 2 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.93 INT_GEN_4 (book=0x00 page=0x01 address=0x6F) [reset=0h]

Assign SAR complete and clock halt 1 to specific interrupt

Figure 135. INT_GEN_4 Register Address: 0x6F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|----------|-----------------|---|---|
| Reserved | INT_GEN_SC[2:0] | | | Reserved | INT_GEN_CL[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 115. Interrupt Generation 4 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | INT_GEN_SC[2:0] | RW | 0h | SAR measurement complete is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | INT_GEN_CL[2:0] | RW | 0h | Clock lost halt 1 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.94 INT_GEN_5 (book=0x00 page=0x01 address=0x70) [reset=0h]

Assign DSP Interrupt 1 and DSP interrupt 2 to specific interrupt

Figure 136. INT_GEN_5 Register Address: 0x70

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------------|---|---|----------|-------------------|---|---|
| Reserved | INT_GEN_DSP1[2:0] | | | Reserved | INT_GEN_DSP2[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 116. Interrupt Generation 5 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | INT_GEN_DSP1[2:0] | RW | 0h | DSP output interrupt 1 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | INT_GEN_DSP2[2:0] | RW | 0h | DSP output interrupt 2 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.95 INT_GEN_6 (book=0x00 page=0x01 address=0x71) [reset=0h]

Assign DSP Interrupt 3 and DSP interrupt 4 to specific interrupt

Figure 137. INT_GEN_6 Register Address: 0x71

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------------|---|---|----------|-------------------|---|---|
| Reserved | INT_GEN_DSP3[2:0] | | | Reserved | INT_GEN_DSP4[2:0] | | |
| RW-0h | RW-0h | | | RW-0h | RW-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 117. Interrupt Generation 6 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6-4 | INT_GEN_DSP3[2:0] | RW | 0h | DSP output interrupt 3 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | INT_GEN_DSP4[2:0] | RW | 0h | DSP output interrupt 4 is 0 = not used in the generation of interrupt 1 = used in the generation of INT1 2 = used in the generation of INT2 3 = used in the generation of INT3 4 = used in the generation of INT4 5-7 = Reserved |

9.6.2.96 INT_IND_MODE (book=0x00 page=0x01 address=0x72) [reset=0h]

Configure how interrupts are reported.

Figure 138. INT_IND_MODE Register Address: 0x72

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|---------------|---|---------------|---|---------------|---|
| INT1_IND[1:0] | | INT2_IND[1:0] | | INT3_IND[1:0] | | INT4_IND[1:0] | |
| RW-0h | | RW-0h | | RW-0h | | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 118. Interrupt Indication Mode Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7-6 | INT1_IND[1:0] | RW | 0h | Interrupt 1 pin will indicate an interrupt as 0 = one active high pulse of duration 2 ms 1 = multiple active high pulses of duration 2 ms with period 4 ms until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high based instantaneous interrupt value |
| 5-4 | INT2_IND[1:0] | RW | 0h | Interrupt 2 pin will indicate an interrupt as 0 = one active high pulse of duration 2 ms 1 = multiple active high pulses of duration 2 ms with period 4 ms until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high based instantaneous interrupt value |
| 3-2 | INT3_IND[1:0] | RW | 0h | Interrupt 3 pin will indicate an interrupt as 0 = one active high pulse of duration 2 ms 1 = multiple active high pulses of duration 2 ms with period 4 ms until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high based instantaneous interrupt value |
| 1-0 | INT4_IND[1:0] | RW | 0h | Interrupt 4 pin will indicate an interrupt as 0 = one active high pulse of duration 2 ms 1 = multiple active high pulses of duration 2 ms with period 4 ms until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high until INT_STICKY_1 and INT_STICKY_2 are read to be cleared. 2 = active high based instantaneous interrupt value |

9.6.2.97 MAIN_CLK_PIN (book=0x00 page=0x01 address=0x73) [reset=Dh]

Configures the main clock input source.

Figure 139. MAIN_CLK_PIN Register Address: 0x73

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|-------------------|---|---|---|
| Reserved | | | | MAIN_CLK_DIN[3:0] | | | |
| RW-0h | | | | RW-Dh | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 119. Main Clock Source Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-4 | Reserved | RW | 0h | Reserved |
| 3-0 | MAIN_CLK_DIN[3:0] | RW | Dh | NDIV_MUX_CLKIN input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 (Preferred pin usage) 14 = GPI3 15 = PLL_CLK generated on-chip |

9.6.2.98 PLL_CLK_PIN (book=0x00 page=0x01 address=0x74) [reset=Dh]

Configures the PLL clock input source.

Figure 140. PLL_CLK_PIN Register Address: 0x74

| | | | | | | | |
|----------|---|---|---|------------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | PLL_CLK_DIN[3:0] | | | |
| RW-0h | | | | RW-Dh | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 120. PLL Clock Source Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7-4 | Reserved | RW | 0h | Reserved |
| 3-0 | PLL_CLK_DIN[3:0] | RW | Dh | PLL_CLKIN input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 (Preferred pin usage) 14 = GPI3 15 = from internal oscillator |

9.6.2.99 CLKOUT_MUX (book=0x00 page=0x01 address=0x75) [reset=Dh]

Configures the CDIV_CLKIN clock input source.

Figure 141. CLKOUT_MUX Register Address: 0x75

| | | | | | | | |
|----------|---|---|---|-----------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | CLKOUT_DIN[4:0] | | | |
| RW-0h | | | | RW-Dh | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 121. CDIV_CLKIN Clock Source Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-5 | Reserved | RW | 0h | Reserved |
| 4-0 | CLKOUT_DIN[4:0] | RW | Dh | CDIV_CLKIN input is from 0 = GPIO1 1 = GPIO2 2 = GPIO3 3 = GPIO4 4 = GPIO5 5 = GPIO6 6 = GPIO7 7 = GPIO8 8 = GPIO9 9 = GPIO10 10-11 = Reserved 12 = GPI1 13 = GPI2 (Preferred pin usage) 14 = GPI3 15 = PLL_CLK 16 = DAC_MOD_CLK 17 = ADC_MOD_CLK 18 = NDIV_CLK 19-31 = Reserved |

9.6.2.100 CLKOUT_CDIV_RATIO (book=0x00 page=0x01 address=0x76) [reset=1h]

Configure the CDIV ratio and power.

Figure 142. CLKOUT_CDIV_RATIO Register Address: 0x76

| | | | | | | | |
|----------|---|---------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CDIV_PWR | | CDIV_RTO[6:0] | | | | | |
| RW-0h | | RW-1h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 122. CLKOUT CDIV Ratio Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | CDIV_PWR | RW | 0h | The CDIV divider is 0 = powered down 1 = powered up |
| 6-0 | CDIV_RTO[6:0] | RW | 1h | The CDIV ratio is 0 = 128 1 = 1 2 = 2 ... 126 = 126 127 = 127 |

9.6.2.101 I2C_MISC (book=0x00 page=0x01 address=0x7C) [reset=0h]

Configures various I2C options

Figure 143. I2C_MISC Register Address: 0x7C

| | | | | | | | |
|----------|--------|----------|----------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | I2C_HD | I2C_GCAE | Reserved | | | | |
| RW-0h | RW-0h | RW-0h | RW-0h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 123. I2C Misc Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | I2C_HD | RW | 0h | I2C hang detecton. Read to clear. Do not write this bit high. I2C hang is 0 = detected 1 = not detected |
| 5 | I2C_GCAE | RW | 0h | When enabled the part will respond to the configured I2C address as well as the general call I2C address. I2C general call address for multi-part loading is 0 = disabled 1 = enabled |
| 4-0 | Reserved | RW | 0h | Reserved |

9.6.2.102 DEVICE_ID (book=0x00 page=0x01 address=0x7D) [reset=12h]

Used to indicate device

Figure 144. DEVICE_ID Register Address: 0x7D

| | | | | | | | |
|-------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEV_ID[7:0] | | | | | | | |
| R-12h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 124. Device ID Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|-------------|
| 7-0 | DEV_ID[7:0] | R | 12h | |

9.6.2.103 PAGE (book=0x00 page=0x02 address=0x00) [reset=1h]

Selects the page for the next read or write.

Figure 145. PAGE Register Address: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| PAGE[7:0] | | | | | | | |
| RW-1h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 125. Page Select Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-0 | PAGE[7:0] | RW | 1h | Selects the Register Page for the next read or write command |

9.6.2.104 RAMP_CTRL (book=0x00 page=0x02 address=0x06) [reset=0h]

Class-D Ramp Control

Figure 146. RAMP_CTRL Register Address: 0x06

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------------|---|----------|---|-------------------|---|
| Reserved | | RAMP_FREQ[1:0] | | Reserved | | RAMP_FREQMOD[1:0] | |
| RW-0h | | RW-0h | | RW-0h | | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 126. Class-D Ramp Control Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5-4 | RAMP_FREQ[1:0] | RW | 0h | Rampgen frequency is 0 = 384kHz, use this for Fs of 48kpsps and its multiples 1 = 352.8kHz, Use this for Fs of 44.1kpsps and its multiples 2 = Reserved |
| 3-2 | Reserved | RW | 0h | Reserved |
| 1-0 | RAMP_FREQMOD[1:0] | RW | 0h | When SSM is enabled the ramp is modulated by 0 = Reserved 1 = +-5 % 2 = +-10 % 3 = Reserved |

9.6.2.105 PROTECTION_CFG (book=0x00 page=0x02 address=0x09) [reset=3h]

Configures the Devices Protection Blocks

Figure 147. PROTECTION_CFG Register Address: 0x09

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|-------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | OT_RT | Reserved | Reserved |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-1h | RW-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 127. Configures the Devices Protection Blocks Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 0h | Reserved |
| 4 | Reserved | RW | 0h | Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2 | OT_RT | RW | 0h | Die over-temperature retry is 0 = Enabled 1 = Disabled |
| 1 | Reserved | RW | 1h | Reserved |
| 0 | Reserved | RW | 1h | Reserved |

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TAS2557 is a digital input high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-H boost converter. In auto-passthrough mode, the Class-H boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide louder audio than a stand-alone amplifier connected directly to the battery. To enable load monitoring, the TAS2557 constantly measures the current and voltage across the load and provides a digital stream of this information back to a processor.

10.2 Typical Application

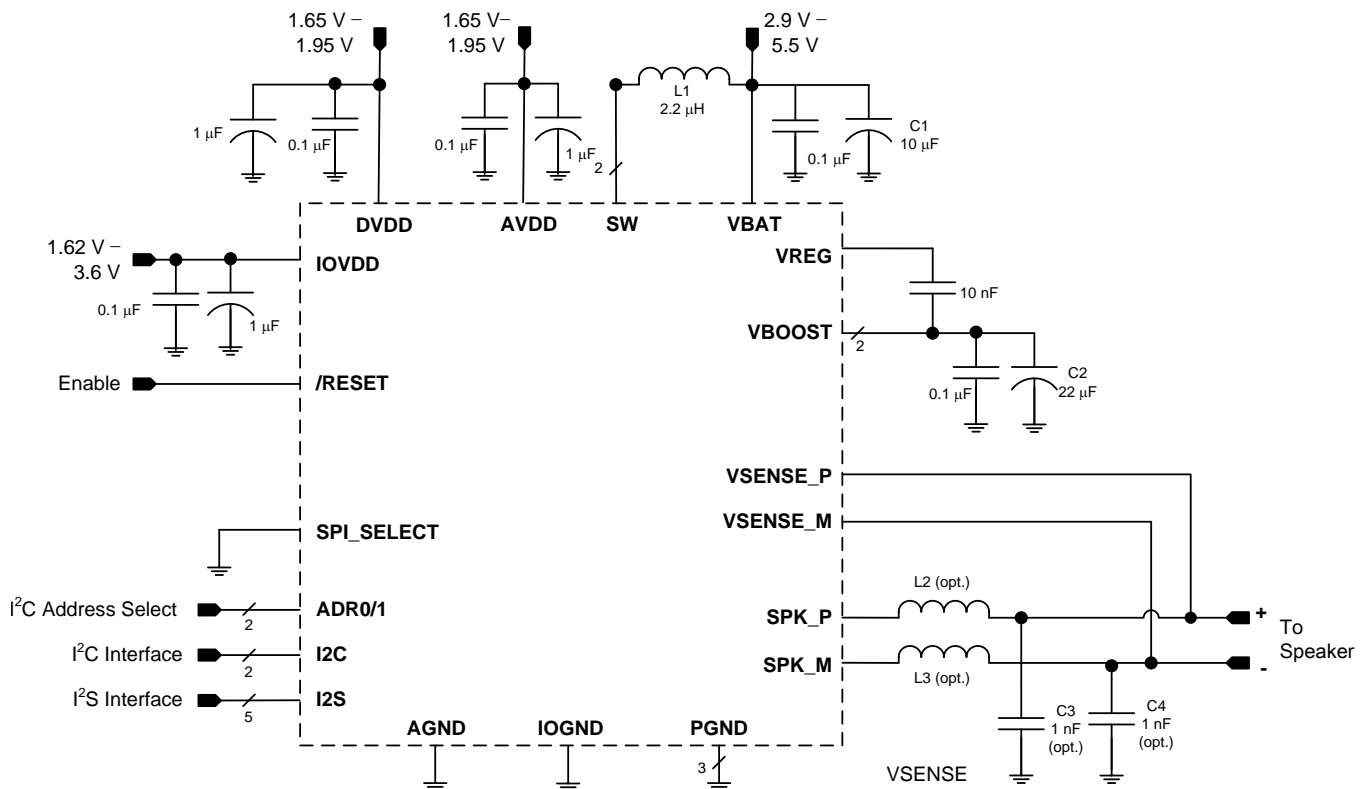


Figure 148. Typical Application - Digital Audio Input

Typical Application (continued)

Table 128. Recommended External Components

| COMPONENT | DESCRIPTION | SPECIFICATION | MIN | TYP | MAX | UNIT |
|-----------|---|-------------------------------|-----|------|-------|------|
| L1 | Boost Converter Inductor | Inductance, 20% Tolerance | 1 | 2.2 | | μH |
| | | Saturation Current | | 3.1 | | A |
| L2, L3 | EMI Filter Inductors (optional). These are not recommended as it degrades THD+N performance. The TAS2557 device is a filter-less Class-D and does not require these bead inductors. | Impedance at 100MHz | | 120 | | Ω |
| | | DC Resistance | | | 0.095 | Ω |
| | | DC Current | | | 2 | A |
| | | Size | | 0402 | | EIA |
| C1 | Boost Converter Input Capacitor | Capacitance, 20% Tolerance | 10 | | | μF |
| C2 | Boost Converter Output Capacitor | Type | X5R | | | |
| | | Capacitance, 20% Tolerance | 22 | | 47 | μF |
| | | Rated Voltage | 16 | | | V |
| | | Capacitance at 8.5 V derating | 3.3 | | | μF |
| C3, C4 | EMI Filter Capacitors (optional, must use L2, L3 if C3, C4 used) | Capacitance | | 1 | | nF |

10.2.1 Design Requirements

For this design example, use the parameters shown in [Table 129](#).

Table 129. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---------------------------------|---------------------------------|
| Audio Input | Digital Audio, I ² S |
| Current and Voltage Data Stream | Digital Audio, I ² S |
| Mono or Stereo Configuration | Mono |
| Max Output Power at 1% THD+N | 3.8 W |

10.2.2 Detailed Design Procedure

10.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See [General I²C Operation](#) for information on changing the I²C address of the TAS2557 to support stereo operation. Mono or stereo configuration does not impact the device performance.

10.2.2.2 Boost Converter Passive Devices

The boost converter requires three passive devices that are labeled L1, C1 and C2 in [Figure 148](#) and whose specifications are provided in [Table 128](#). These specifications are based on the design of the TAS2557 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current for L1 should be > ILIM to deliver Class-D peak power.

Additionally, the ratio of L1/C2 (the derated value of C2 at 8.5 V should be used in this ratio) has to be lesser than 1/3 for boost stability. This 1/3 ratio should be maintained including the worst case variation of L1 and C2. To satisfy sufficient energy transfer, L1 needs to be >= 1μH at the boost switching frequency (~1.7 MHz). Using a 1μH will have more boost ripple than a 2.2μH but the PSRR should minimize the effect from the additional ripple. Finally, the minimum C2 (derated value at 8.5 V) should be > 3.3μF for Class-D power delivery specification.

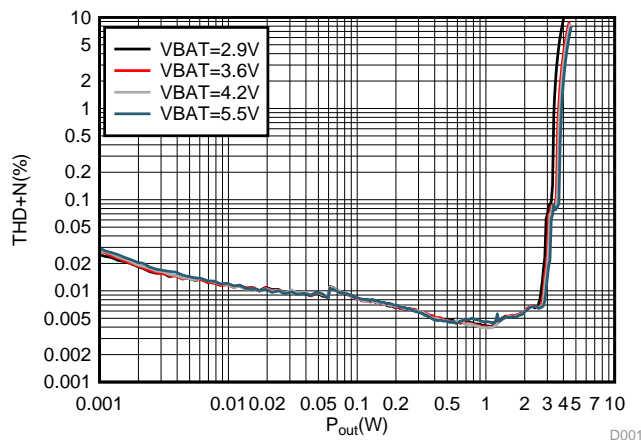
10.2.2.3 EMI Passive Devices

The TAS2557 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output devices. These passive devices that are labeled L2, L3, C3 and C4 in [Figure 148](#) and their recommended specifications are provided in [Table 128](#). If C3 and C4 are used, they must be placed after L2 and L3 respectively to maintain the stability of the output stage.

10.2.2.4 Miscellaneous Passive Devices

- VREG Capacitor: Needs to be 10 nF to meet boost and Class-D power delivery and efficiency specs.

10.2.3 Application Curve



Freq = 1kHz VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, $\overline{\text{RESET}}$ = IOVDD, $R_L = 8 \Omega + 33 \mu\text{H}$, I2S digital input, ROM mode 1

Figure 149. THD+N vs Output Power (8 Ω) for Digital Input

10.3 Initialization Setup

To configure the TAS2557, follow these steps.

1. Bring-up the power supplies as in [Power Supply Sequencing](#).
2. Set the $\overline{\text{RESET}}$ terminal to HIGH.
3. Follow the software sequence in section [Device Power Up and Unmute Sequence](#)

11 Power Supply Recommendations

11.1 Power Supplies

The TAS2557 requires four power supplies:

- Boost Input (terminal: VBAT)
 - Voltage: 2.9 V to 5.5 V
 - Max Current: 5 A for ILIM = 3.0 A (default)
- Analog Supply (terminal: AVDD)
 - Voltage: 1.65 V to 1.95 V
 - Max Current: 30 mA
- Digital Supply (terminal: DVDD)
 - Voltage: 1.65 V to 1.95 V
 - Max Current: 50 mA
- Digital I/O Supply (terminal: IOVDD)
 - Voltage: 1.62 V to 3.6 V
 - Max Current: 5 mA

The decoupling capacitors for the power supplies should be placed close to the device terminals. For VBAT, IOVDD, DVDD and AVDD, a small decoupling capacitor of 0.1 μ F should be placed close to the device terminals. Refer to [Figure 148](#) for the schematic.

11.2 Power Supply Sequencing

The following power sequence should be followed for power up and power down. If the recommended sequence is not followed there can be large current in device due to faults in level shifters and diodes becoming forward biased. The T_{delay} between power supplies should be large enough for the power rails to settle.

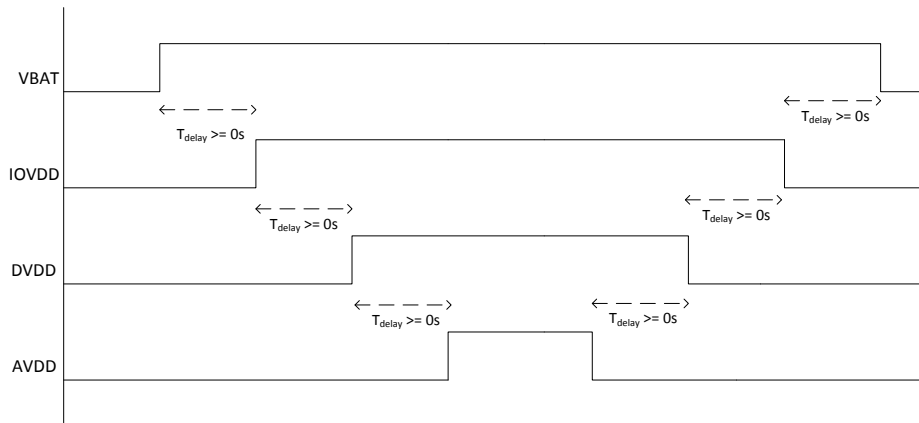


Figure 150. Power Supply Sequence for Power-Up and Power-Down

When the supplies have settled, the /RESET terminal can be set HIGH to operate the device. Additionally the /RESET pin can be tied to IOVDD and the internal DVDD POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100 μ s to allow the OTP to load. The above sequence should be completed before any I²C operation.

12 Layout

12.1 Layout Guidelines

- Place the boost inductor between VBAT and SW close to device terminals with no VIAS between the device terminals and the inductor.
- Place the capacitor between VREG and VBOOST close to device terminals with no VIAS between the device terminals and capacitor.
- Place the capacitor between VBOOST/VBAT and GND close to device terminals with no VIAS between the device terminals and capacitor.
- Do not use VIAS for traces that carry high current. These include the traces for VBOOST, SW, VBAT, PGND and the speaker SPK_P, SPK_M.
- Use epoxy filled vias for the interior pads.
- Connect VSENSE+, VSENSE- as close as possible to the speaker.
 - VSENSE+, VSENSE- should be connected between the EMI ferrite filter and the speaker if EMI ferrites are used on SPK_P, SPK_M.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in [Figure 148](#) and described in [Power Supply Recommendations](#).
- Place EMI ferrites, if used, close to the device.

12.2 Layout Example

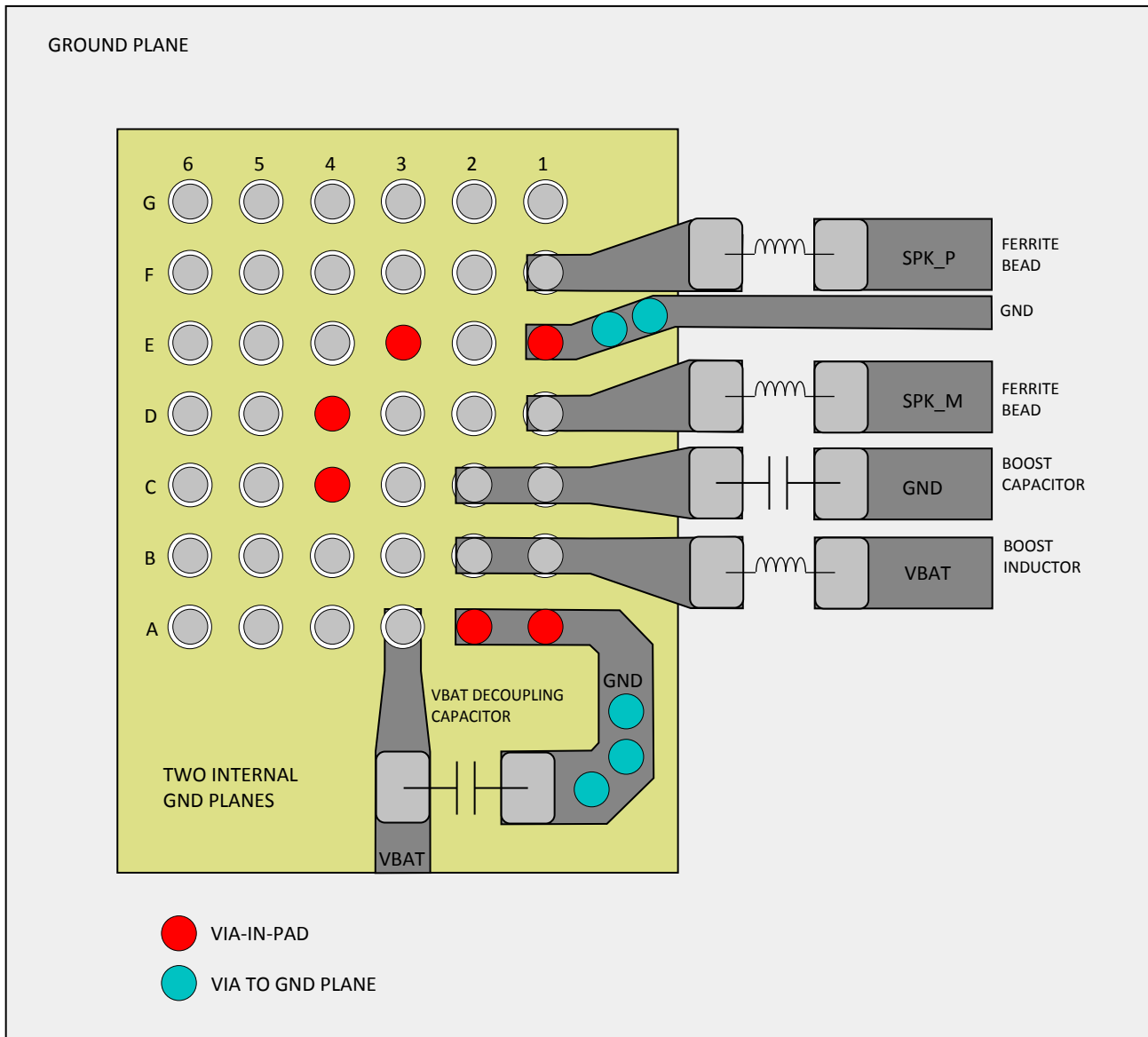


Figure 151. TAS2557 Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

PurePath, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

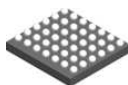
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Package Dimensions

The TAS2557 uses a 42-ball, 0.5-mm pitch DSBGA package.

Package Dimensions (continued)

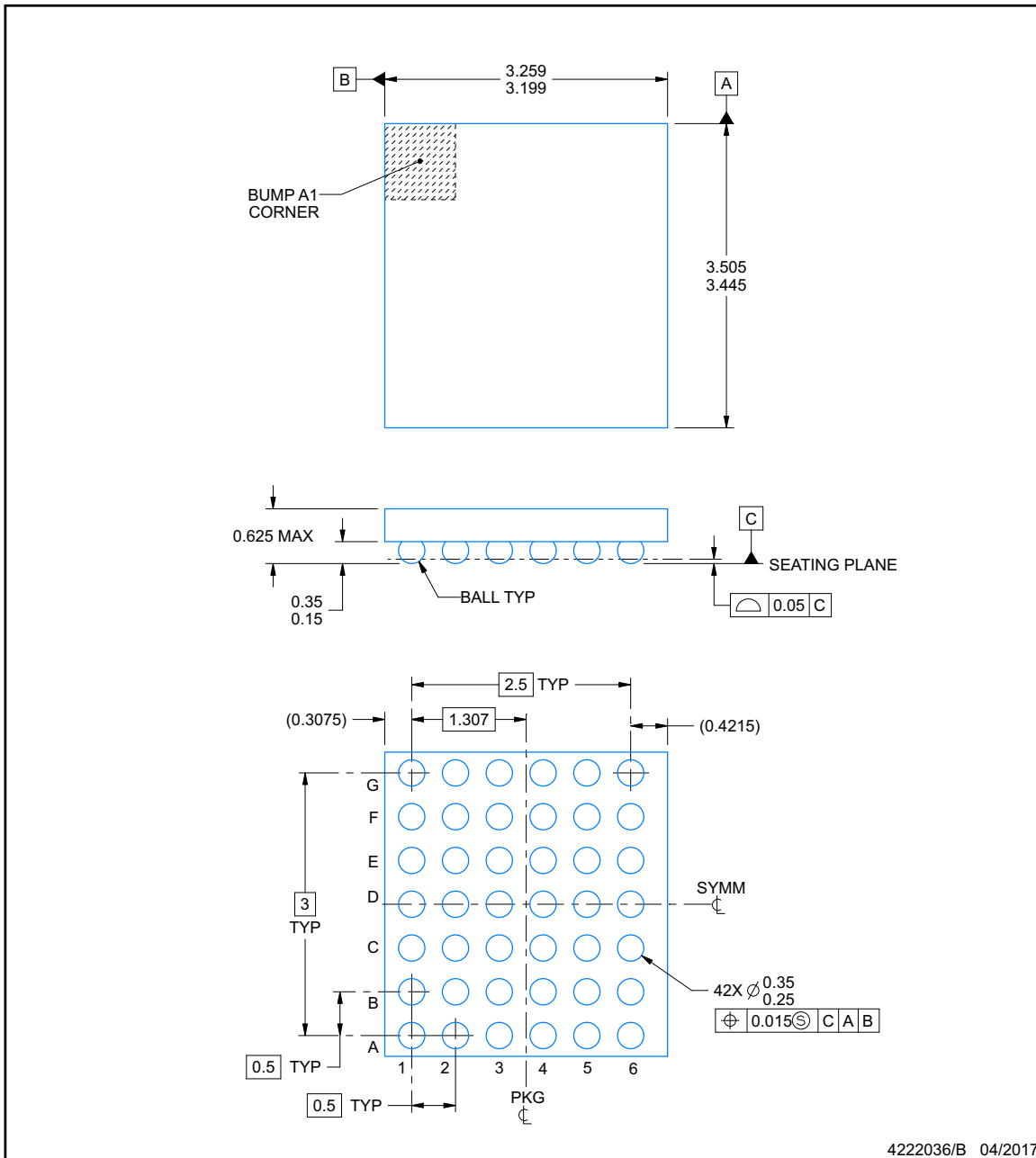
TAS255xYZ, SN____255xYZ
YZ0042-C01



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Package Dimensions (continued)

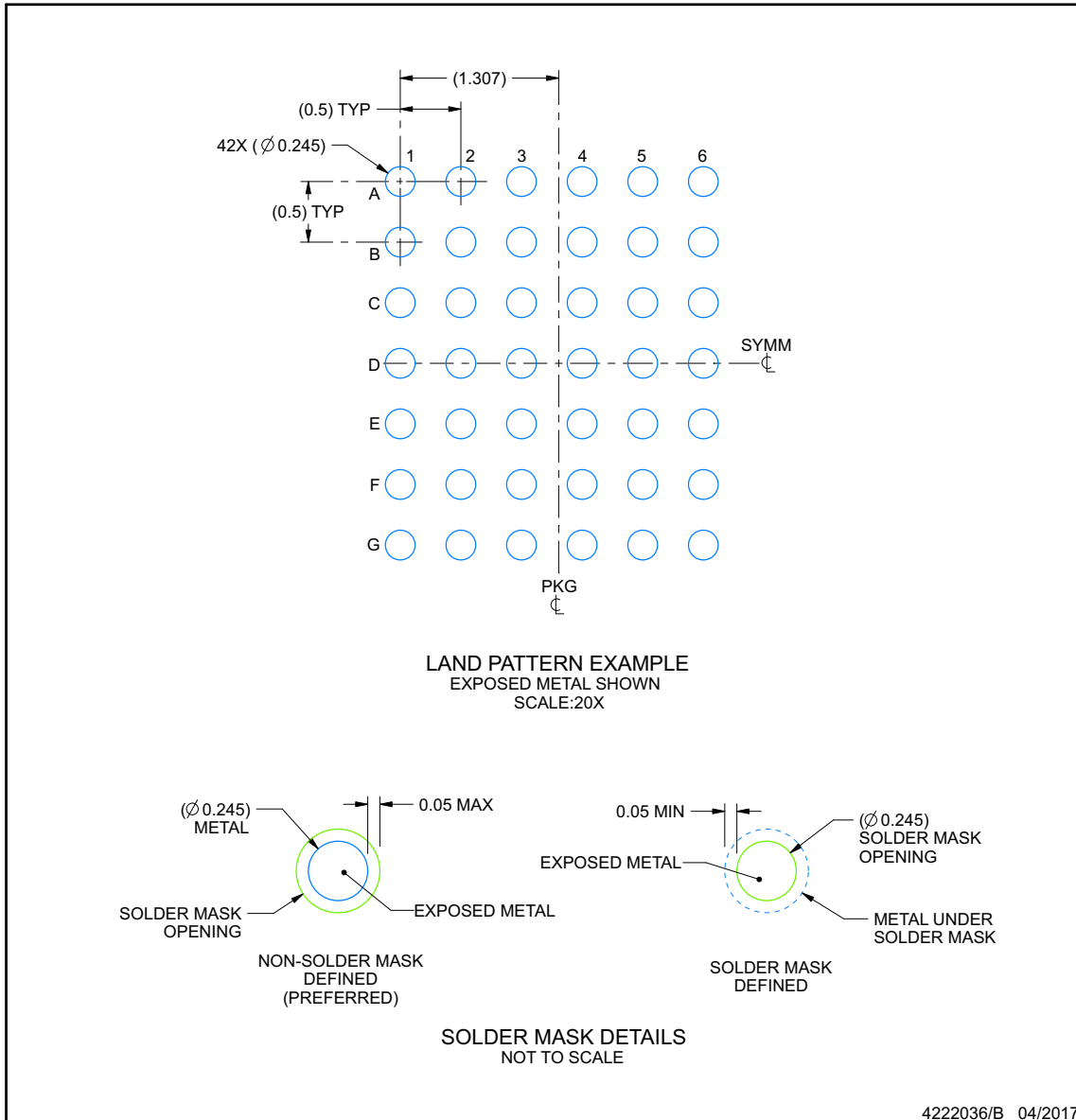
TAS255xYZ, SN____255xYZ

EXAMPLE BOARD LAYOUT

YZ0042-C01

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

Package Dimensions (continued)

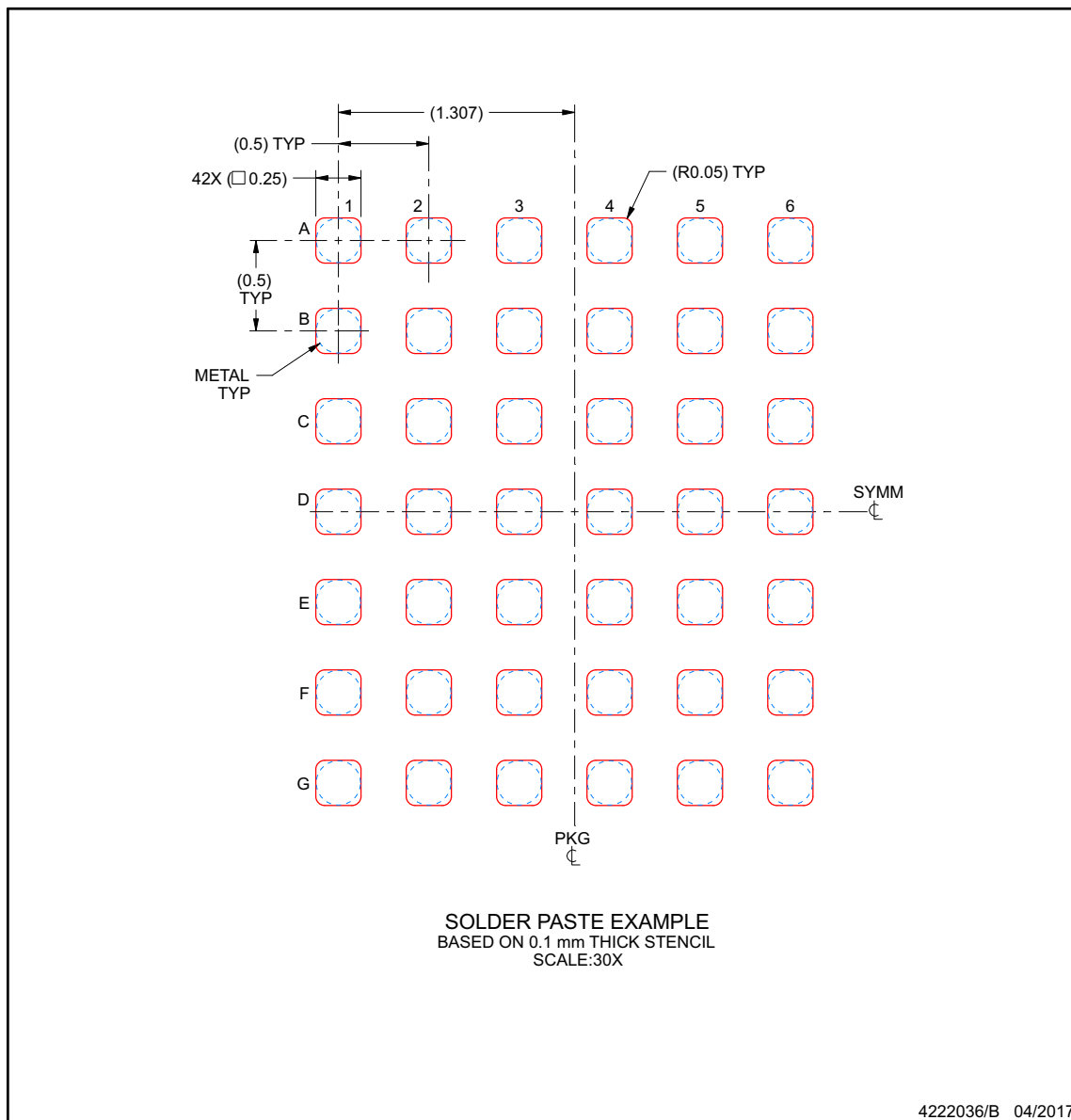
TAS255xYZ, SN____255xYZ

EXAMPLE STENCIL DESIGN

YZ0042-C01

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAS2557YZR | ACTIVE | DSBGA | YZ | 42 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 2557 | Samples |
| TAS2557YZT | ACTIVE | DSBGA | YZ | 42 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 2557 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS2557YZR | DSBGA | YZ | 42 | 3000 | 330.0 | 12.4 | 3.4 | 3.75 | 0.82 | 8.0 | 12.0 | Q1 |
| TAS2557YZR | DSBGA | YZ | 42 | 3000 | 330.0 | 12.4 | 3.4 | 3.75 | 0.82 | 8.0 | 12.0 | Q1 |
| TAS2557YZT | DSBGA | YZ | 42 | 250 | 330.0 | 12.4 | 3.4 | 3.75 | 0.82 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS2557YZR | DSBGA | YZ | 42 | 3000 | 380.0 | 380.0 | 50.0 |
| TAS2557YZR | DSBGA | YZ | 42 | 3000 | 367.0 | 367.0 | 35.0 |
| TAS2557YZT | DSBGA | YZ | 42 | 250 | 380.0 | 380.0 | 50.0 |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated