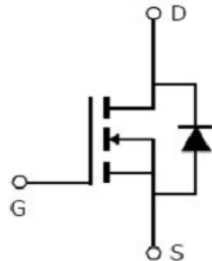


# PTF2N65

650V/2A N-Channel Advanced Power MOSFET

## Features

- $R_{DS(on)}$  (Typical 4.9 $\Omega$ )@ $V_{GS}=30V$
- Improved dv/dt Capability, High Ruggedness
- 100% Avalanche Tested
- Maximum Junction Temperature Range (150°C)



## Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Rating	Unit
<b>Common Ratings (<math>T_J=25^\circ\text{C}</math> Unless Otherwise Noted)</b>			
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650	V
$T_J$	Maximum Junction Temperature	-50 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-50 to 150	$^\circ\text{C}$
$I_S$	Diode Continuous Forward Current	2	A

## Mounted on Large Heat Sink ( $T_J=25^\circ\text{C}$ Unless Otherwise Noted)

$I_{DM}$	Pulse Drain Current Tested (Silicon Limit) (Note1)		8	A
$I_D$	Continuous Drain current@ $V_{GS}=10V$	$T_C=25^\circ\text{C}$	2	A
$P_D$	Maximum Power Dissipation		39	W
$E_{AS}$	Sing Pulsed Avalanche Energy (Note2)		20	mJ
$R_{\theta JC}$	Thermal Resistance Junction-to-Case		3.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient		65	$^\circ\text{C/W}$

Note :

1. Repetitive Rating:Pulse width limited by maximum junction temperature.
2.  $I_L=15.7\text{mH}, I_{AS}=7\text{ A}, V_{DD}=50\text{V}, R_G=25\Omega, T_J=25^\circ\text{C}$

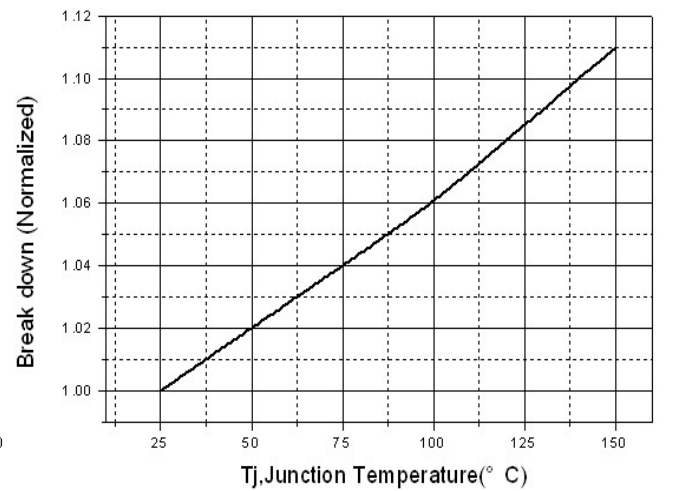
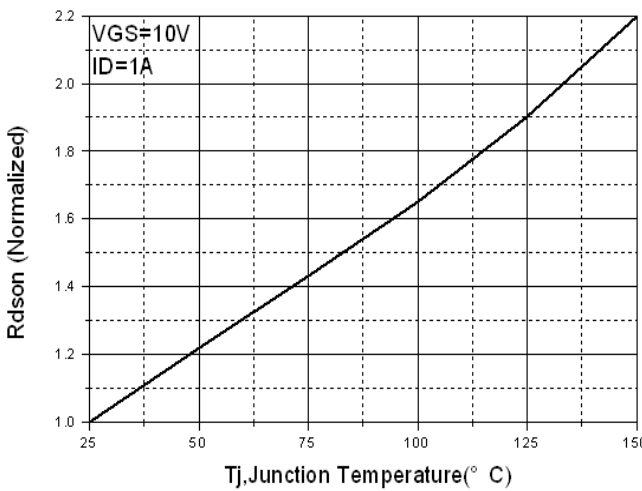
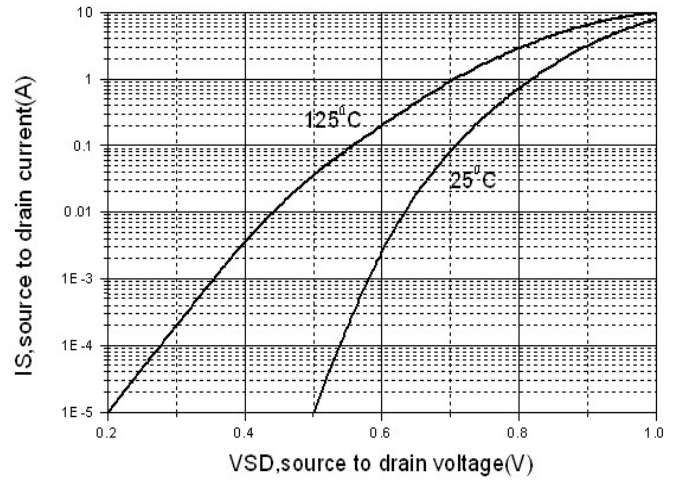
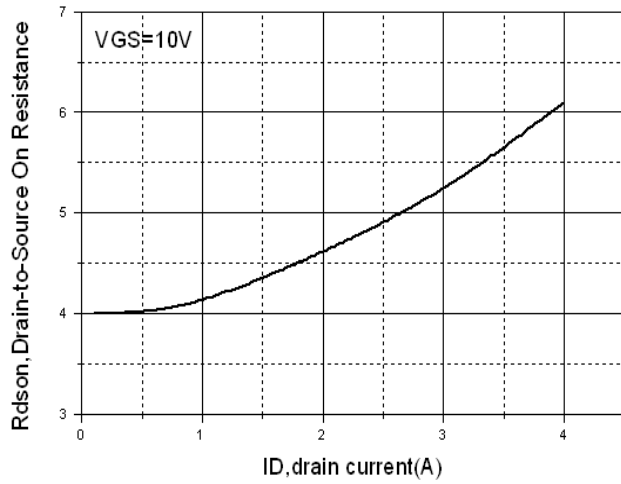
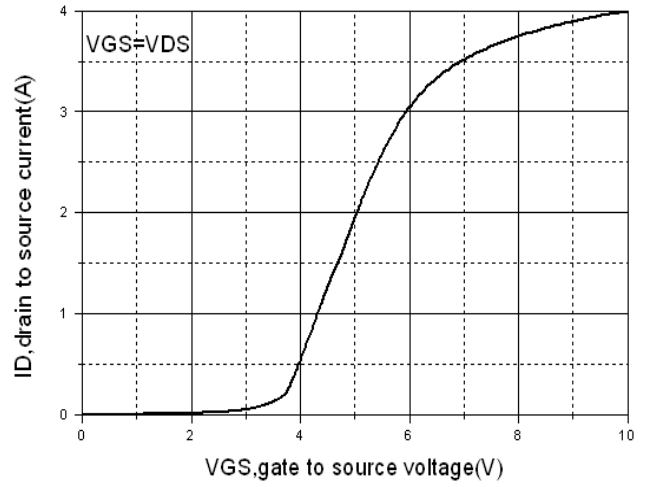
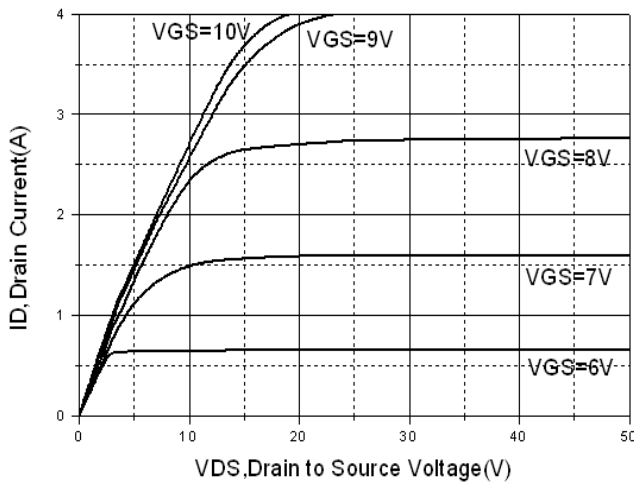
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise stated)</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	650	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain current(Tc=25°C)	VDS=600V,VGS=0V	--	--	1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	VGS=±30V,VDS=0V	--	--	±100	nA
V <sub>GS(TH)</sub>	Gate Threshold Voltage	VDS=VGS,ID=250μA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance note A	VGS=10V,ID=1A	--	4.9	6	Ω
<b>Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise stated) <sup>note B</sup></b>						
C <sub>iss</sub>	Input Capacitance	VDS=25V,VGS=0V, f=1MHz	--	350	--	pF
C <sub>oss</sub>	Output Capacitance		--	30	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	1.5	--	pF
Q <sub>g</sub>	Total Gate Charge	VDS=480V,ID=2A VGS=10V	--	6.6	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	1.4	--	nC
<b>Switching Characteristics <sup>note B</sup></b>						
t <sub>d(on)</sub>	Turn-on Delay Time	VDS=300V ID=2A, RG=25Ω VGS=10V	--	14.5	--	nS
t <sub>r</sub>	Turn-on Rise Time		--	10	--	nS
t <sub>d(off)</sub>	Turn-Off Delay Time		--	28	--	nS
t <sub>f</sub>	Turn-Off Fall Time		--	13	--	nS
<b>Source- Drain Diode Characteristics@ T<sub>J</sub> = 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	IS= 2A,VGS=0V	--	0.85	1.4	V

Note:

A: Pulse Test: pulse width ≤ 300 us, duty cycle ≤ 2%

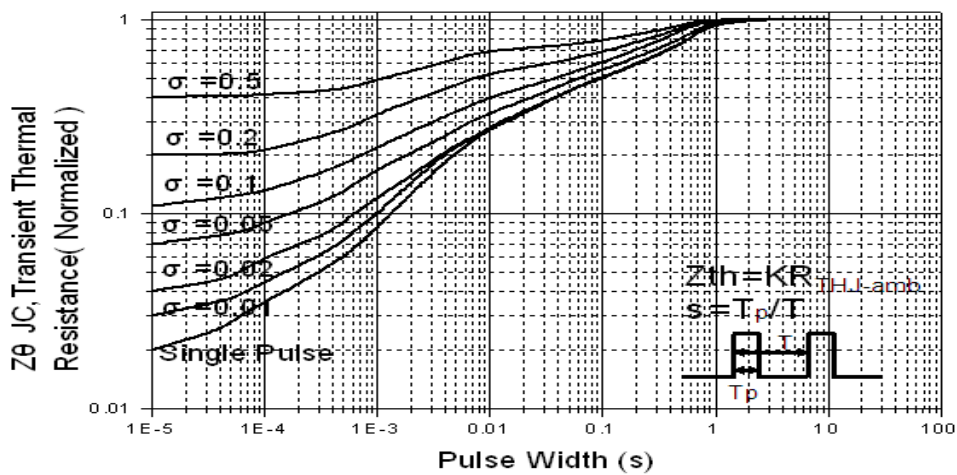
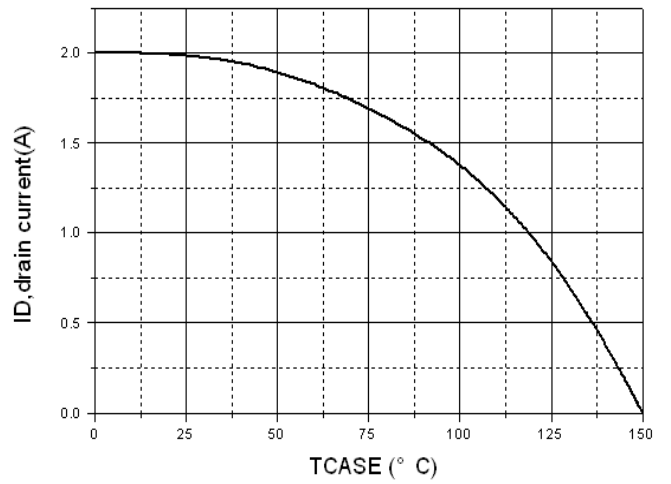
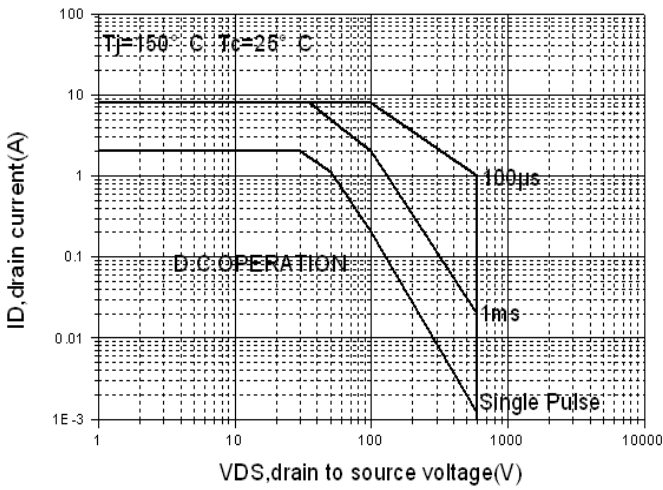
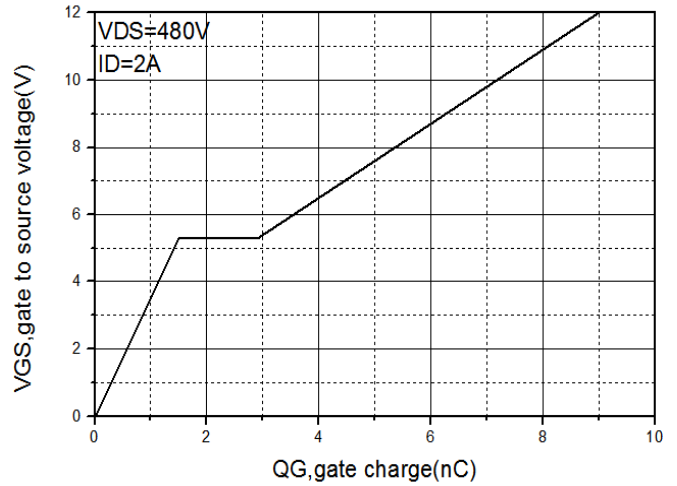
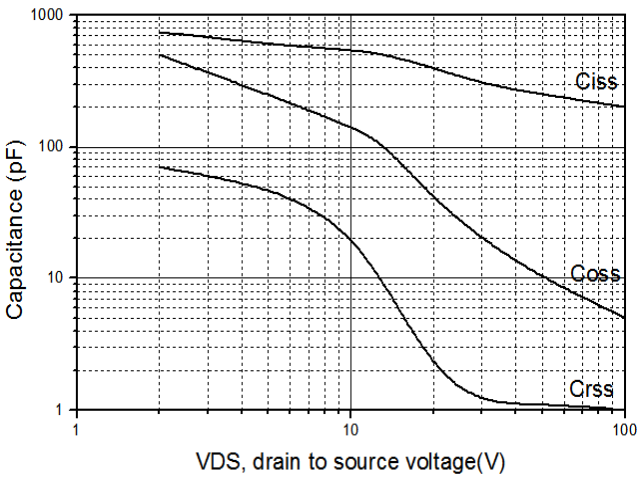
B: Guaranteed by design, not subject to production testing.

Typical characteristic curve:



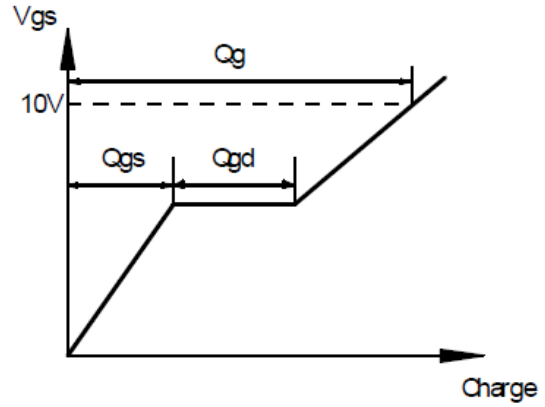
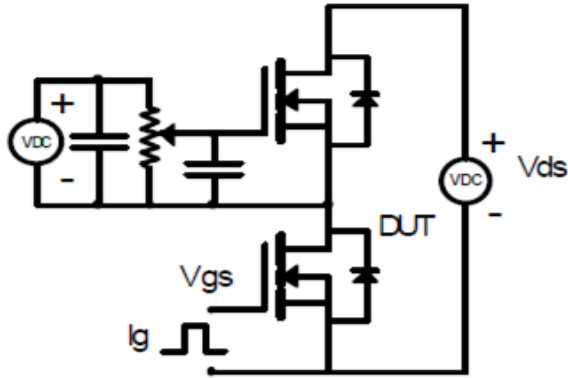
# PTF2N65

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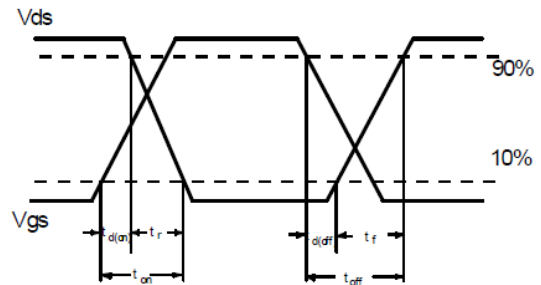
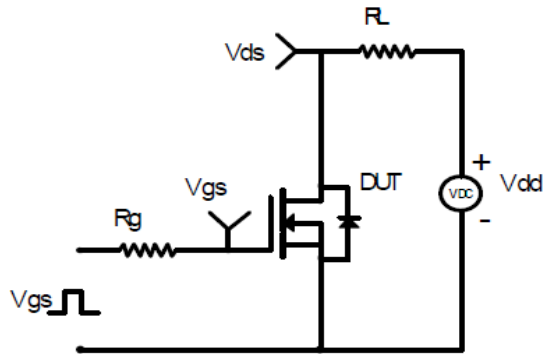


Test Circuit and Waveform

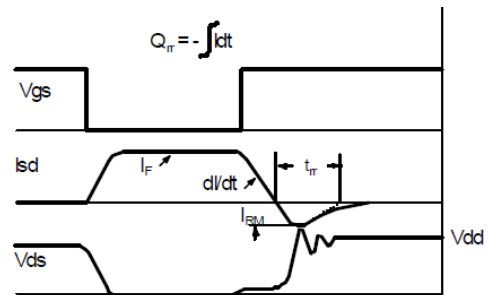
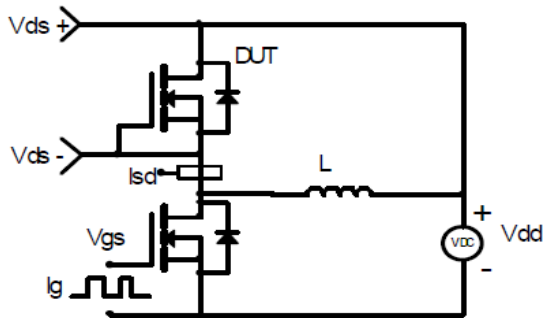
Gate Charge Test Circuit and Waveform



Switching time test circuit and waveform



Reverse Recovery Test Circuit and Waveform



Avalanche Test Circuit and Waveform

