芯鼎盛®

TX50N06

N channel 60V MOSFET

Description

The TX50N06 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on-state resistance.These devices are particularly suited for low voltage application.

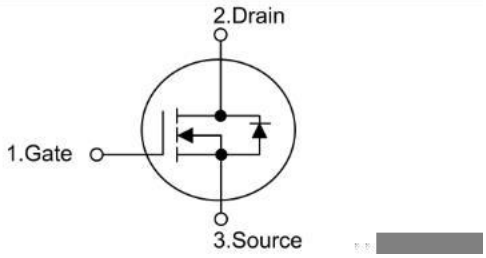
Features

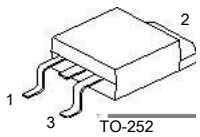
V_{DS}	60V
$R_{DS(on)}$Max.	20mΩ
I_D	50A

- High density cell design for ultra low $R_{DS(on)}$
- Excellent package for good heat dissipation

Pin configuration

Order Number	Package
TX50N06	TO-252





Maximum Ratings (Tc = 25℃ unless otherwise noted*)

Parameter		Symbol	Ratings	Units
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Tc=25℃	I_D	50*	A
	Tc=100℃		35.4*	A
Pulsed Drain Current		I_{DM}	90	A
Power Dissipation	Tc=25℃	P_D	85	W
	Derate above 25℃		0.3	
Single pulse avalanche energy（note 1）		E_{AS}	245	
Operating Junction and Storage Temperature Range		T_J,Tstg	-55~+175	℃

* Dran current limited by maximum junction temperature.

1：EAS condition:L=0.5mH, V_{DD}=30V, R_G=25Ω,T_J=25℃.

Thermal Characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ.	RthCS	0.5	℃/W
Thermal resistance junction to case.	RthJC	3.3	℃/W
Thermal resistance junction to ambient.	RthJA	110	℃/W

Electrical characteristics (TA =25℃ Unless Otherwise Specified)

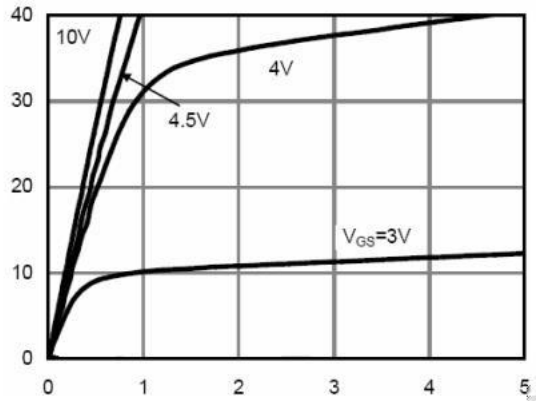
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	—	—	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.4	—	2.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V	—	—	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	—	—	1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=20A	—	14	20	mΩ
V_{SD}	Diode Forward Voltage	I_S=20A, V_{GS}=0V	—	—	1.2	V
DYNAMIC						
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_D=20A	—	50	—	nC
Q_{gs}	Gate-Source Charge		—	6	—	
Q_{gd}	Gate-Drain Charge		—	15	—	
C_{iss}	Input Capacitance	V_{DS}=30V, V_{GS}=0V, f=1MHz	—	2050	—	pF
C_{oss}	Output Capacitance		—	158	—	
C_{rss}	Reverse Transfer Capacitance		—	120	—	
$t_{d(on)}$	Turn-On Delay Time	V_{DD} =30V, R_G=3Ω R_L=6.7Ω,V_{GS}=10V,	—	7..4	—	ns
t_r	Turn-On Rise Time		—	5.1	—	
$t_{d(off)}$	Turn-Off Delay Time		—	28.2	—	
t_f	Turn-Off Fall Time		—	5.5	—	
t_{rr}	Reverse Recovery Time	TJ = 25°C, IF =20A di/dt = 100A/μs	—	28	—	nS
Q_{rr}	Reverse Recovery Charge		—	40	—	nC

Notes :a. Pulse test:pulse width 300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

b. XDSSEMI reserves the right to improve product design,functions and reliability without notice.

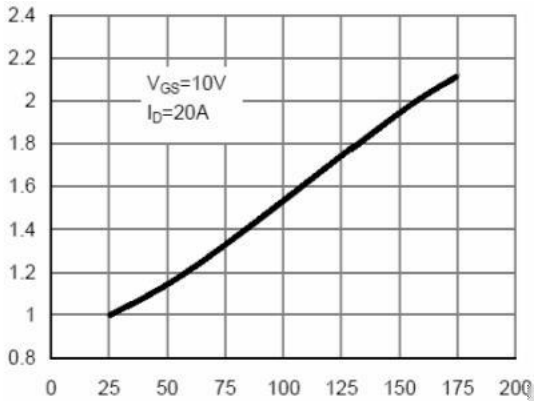
Typical Characteristics (TJ =25℃ Noted)

Output Characteristics



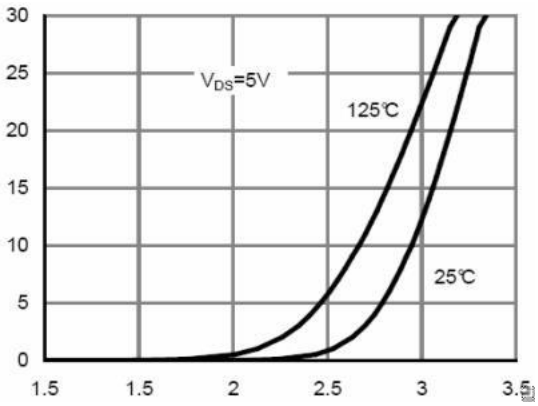
Drain-Source Voltage,VDS(V)

RDS(on) vs. JunctionTemperature



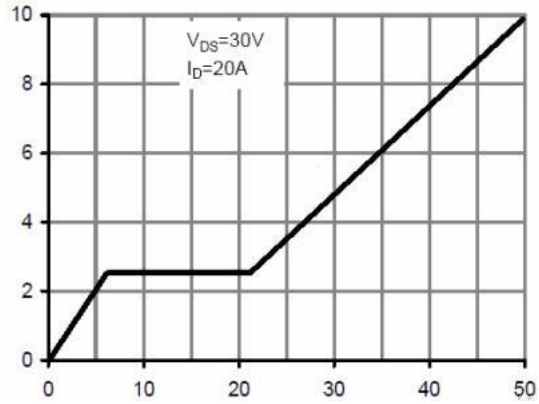
Junction Temperature,Tj(℃)

Transfer Characteristics



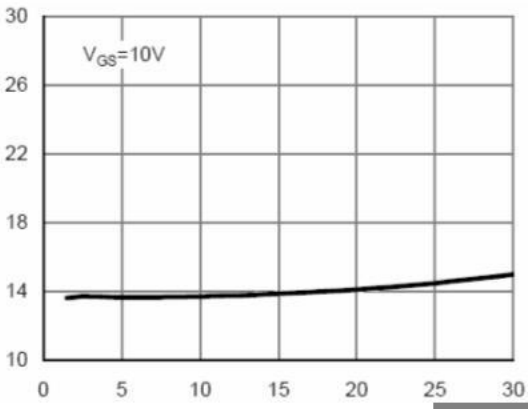
Gate-to-Source Voltage,VGS(V)

Gate Charge



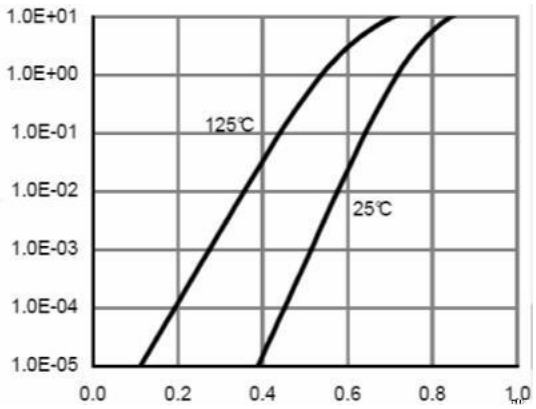
Gate Charge,Qg(nC)

RDS(on) vs. Drain Current



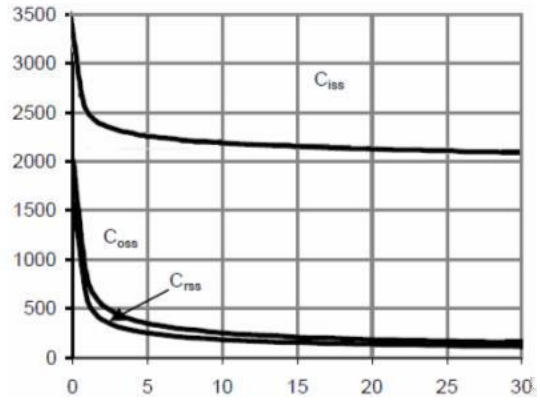
Drain Current,ID(A)

Source-to- Drain Diode Forward



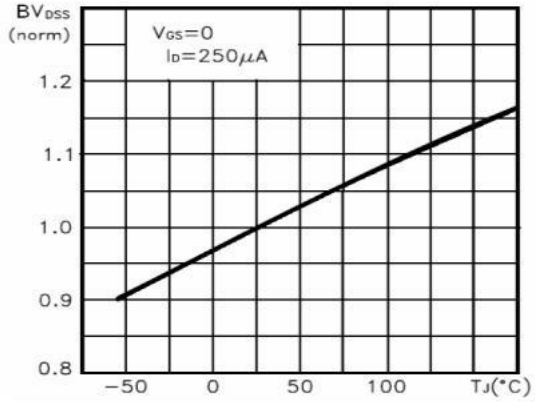
Source-Drai Voltage,VSD(V)

Capacitance vs. Drain Source Voltage



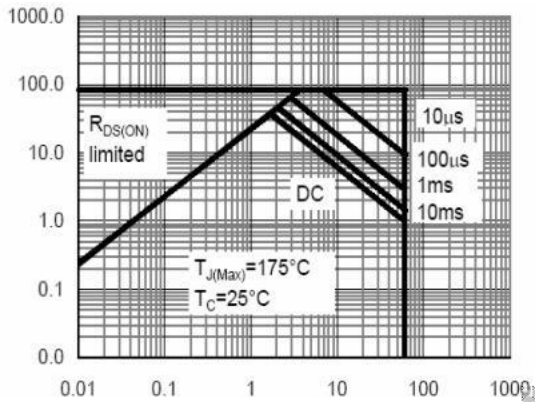
Drain Source Voltage VDS (V)

BVDSS vs. Junction Temperature



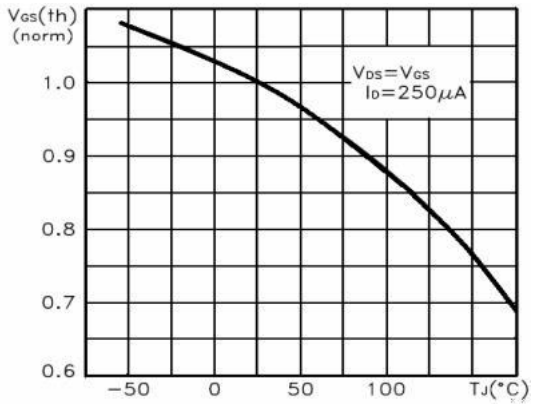
Junction Temperature,TJ(℃)

Safe Operation Area



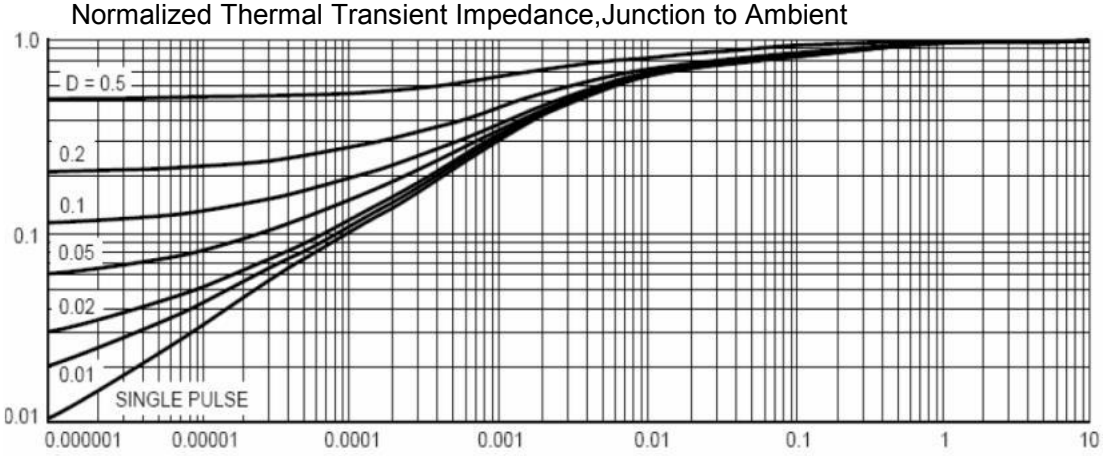
Drain-Source Voltage,VDS(V)

BVDSS vs Junction Temperature



Junction Temperature,TJ(℃)

Normalized Thermal Transient Impedance,Junction to Ambient



Square Wave Pulse Duration,t1(sec)

TO-252

Unit：mm