General Description

The WSF40P04 is the highest performance trench P-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSF40P04 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summery

BVDSS	RDSON	ID
-40V	32mΩ	-20A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

TO-252-3L(D-PAK) Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-20	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-16	A
I_{DM}	Pulsed Drain Current[2]	-28	A
I_{AR}	Avalanche Current	-22	A
EAR	Repetitive avalanche energy L=0.1mH	28	mJ
EAS	Single pulse avalanche energy L=0.3mH	55	mJ
P_D@T_C=25℃	Total Power Dissipation[4]	45	W
P_D@T_C=100℃	Total Power Dissipation[4]	20	W
P_D@T_A=25℃	Power Dissipation [A]	2.1	W
P_D@T_A=70℃	Power Dissipation [A]	1.5	W
T_J T_{STG}	Junction and Storage Temperature Range	-55 to 175	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	50	℃/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1] (t ≤10s)	---	25	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	2.5	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.0232	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-12A	---	32	42	mΩ
		V_{GS}=-4.5V , I_D=-8A	---	52	58	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1	-2	-3	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.6	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-32V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-32V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-12A	---	10	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	6.0	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-10V , I_D=-15A	---	20	---	nC
Q_{gs}	Gate-Source Charge		---	2.5	---	
Q_{gd}	Gate-Drain Charge		---	4.5	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-20V , V_{GS}=-10V , R_G=1.6Ω	---	5	---	ns
T_r	Rise Time		---	12	---	
$T_{d(off)}$	Turn-Off Delay Time		---	20	---	
T_f	Fall Time		---	4.5	---	
C_{iss}	Input Capacitance	V_{DS}=-25V , V_{GS}=0V , f=1MHz	---	840	---	pF
C_{oss}	Output Capacitance		---	92	---	
C_{rss}	Reverse Transfer Capacitance		---	60	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	-10	A
I_{SM}	Pulsed Source Current[2,6]		---	---	-20	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
t_{rr}	Reverse Recovery Time	IF=-12A,dI/dt=100A/μs,		20	---	nS
Q_{rr}	Reverse Recovery Charge		---	16	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AR}=-12A
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

Figure1. Power Dissipation

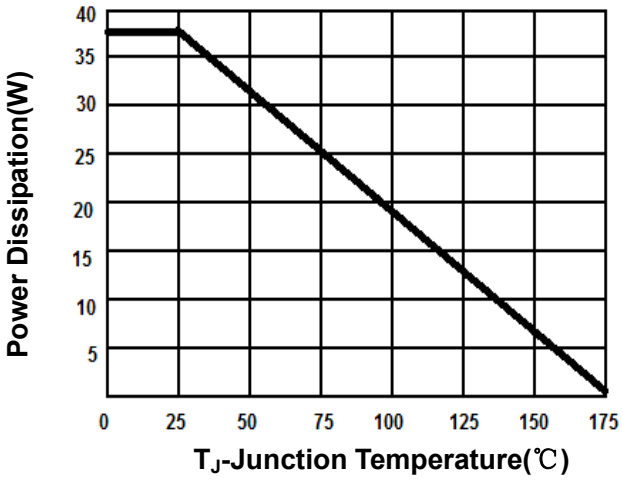


Figure2. Drain Current

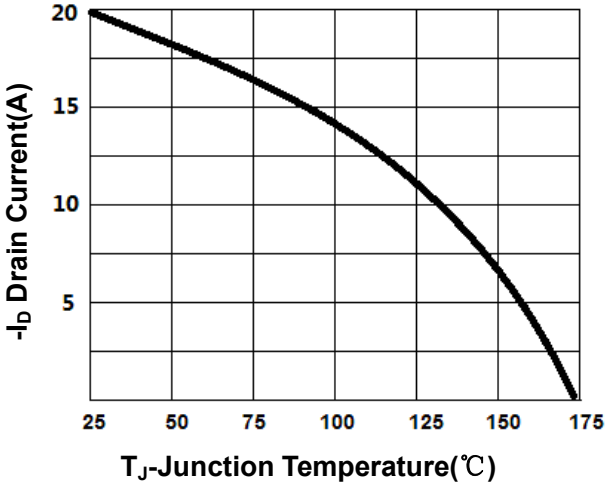


Figure3. Output Characteristics

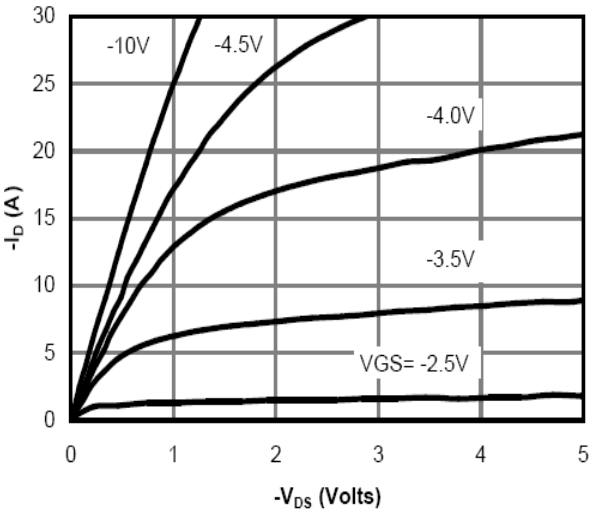
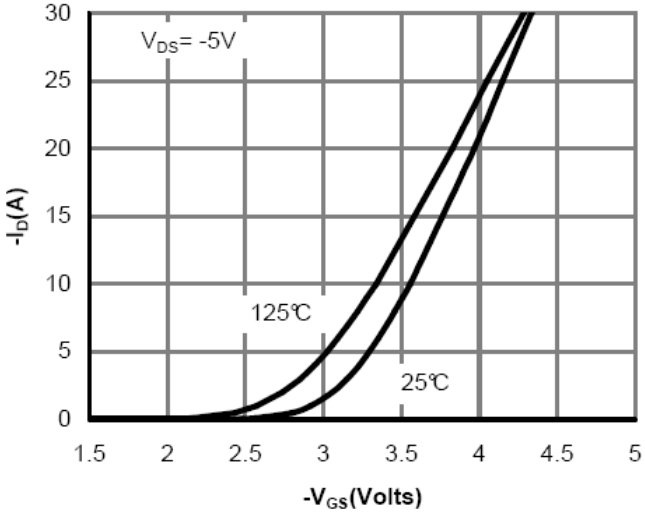


Figure4. Transfer Characteristics



Typical Characteristics

Figure5. Capacitance

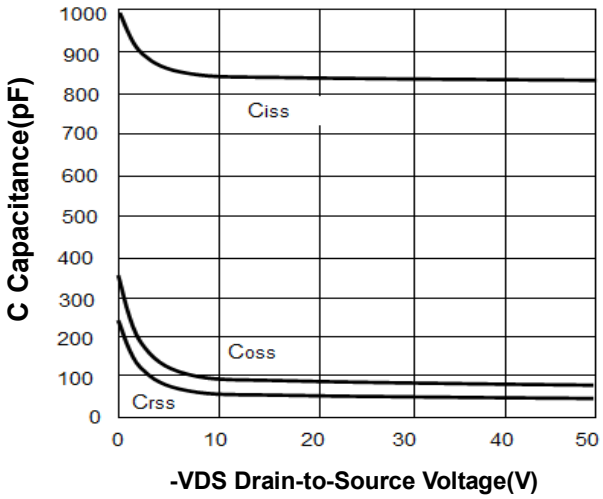


Figure6. $R_{DS(ON)}$ vs Junction Temperature

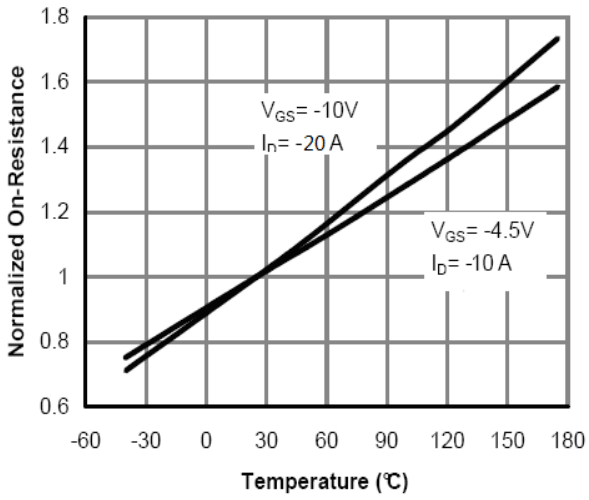


Figure7. $V_{GS(th)}$ vs Junction Temperature

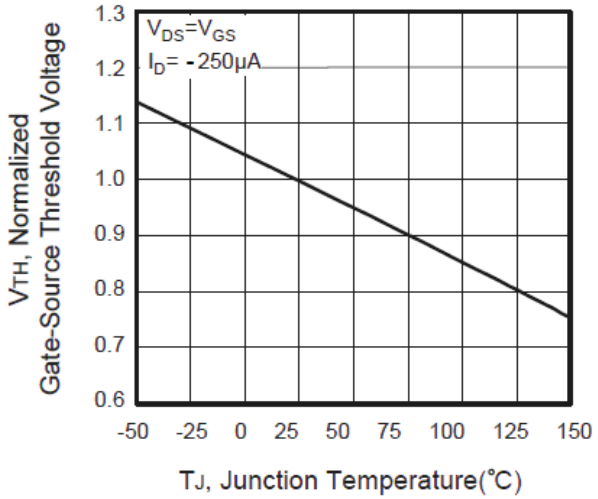
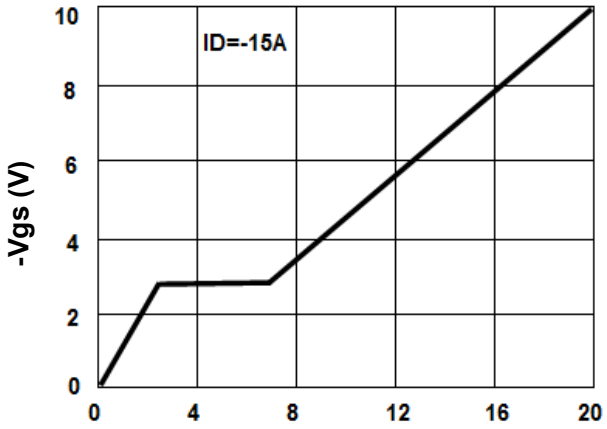
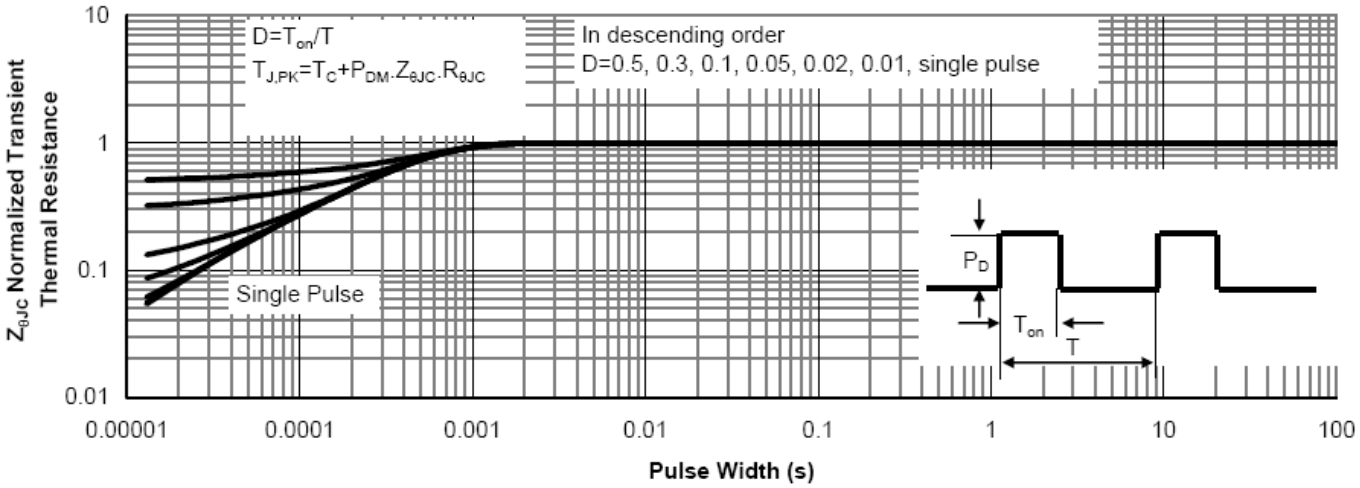


Figure8. Gate Charge Waveforms

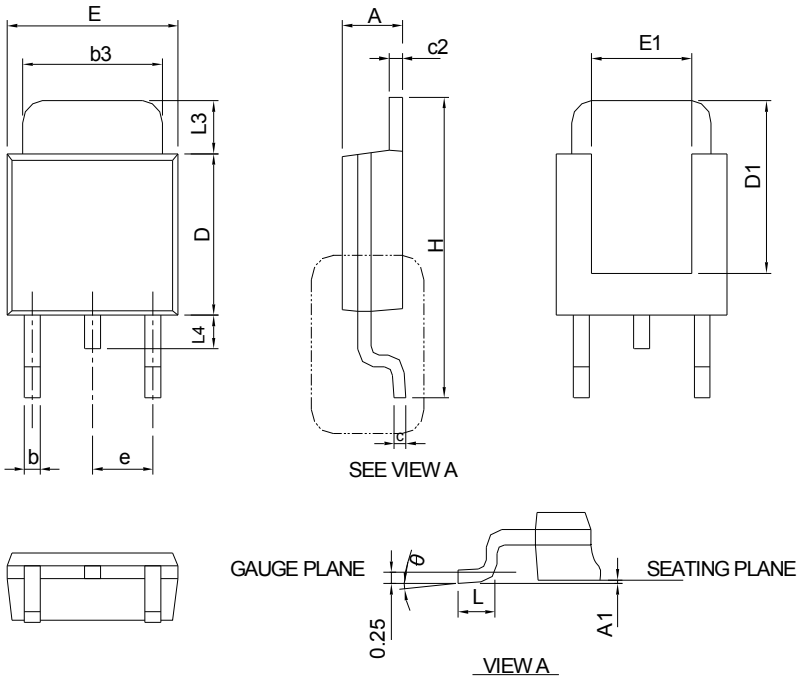


Typical Characteristics

Figure9. Normalized Maximum Transient Thermal Impedance



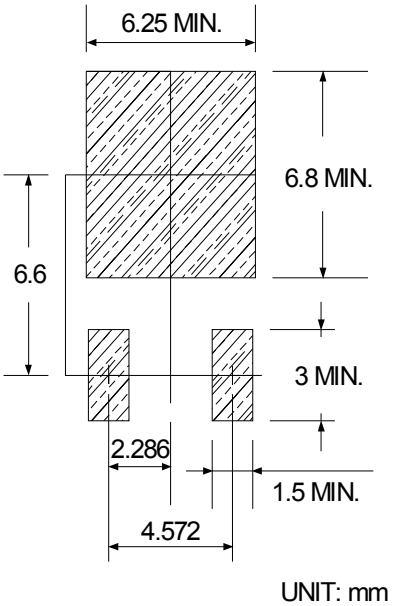
D-Pak (TO-252AA) (TO-252) (TO-252-3L) Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	TO-252-3L			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	-	0.13	-	0.005
b	0.50	0.89	0.020	0.035
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	0.90	1.78	0.035	0.070
L3	0.89	2.03	0.035	0.080
L4	-	1.02	-	0.040
θ	0°	8°	0°	8°

Note : Follow JEDEC TO-252 .

RECOMMENDED LAND PATTERN



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