

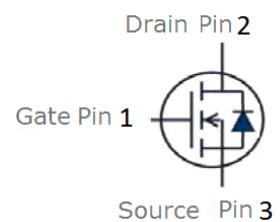
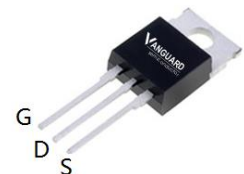
Features

- N-Channel, 5V Logic Level Control
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- VitoMOS[®] Technology
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VST007N07MS	TO-220AB	007N07M	50pcs/Tube

V_{DS}	80	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	8	m Ω
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	9	m Ω
I_D	80	A

TO-220AB


Maximum ratings, at $T_A=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	80	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C=25\text{ }^\circ\text{C}$	80 A
I_D	Continuous drain current @ $V_{GS}=10\text{ V}$	$T_C=25\text{ }^\circ\text{C}$	80 A
		$T_C=100\text{ }^\circ\text{C}$	57 A
I_{DM}	Pulse drain current tested ①	$T_C=25\text{ }^\circ\text{C}$	320 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{ V}$	$T_A=25\text{ }^\circ\text{C}$	10 A
		$T_A=70\text{ }^\circ\text{C}$	8 A
EAS	Avalanche energy, single pulsed ②	132	mJ
P_D	Maximum power dissipation	$T_C=25\text{ }^\circ\text{C}$	120 W
P_{DSM}	Maximum power dissipation ③	$T_A=25\text{ }^\circ\text{C}$	2 W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$



Typical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	80	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =80V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =80V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	--	2.3	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =40A	--	8	11	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =20A	--	9	12	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	3500	4420	5300	pF
C _{oss}	Output Capacitance		100	225	350	pF
C _{rss}	Reverse Transfer Capacitance		90	195	300	pF
R _g	Gate Resistance	f=1MHz	--	3.4	--	Ω
Q _g	Total Gate Charge	V _{DS} =40V, I _D =40A, V _{GS} =10V	--	71	--	nC
Q _{gs}	Gate-Source Charge		--	22	--	nC
Q _{gd}	Gate-Drain Charge		--	24	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =40V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	23	--	ns
t _r	Turn-on Rise Time		--	17	--	ns
t _{d(off)}	Turn-Off Delay Time		--	40	--	ns
t _f	Turn-Off Fall Time		--	14	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =40A, V _{GS} =0V	--	29	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=500A/μs	--	131	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.



Typical Characteristics

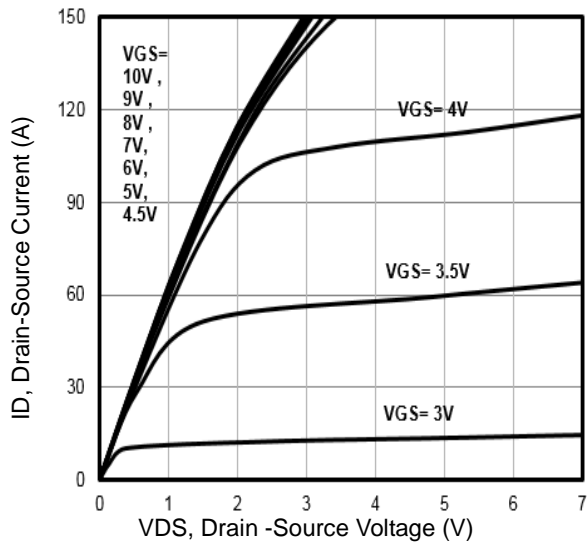


Fig1. Typical Output Characteristics

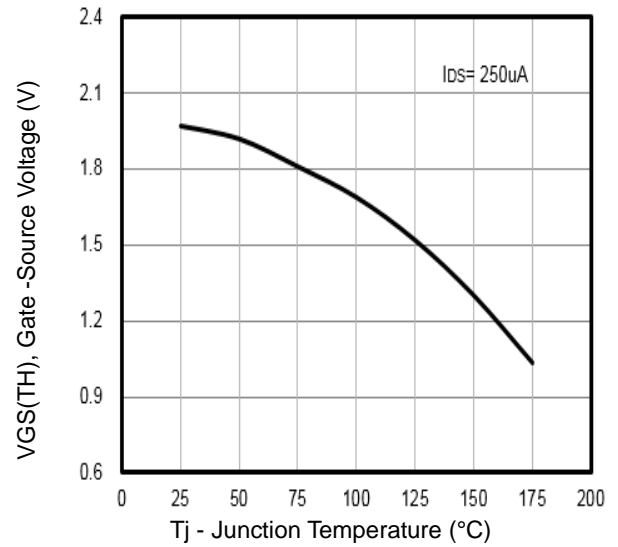


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

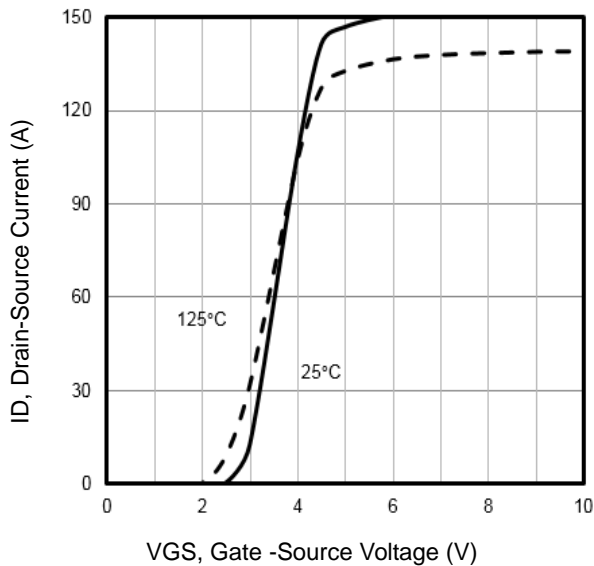


Fig3. Typical Transfer Characteristics

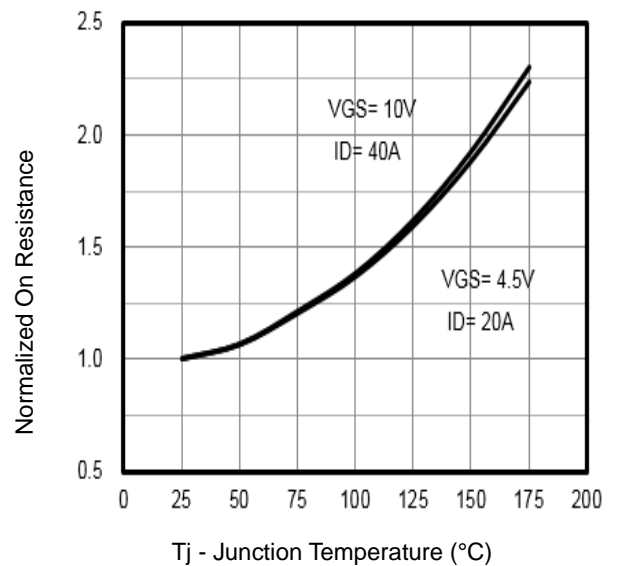


Fig4. Normalized On-Resistance Vs. Temperature

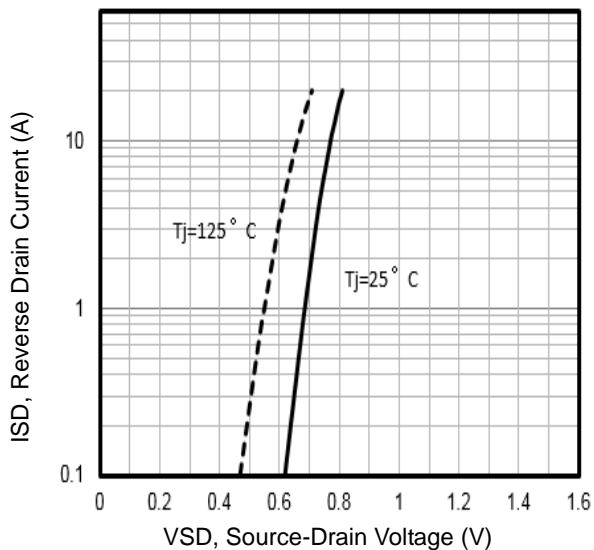


Fig5. Typical Source-Drain Diode Forward Voltage

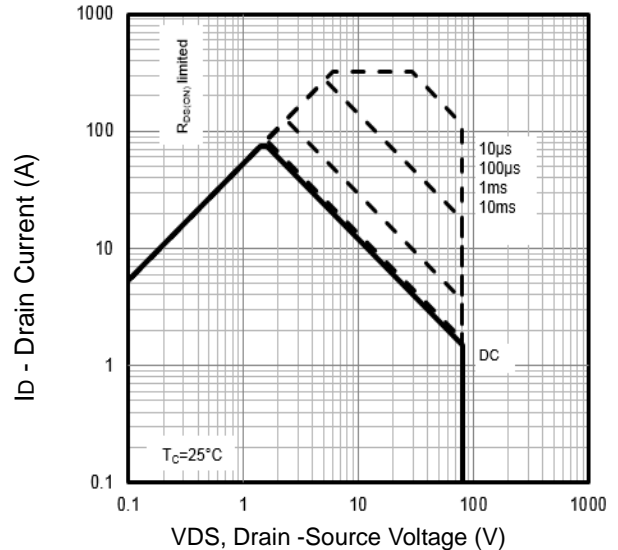


Fig6. Maximum Safe Operating Area

Typical Characteristics

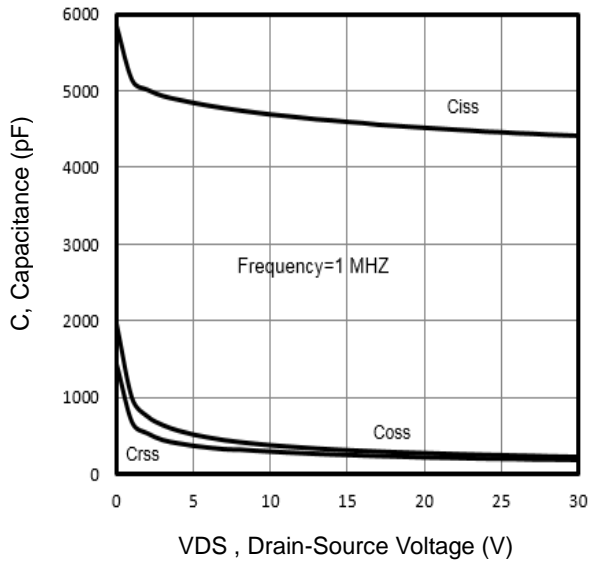


Fig7. Typical Capacitance Vs.Drain-Source Voltage

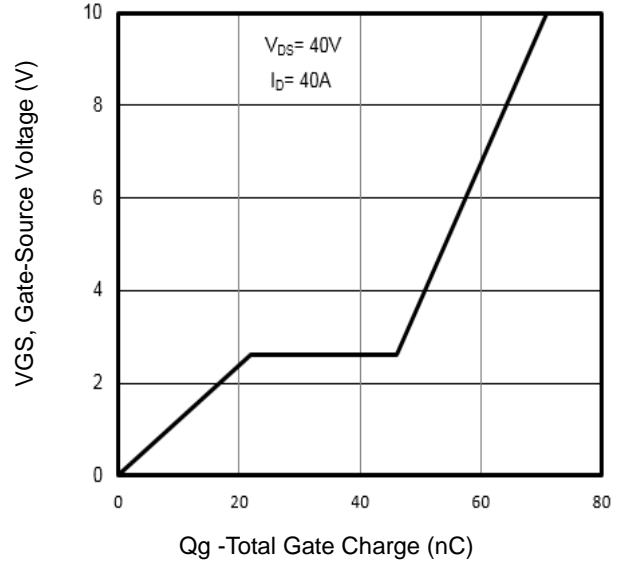


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

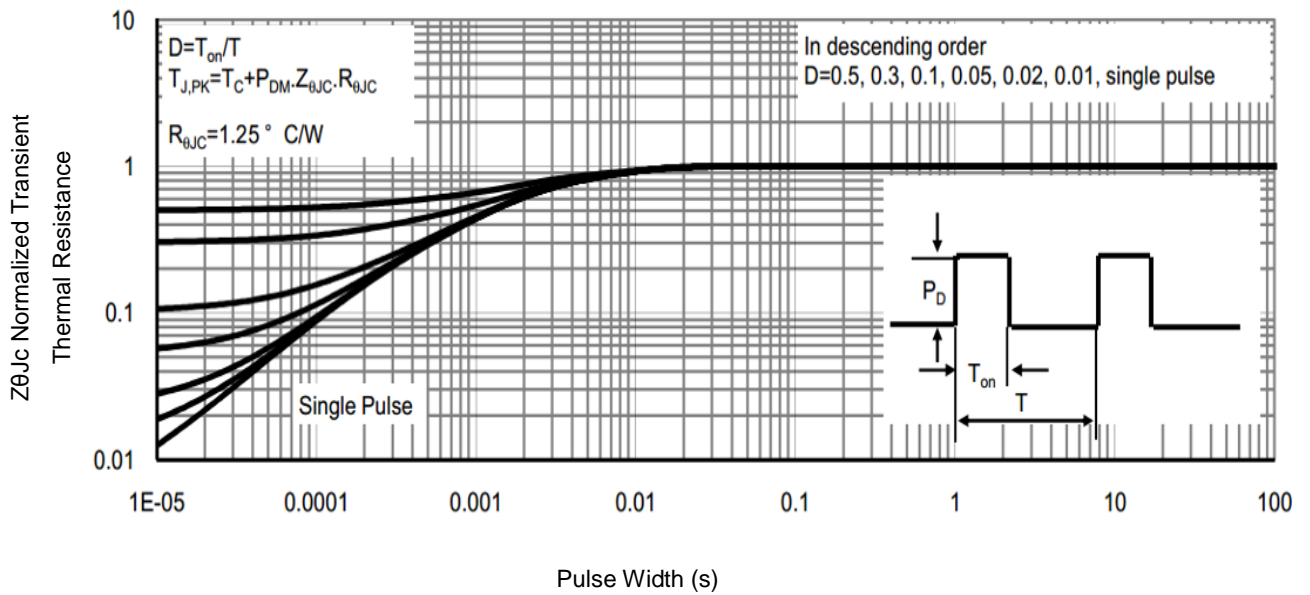


Fig9. Normalized Maximum Transient Thermal Impedance

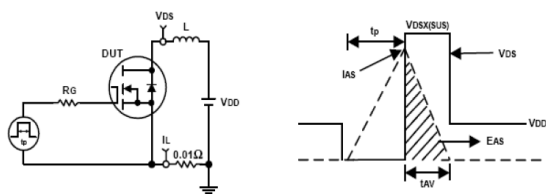


Fig10. Unclamped Inductive Test Circuit and waveforms

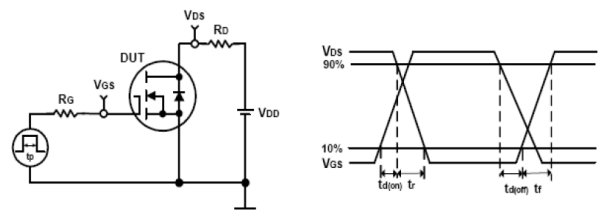
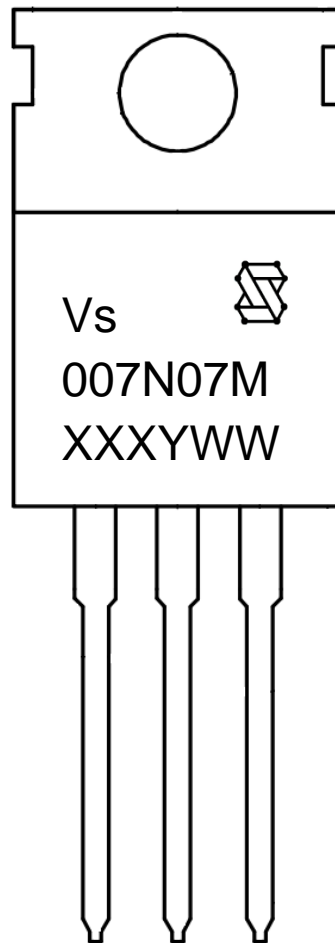


Fig11. Switching Time Test Circuit and waveforms



Marking Information



1st line: Vanguard Code (Vs), Vanguard Logo

2nd line: Part Number (007N07M)

3rd line: Date code (XXXYWW)

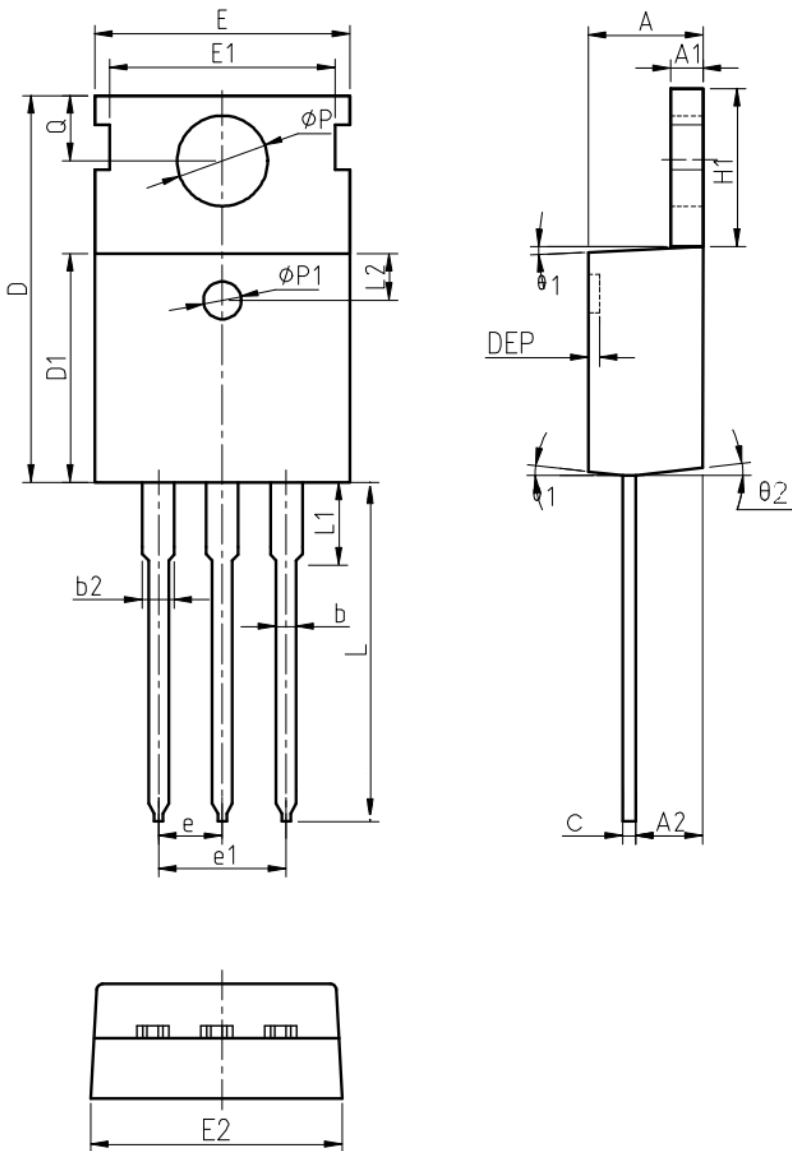
XXX: Wafer Lot Number

Y: Year Code, e.g. E means 2017

WW: Week Code



TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.32	1.50
c	0.45	0.50	0.61
D	15.30	15.65	15.90
D1	9.00	9.20	9.40
DEP	0.05	0.10	0.25
E	9.66	9.90	10.28
E1	-	8.70	-
E2	9.80	10.00	10.20
$\phi P1$	1.40	1.50	1.60
e	2.54 BSC		
e1	5.08 BSC		
H1	6.40	6.50	6.80
L	12.70	-	14.27
L1	-	-	3.95
L2	2.40	2.50	2.60
ϕP	3.53	3.60	3.70
Q	2.70	2.80	2.90
$\theta1$	5 °	7 °	9 °
$\theta2$	1 °	3 °	5 °

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Customer Service

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