4.5-V TO 16-V INPUT, HIGH CURRENT, SYNCHRONOUS STEP DOWN DUAL BUCK SWITCHER WITH INTEGRATED FET AND ONE USB SWITCH AND SVS

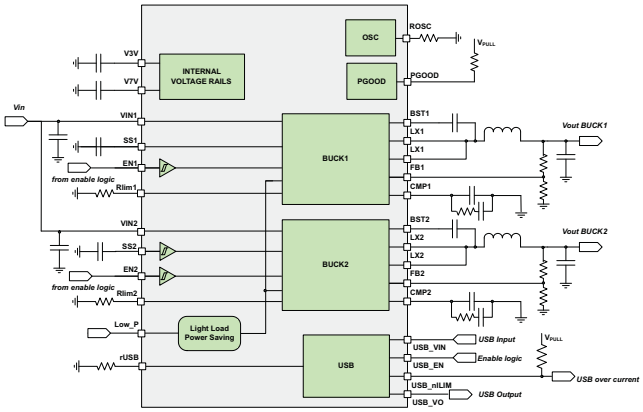
Check for Samples: TPS65252

FEATURES

- **Wide Input Supply Voltage Range (4.5 V - 16 V)**
- **Output Range 0.8 to ~V_{IN} - 1 V**
- **Fully Integrated Dual Buck, 3.5-A/2.5-A Maximum Current, 3-A/2-A Continuous Operation**
- **High Efficiency**
- **Switching Frequency: 300 kHz - 2.2 MHz Set By External Resistor**
- **External Enable/Sequencing Pins**
- **Adjustable Cycle-By-Cycle Current Limit Set By External Resistor**
- **Soft Start Pins**
- **Current Mode Control With Simple Compensation Circuit**
- **Power Good and Reset Generator**
- **Low Power Mode Set By External Signal**
- **One Current Adjustable USB Switch With Over Current Protection**
- **Supervisory Circuit**
- **QFN Package, 28-Pin 5 mm x 5 mm RHD**

APPLICATIONS

- **DTV**
- **DSL Modems**
- **Cable Modems**
- **Set Top Boxes**
- **Car DVD Players**
- **Home Gateway and Access Point Networks**
- **Wireless Routers**



DESCRIPTION/ORDERING INFORMATION

The TPS65252 features two synchronous wide input range high efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9- or 12-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and the input supply minus 1 V. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The COMP pin allows optimizing transient versus dc accuracy response with a simple RC compensation.

The switching frequency of the converters can be set with an external resistor connected to ROSC pin. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. The converters operate with 180° phase between them to minimize the input filter requirements.

TPS65252 also features a low power mode enabled by an external signal, which allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

The USB switch provides up to 1-A of current as required by downstream USB devices. When the output load exceeds the current-limit threshold selected with an external resistor or a short is present, the PMU limits the output current to a safe level by switching into a constant-current mode and pulling the over current logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to allow continuous non-interrupted operation the buck converters.

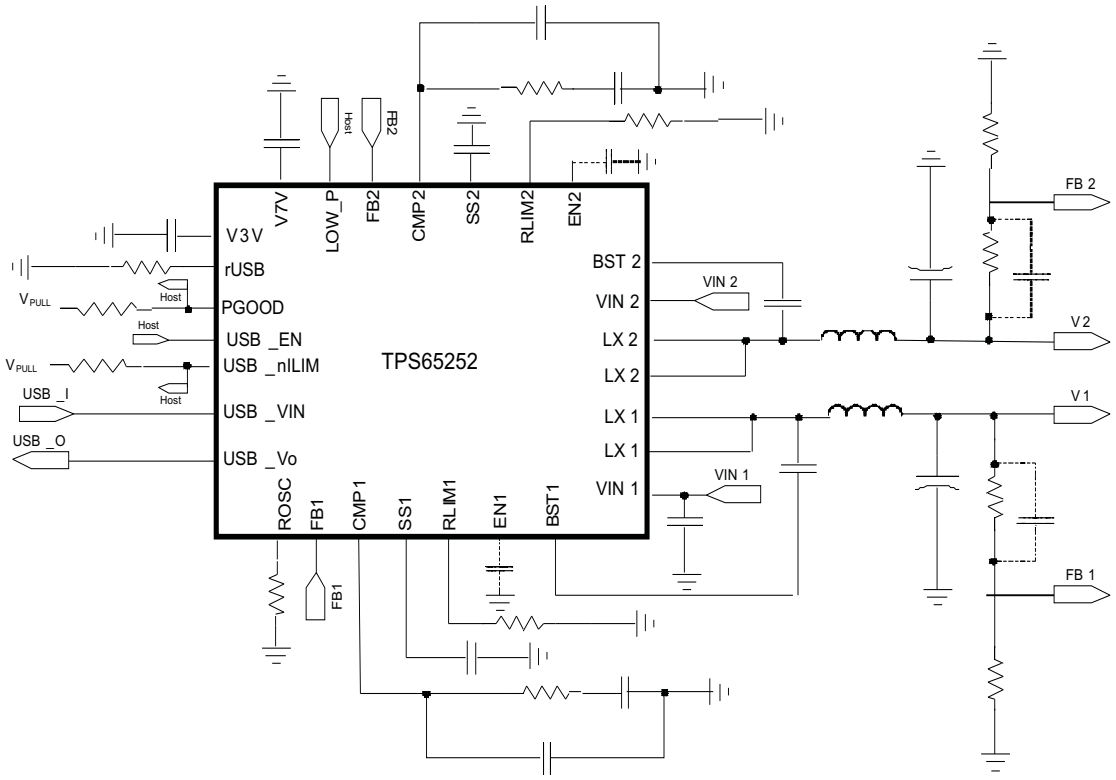
The TPS65252 features a supervisor circuit that monitors both converters and provides a PGOOD signal (End of Reset) with a 256-ms timer.

TPS65252 is packaged in a small, thermally efficient 28-pin QFN package.

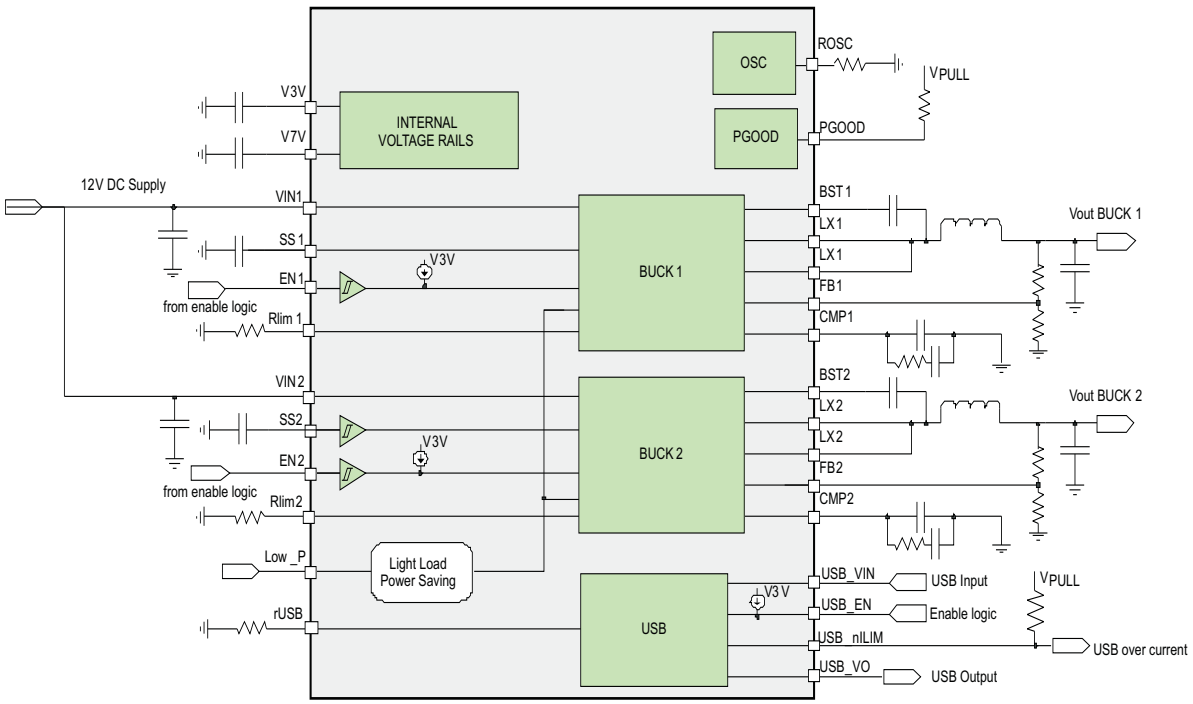
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM

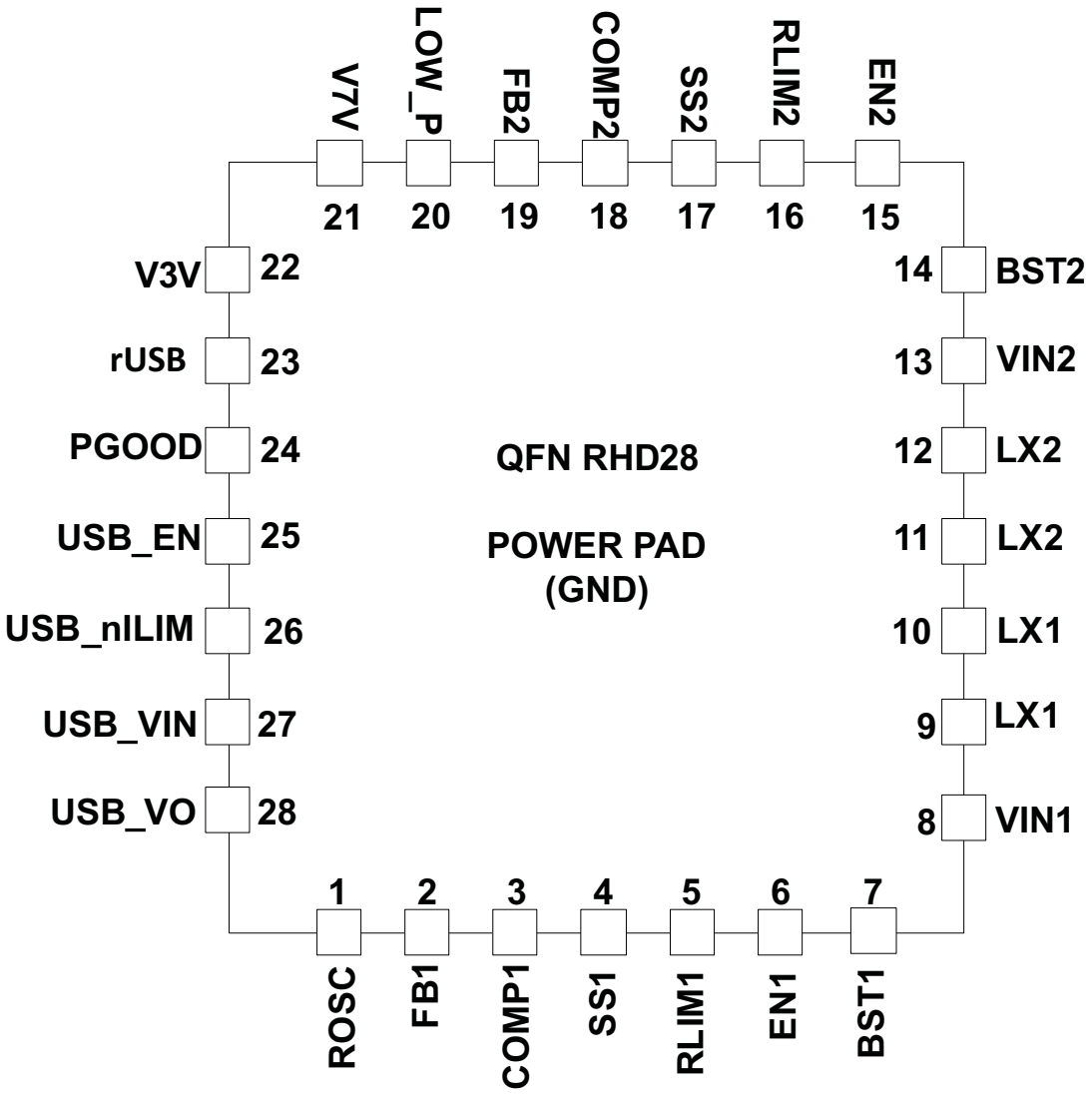


ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	28-pin (QFN) - RHD	TPS65252RHD	TPS65252

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN OUT



TERMINAL FUNCTIONS

NAME	I/O	NO.	DESCRIPTION
ROSC	I	1	Oscillator set. This resistor sets the frequency of internal autonomous clock.
FB1	I	2	Feedback pin for buck 1. Connect a divider set to 0.8V from the output of the converter to ground.
COMP1	O	3	Compensation pin for buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	I	4	Soft start pin for buck 1. Fit a small ceramic capacitor to this pin to set the converter soft start time.
RLIM1	I	5	Current limit setting pin for buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	I	6	Enable pin for buck 1. A high signal on this pin enables the regulator buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	I	7	Bootstrap capacitor for buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	I	8	Input supply for buck 1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	O	9	Switching node for buck 1
LX1		10	
LX2	O	11	Switching node for buck 2
LX2		12	
VIN2	I	13	Input supply for buck 2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	I	14	Bootstrap capacitor for buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	I	15	Enable pin for buck 2. A high signal on this pin enables the regulator buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	I	16	Current limit setting pin for buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	I	17	Soft start pin for buck 2. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP2	O	18	Compensation pin for buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB2	I	19	Feedback pin for buck 2. Connect a divider set to 0.8V from the output of the converter to ground.
LOW_P	I	20	Low power operation mode (active high) input for TPS65252
V7V	O	21	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
V3V	O	22	Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.
rUSB	I	23	USB current limit setting resistor. Fit a resistor from this pin to ground to set the peak current limit on the USB switch.
PGOOD		24	Open drain power good output
USB_EN	I	25	Enable input, logic high turns on the USB
USB_nILIM	O	26	Over current open-drain output, active low
USB_VIN	I	27	USB input supply
USB_VO	O	28	USB switch output
PAD			Power pad. Connect it to ground

ABSOLUTE MAXIMUM RATINGS (OPERATING IN A TYPICAL APPLICATION CIRCUIT) (1)

Over operating free-air temperature range and all voltages are with respect to GND (unless otherwise noted).

	Voltage range at VIN1,VIN2, LX1, LX2	–0.3 to 18	V
	Voltage range at LX1, LX2 (maximum withstand voltage transient < 20 ns)	–3 to 18	V
	Voltage at BST1, BST2, referenced to Lx pin	–0.3 to 7	V
	Voltage at V7V, COMP1, COMP2, USB_VIN, USB_VO	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, EN1,EN2, SS1, SS2, FB1, FB2, ROSC, LOW_P, USB_EN, USB_nILIM, PGOOD, rUSB	–0.3 to 3.6	V
	Voltage at GND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		16	V
T_A	Operating ambient temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)
RHD	34 (simulated)	2.9	2

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x .6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input Voltage range		4.5		16	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		0.3		mA
IDD_Q	Quiescent, low power disabled (Lo)	Converters enabled, no load		10		mA
$IDD_{Q\_LOW\_P}$	Quiescent, low power enabled (Hi)	Converters enabled, no load		0.5		mA
$UVLO_{VIN}$	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V3p3	Internal biasing supply			3.3		V
I_{3V}	Biasing supply output current	V_{IN} = 12 V			10	mA
V7V	Internal biasing supply			6.25		V
I_{7V}	Biasing supply output current	V_{IN} = 12 V			10	mA
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT START, SWITCHING FREQUENCY AND LOW POWER MODE)						
V_{IH}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	1.55		1.82	V
	Enable high level	External GPIO, V_{ENX} rising	0.66 x V3p3			
V_{IL}	Enable threshold Low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling	0.98		1.24	V
	Enable low level	External GPIO, V_{ENX} falling			0.33 x V3p3	
ICH_{EN}	Pull up current enable pin			1.1		µA
R_{EN_DIS}	Enable discharge resistor		-25%	2.1	25%	kΩ
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor	Depending on set frequency	50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
VIH_{LOW_P}	Low power mode threshold high	V3p3 = 3.3 V	1.55		1.82	V
VIL_{LOW_P}	Low power mode threshold Low	V3p3 = 3.3 V	0.98		1.24	V
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V, T_J = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 V to 16 V	-2%	0.8	2%	
I_{FB}	Feedback leakage current				50	nA
t_{ON_MIN}	Minimum on time (current sense blanking)			80	120	ns
MOSFET (BUCK 1)						
H.S. Switch	Turn-On resistance high side FET on CH1	T_J = 25°C, V_{IN} = 12 V		95		mΩ
L.S. Switch	Turn-On resistance low side FET on CH1	T_J = 25°C, V_{IN} = 12 V		50		mΩ
MOSFET (BUCK 2)						
H.S. Switch	Turn-On resistance high side FET on CH2	T_J = 25°C, V_{IN} = 12 V		120		mΩ
L.S. Switch	Turn-On resistance low side FET on CH2	T_J = 25°C, V_{IN} = 12 V		80		mΩ

ELECTRICAL CHARACTERISTICS (continued)

T_J = -40°C to 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA		130		µmhos
gm_{PS}	COMP to ILX g_M	ILX = 0.5 A		10		A/V
USB						
VIN_{USB}	USB input voltage		3.3		6	V
R_{DS_USB}	Static drain-source on-state resistance	USB_VIN = 5 V and Io_USB = 0.5 A		120		mΩ
V_{IH}	USB_EN high level input voltage	V3p3 = 3.2 V - 3.4 V	1.55			V
V_{IL}	USB_EN low level input voltage	V3p3 = 3.2 V - 3.4 V			1.3	V
$I_{CS\_USB\_1}$	USB current limit when 154 kΩ is connected from rUSB to GND	Increasing USB_VO current di/dt < 1A/s	0.42	0.55	0.68	A
$I_{CS\_USB\_2}$	USB current limit when 76.8 kΩ is connected from rUSB to GND	Increasing USB_VO current di/dt < 1A/s	0.84	1.10	1.36	A
$K_{OVERCURRENT}$	Overcurrent detection factor Ratio of I_{LIM_START}/ I_{CS_USB}	Increasing USB_VO current di/dt < 1A/s	1.8	2.1	2.4	
V_{USB_ILIM}	USB ILIM output voltage low	I_{USB_ILIM} = 3 mA			0.4	V
T_{CS_USB}	USB over current fault deglitch	Fault assertion or de-assertion due to OCP		6		ms
T_{USB_TRIP}	USB thermal trip point	Rising temperature		130		°C
$V_{USB\_Nilim\_LO}$	Usb switch alarm low level	Pulled to 3V3 with 100-kΩ resistors			0.3	V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling (device will be disabled after t_{ON_HICCUP})		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglitch time (both edges)			11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time before re-start is attempted	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		20		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side fet will be forced off)		109		%
		Output falling (high side fet will be allowed to switch)		107		
t_{RP}	Minimum reset period	Measured after minimum reset period of all bucks power-up successfully		256		ms
$PGOOD_{LO}$	Power good low level	Pulled to 3V3 with 100-kΩ resistors			0.3	V
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch		100		120	µs
CURRENT LIMIT PROTECTION						
$RLIM_x$	Limit resistance range		75		300	kΩ
$ILIM_1$	Buck 1 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 17	1.1		5.2	A
$ILIM_2$	Buck 2 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 18	0.9		4.5	A

TYPICAL CHARACTERISTICS

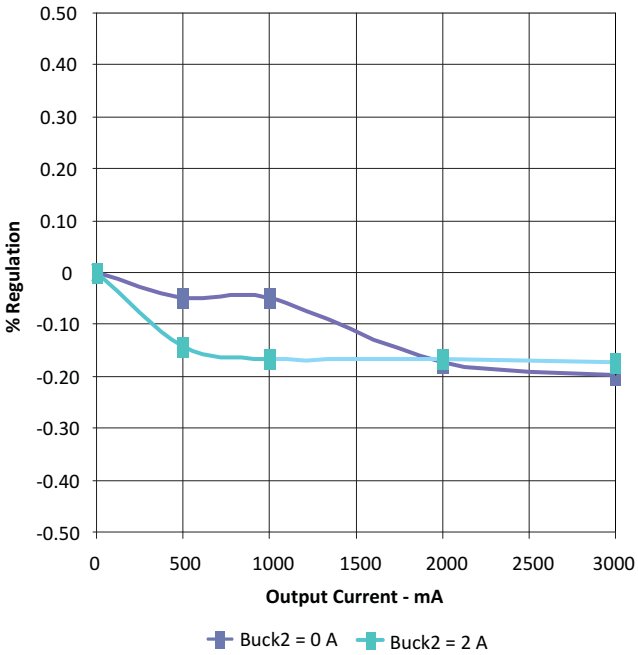


Figure 1. Buck1 Load Regulation, V_O = 1.2 V

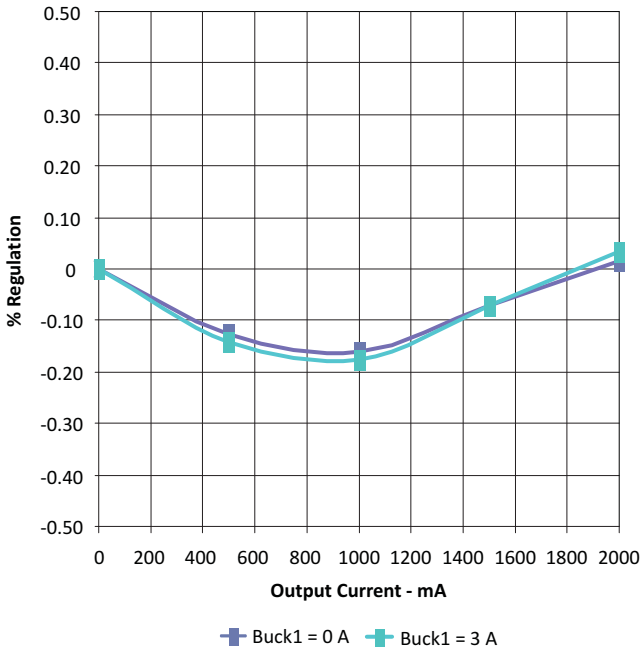


Figure 2. Buck2 Load Regulation V_O = 1.8 V

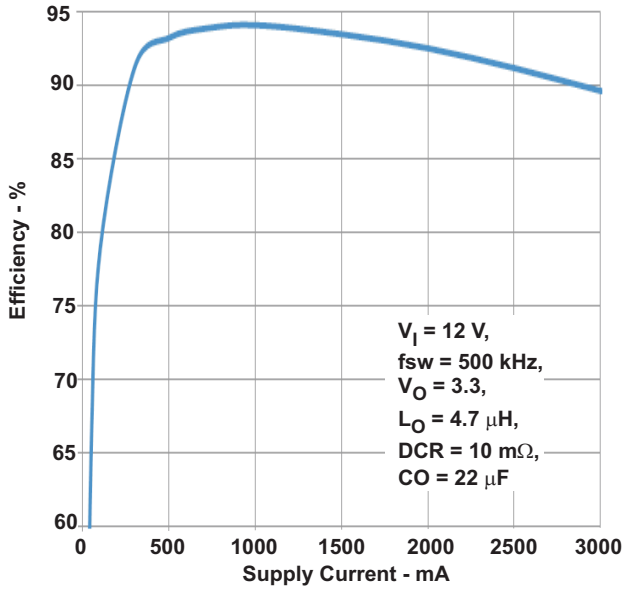


Figure 3. Buck 1 Efficiency, V_O = 3.3 V, V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

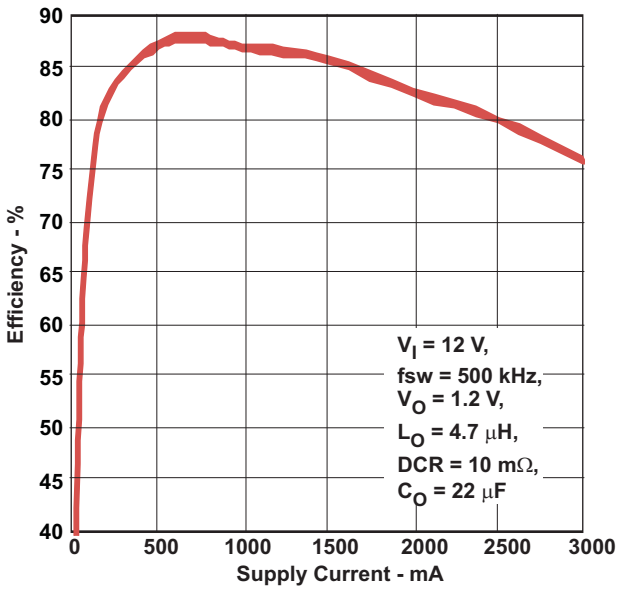


Figure 4. Buck 1 Efficiency, V_O = 1.2 V, V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

TYPICAL CHARACTERISTICS (continued)

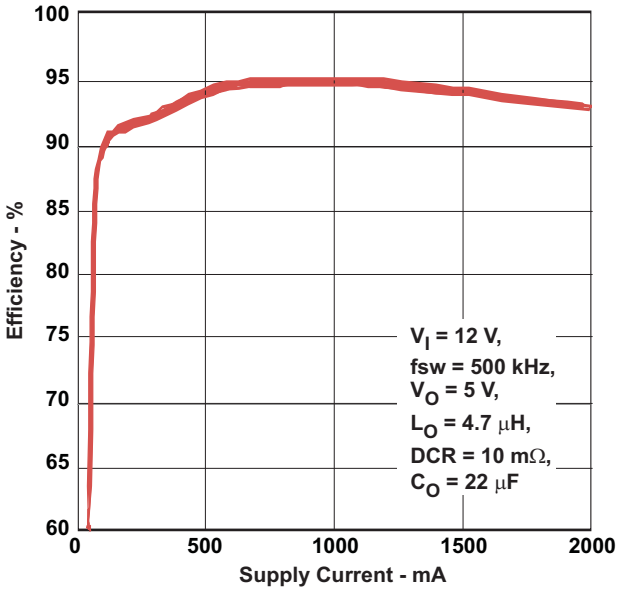


Figure 5. Buck 2 Efficiency, V_O = 5 V, V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

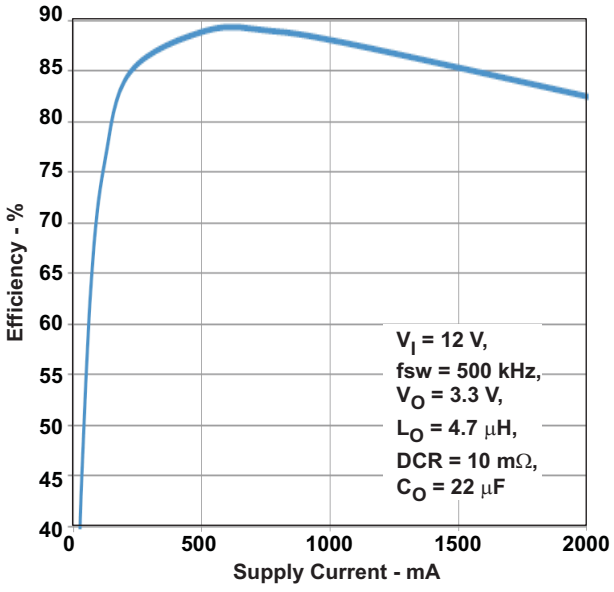


Figure 6. Buck 2 Efficiency, V_O = 3.3 V, V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

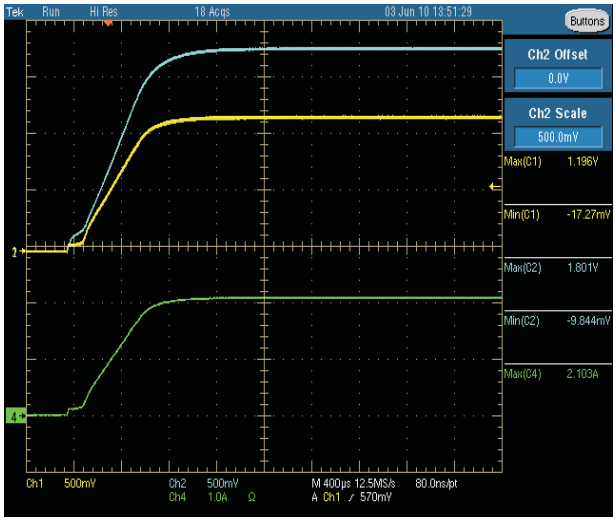


Figure 7. Soft Start for Buck 1 (Yellow Trace) 1.2 V, 3 A and Buck 2 (Blue Trace) 1.8 V, 2 A, V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

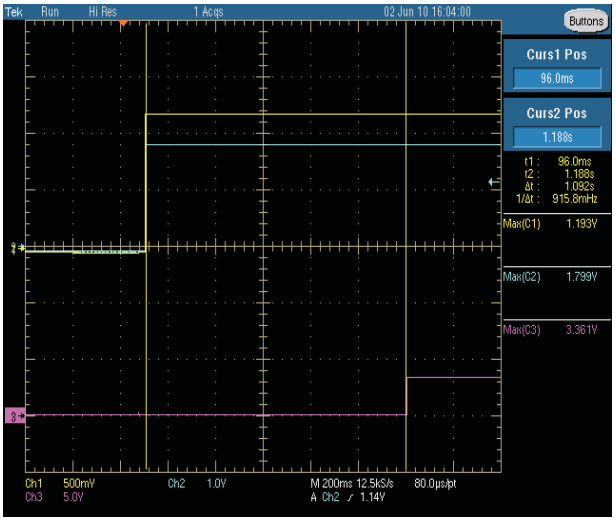


Figure 8. Power Up and PGOOD (From Top to Bottom, Buck2 = 1.8 V, Buck1 = 1.2 V, PGOOD) V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

TYPICAL CHARACTERISTICS (continued)

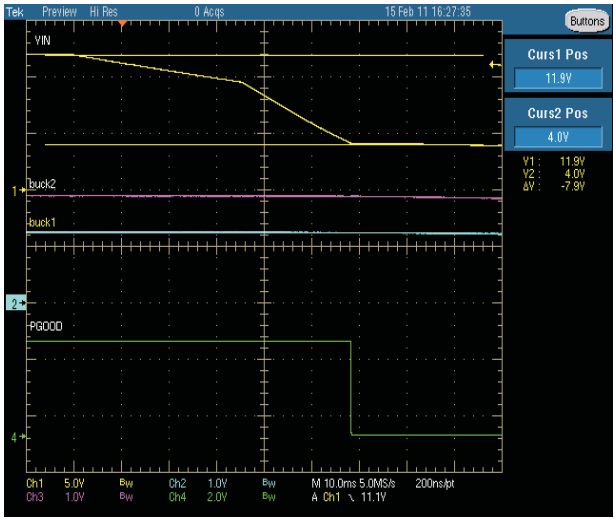


Figure 9. Power Down Behavior (From Top to Bottom V_{IN}, Buck2 = 1.8 V, Buck1 = 1.2 V, PGOOD) V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

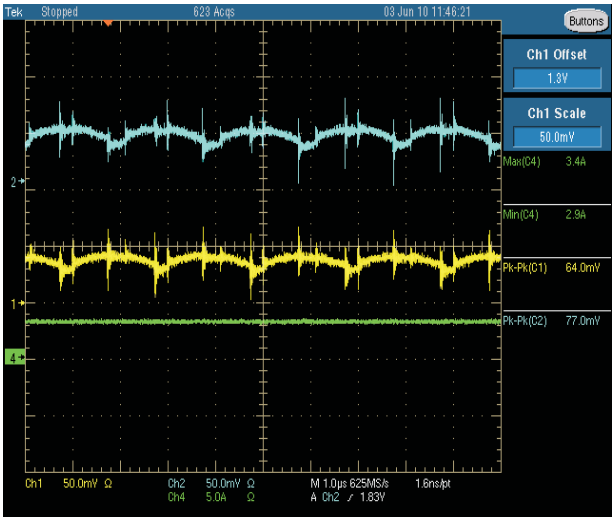


Figure 10. Ripple for Buck 1 (Yellow Trace) 1.2 V, 3 A and Buck 2 (Blue Trace) 1.8 V, 2 A, 50 mV per Division V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

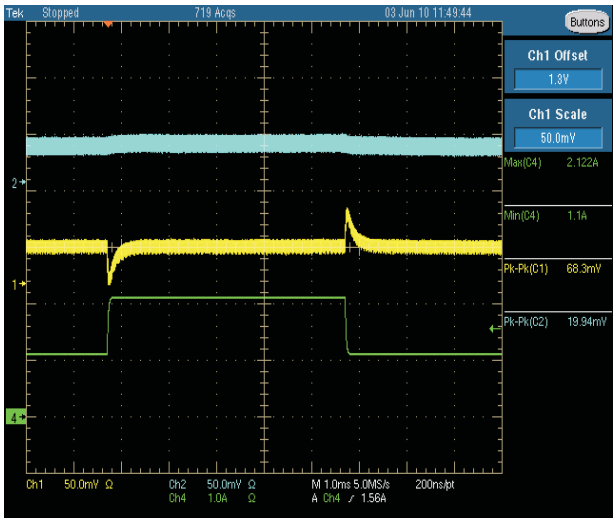


Figure 11. Buck 1 (Yellow Trace) Dynamic Response 1-A - 2-A Step, 50 mV/div. Buck 2 (Blue Trace), 50 mV/div V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

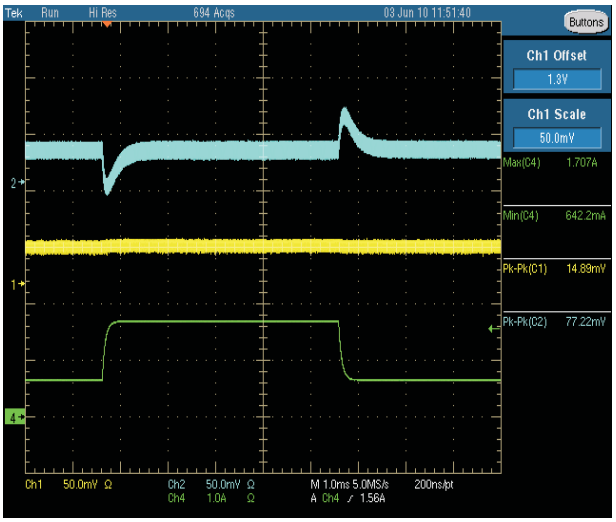


Figure 12. Buck 2 (Blue Trace) Dynamic Response 0.5-A - 1.5-A Step, 50 mV/div. Buck 1 (Yellow Trace), 50 mV/div V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 4.7 µH, DCR = 10 mΩ, C_O = 22 µF

OVERVIEW

TPS65252 is a power management IC with two step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65252 can support 4.5-V to 16-V input supply, high load current, 300-kHz to 2.2-MHz clocking. The buck converters have an optional PFM mode, which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 2.2 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. Input ripple is reduced by 180° out-of-phase operation between buck 1 and buck 2.

Both buck converters have peak current mode control which simplifies external frequency compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

Each buck converter has an individual current limit, which can be set up by a resistor to ground from the RLIM pin. The adjustable current limiting enables high efficiency design with smaller and less expensive inductors.

The device has two built-in LDO regulators. During a standby mode, the 3.3-V LDO and the 6.5-V LDO can be used to drive MCU and other active loads. By this, the system is able to turn off the two buck converters and improve the standby efficiency.

The device has a power good comparator monitoring the output voltage. Each converter has its own soft start and enable pins, which provide independent control and programmable soft start.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from ROSC to ground. Figure 13 shows the required resistance for a given switching frequency.

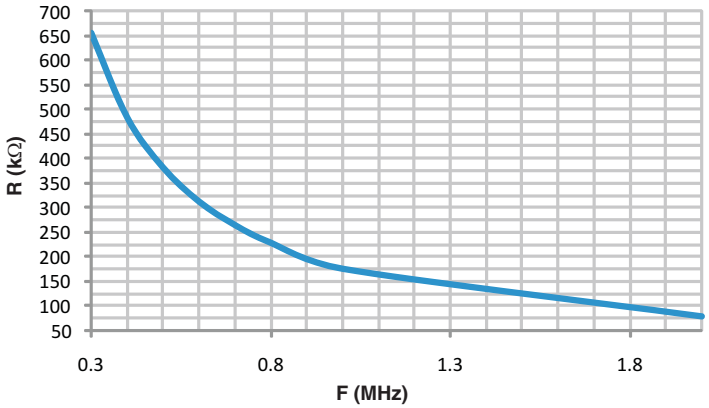


Figure 13. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \bullet f^{-1.122} \quad (1)$$

Out-of-Phase Operation

In order to reduce input ripple current, buck 1 and buck 2 operate 180° out-of-phase. This feature allows for lower component cost, reduced board space and reduced EMI.

Start-Up and Sequencing

Figure 14 shows the start-up sequencing and PGOOD signal generation.

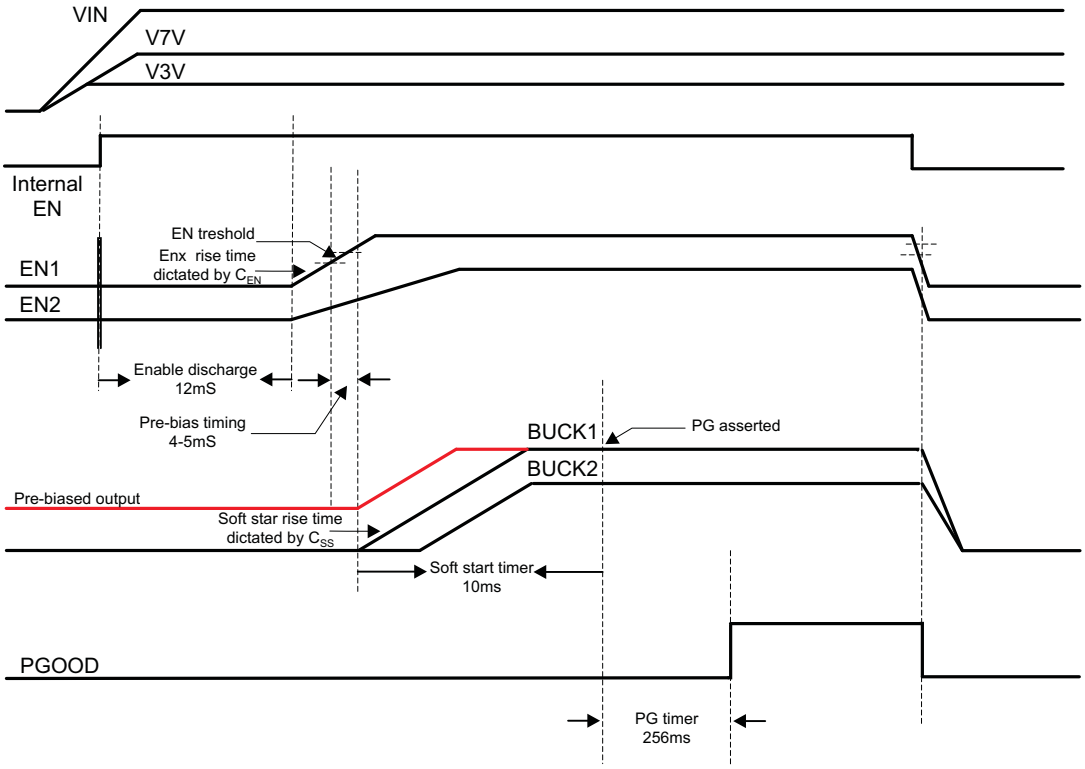


Figure 14. Start-Up Sequencing and PGOOD Signal Generation

Delayed Start-Up

On power-up the internal LDOs are powered immediately after the UVLO threshold is reached. The ENx (enable) pins will be shorted for 12 ms and then released to make sure they are always at 0 V at power-up. Once released the EN pins have a weak 1-MΩ pull-up to the 3V3 rail and the converters will start immediately. If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin.

Soft Start Time

The device has an internal pull-up current source of 5 µA that charges an external slow start capacitor to implement a slow start time. Equation 2 shows how to select a slow start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the slow start charge current (I_{SS}) is 5 µA. The soft start circuit requires 1 nF per 167 µS to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \quad (2)$$

The Power Good circuit for the bucks has a 10-ms watchdog. Therefore the soft start time should be lower than this value. It is recommended not to exceed 5 ms.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use the Equation 3 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \quad (3)$$

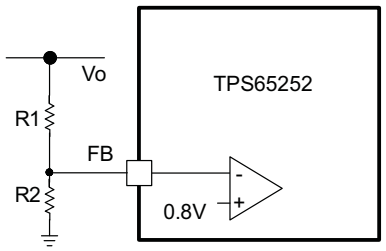


Figure 15. Voltage Divider Circuit

Loop Compensation

TPS65252 is a current mode control dc/dc converter. The error amplifier is a transconductance amplifier with a g_M of 130 µA/V.

A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60° and 90°, or type III (R_c, C_c and C_{ff}) to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. . It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

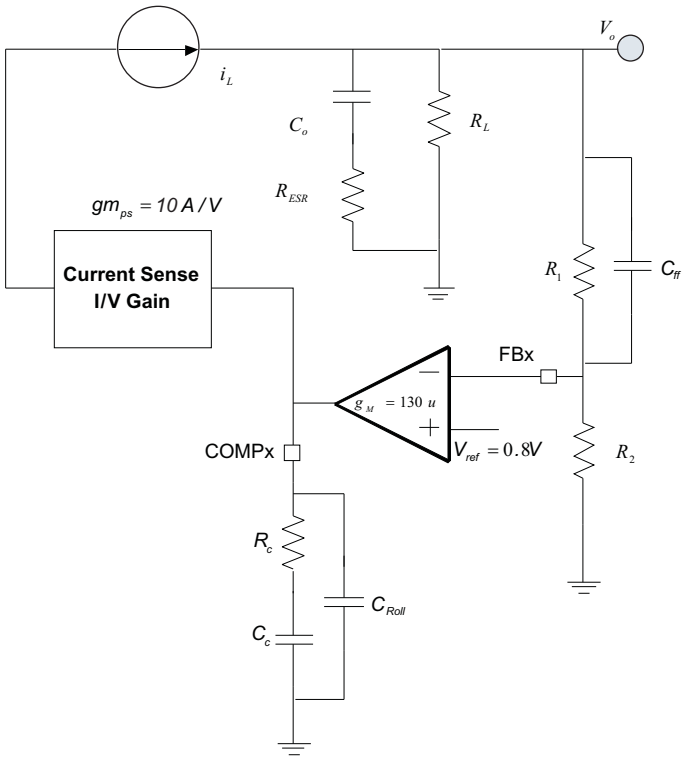


Figure 16. Loop Compensation

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies between 500 kHz and 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency (fc) to be less than 1/5 to 1/10 of switching frequency.	Suggested fc = fs/10	Suggested fc = fs/10
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Co}{g_M \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft start equivalent frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

Input Capacitor

Use 10-µF X7R/X5R ceramic capacitors at the input of the converter inputs. These capacitors should be connected as close as physically possible to the input pins of the converters.

Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters' outputs are more than 90% of its nominal output voltage. The default reset time is 256 ms. The polarity of the PGOOD is active high.

Current Limit Protection

Figure 17 shows the (peak) inductor current limit for Buck 1. The typical limit can be approximated with the following graph.

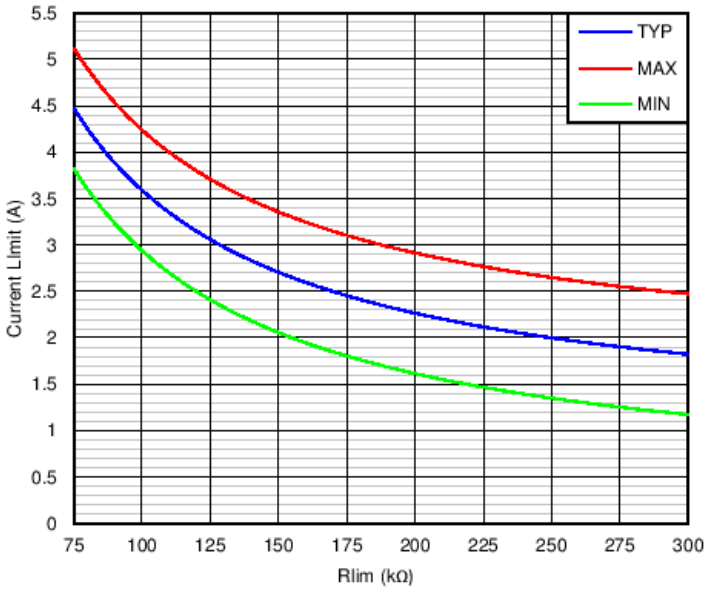


Figure 17. Buck 1

Figure 18 shows the (peak) inductor current limit for Buck 2. The typical limit can be approximated with the following graph.

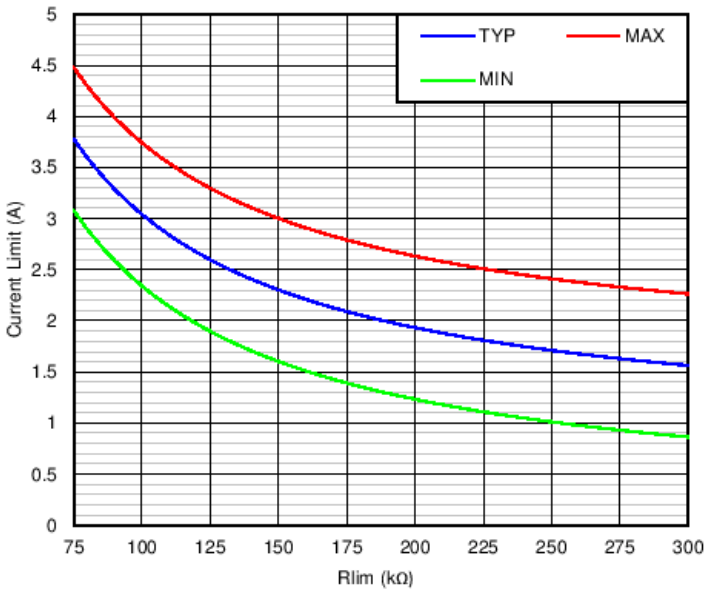


Figure 18. Buck 2

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, all the converters will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 10 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops below the lower OVP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Low Power Mode Operation

By pulling the Low_p pin high all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. Although each buck converter has a skip comparator that makes sure regulation is not lost when a heavy load is applied and low power mode is enabled, system design needs to make sure that the LP pin is pulled low for continuous loading in excess of 100 mA.

When low power is implemented, the peak inductor current used to charge the output capacitor is:

$$I_{LIMIT} = 0.25 \bullet T_{SLEEP\_CLK} \bullet \frac{V_{IN} - V_{OUT}}{L} \quad (4)$$

Where T_{SLEEP_CLK} is half of the converter switching period, $2/f_{SW}$.

The size of the additional ripple added to the output is:

$$\Delta V_{OUT} = \frac{1}{C} \bullet \left(\frac{L \bullet I_{LIMIT}^{2}}{2} \bullet \frac{V_{IN}}{V_{OUT} \bullet (V_{IN} - V_{OUT})} - \frac{I_{LOAD}}{f_{SLEEP\_CLK}} \right) \quad (5)$$

And the peak output voltage during low power operation is:

$$V_{OUT\_PK} = V_{OUT} + \frac{\Delta V_{OUT}}{2} \quad (6)$$

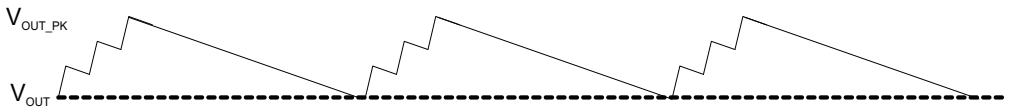


Figure 19. Peak Output Voltage During Low Power Operation

USB Switch

The USB switch has a typical resistance of 120 mΩ and can also operate in 3.3-V distribution systems. The USB switch is enabled with an active high signal to the USB_EN pin. The switch current limit can be set by a resistor connected to the rUSB pin to ground. When an over-current condition occurs at the output the switch will limit it to a value set by the following formula:

$$I_{CS\_USB}(A) = \frac{85}{rUSB(k\Omega)} \quad (7)$$

USB_Vin = 5 V

The overcurrent trip point (when current limit starts to operate and the switch operation changes from resistive mode to constant current mode) is typically twice the set value of I_{CS_USB}. If the overcurrent condition lasts more than T_{CS_USB} the USB_nLIM pin (active low, open drain) will change status to indicate an alarm condition.

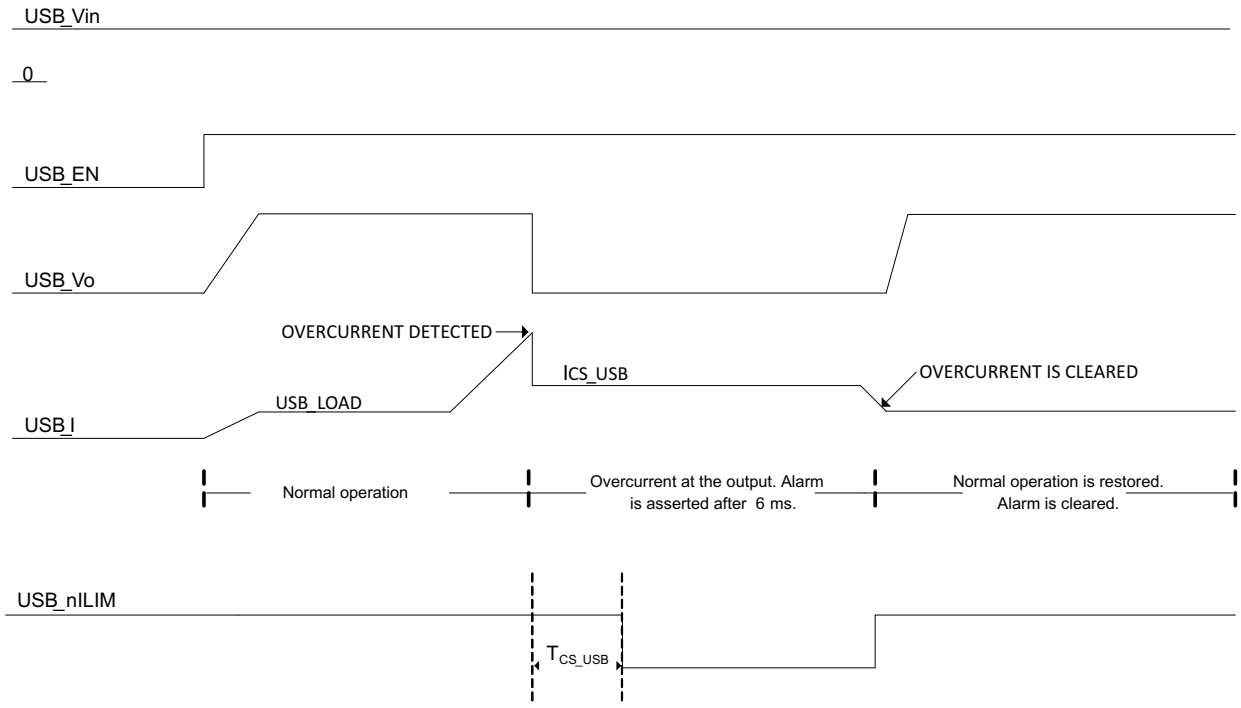


Figure 20. USB Switch

The TPS65252 switch will safely handle overcurrent conditions due to heavy capacitive loads or overcurrent and solid short conditions at the output of the switch. If a continuous short-circuit condition is applied to its output, the USB switch will shut-down once its temperature reaches 130°C, allowing for the buck converters to operate unaffected. Once the USB switch cools down it will restart automatically, as long as the USB_EN pin stays enabled during the whole procedure.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

APPLICATION INFORMATION

3.3-V and 6.5-V LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 10 µF for V7V pin 21
- 3.3 µF to 10 µF for V3V pin 22

Power Dissipation

Total power dissipation inside TPS65252 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature.

To calculate the temperature inside the device under continuous loading use the following procedure.

1. Define the set voltage for arch converter.
2. Define the continuous loading on each converter. The maximum loading for continuous operation is 3 A for buck1 and 2 A for buck 2 for the whole operational voltage range. Extended loading to 3.5 A and 2.5 A is acceptable for short time periods.
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.

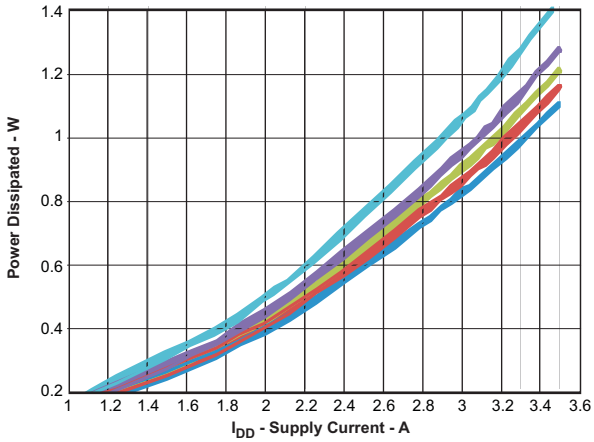


Figure 21. Buck 1 V_{IN} = 12 V, f_S = 500 kHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

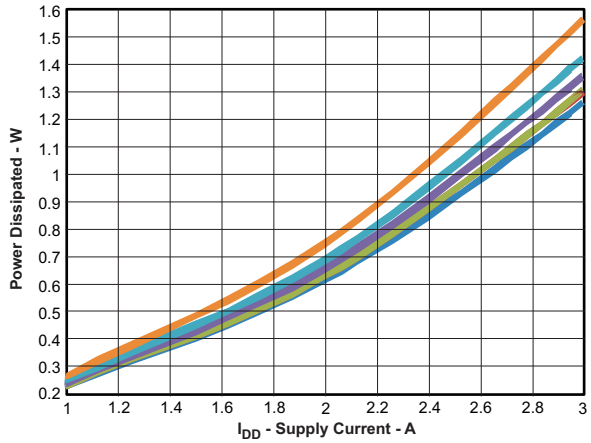


Figure 22. Buck 2 V_{IN} = 12 V, f_S = 500 kHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

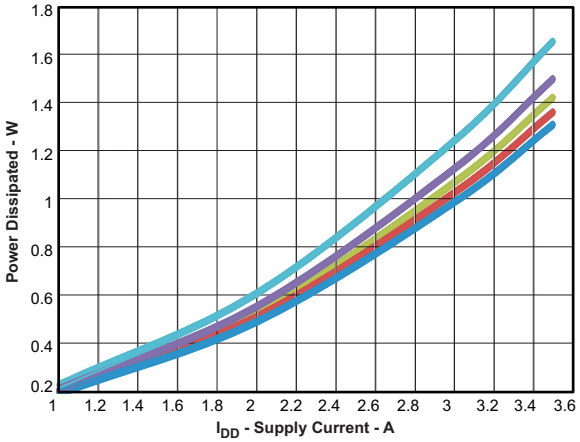


Figure 23. Buck 1 V_{IN} = 12 V, f_S = 1.1 MHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

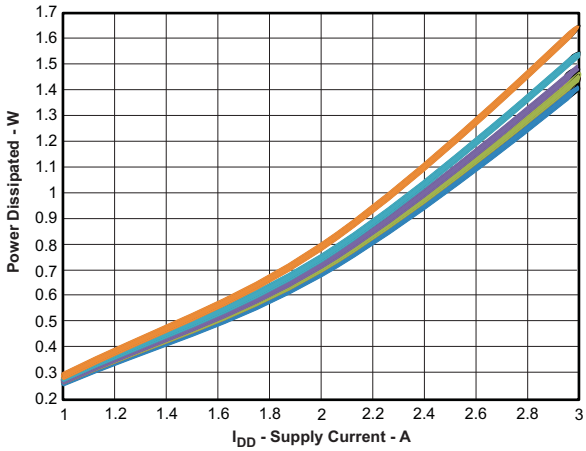


Figure 24. Buck 2 V_{IN} = 12 V, f_S = 1.1 MHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

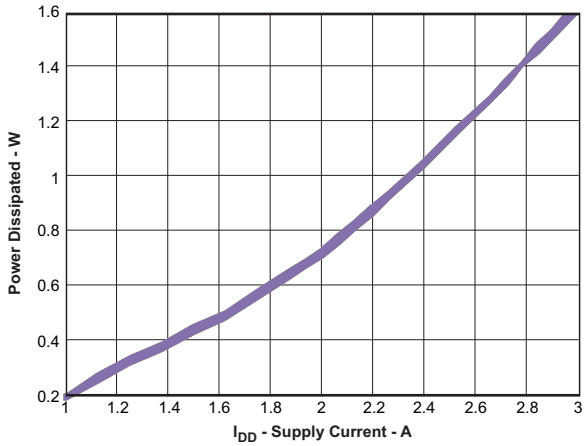


Figure 25. Buck 1 V_{IN} = 5 V, f_S = 500 kHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

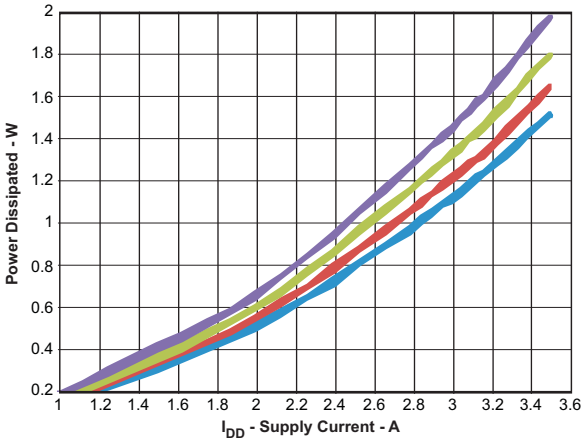


Figure 26. Buck 2 V_{IN} = 5 V, f_S = 500 kHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

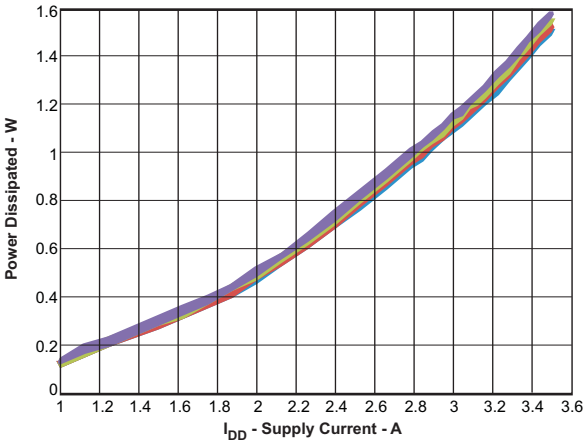


Figure 27. Buck 1 V_{IN} = 5 V, f_S = 1.1 MHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

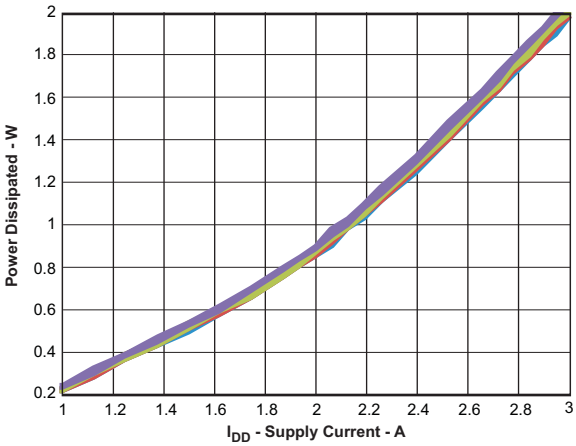


Figure 28. Buck 2 V_{IN} = 5 V, f_S = 1.1 MHz, V_O (From Top to Bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

4. To calculate the maximum temperature inside the IC use the following formula.

$$T_{HOTSPOT} = T_A + P_{DIS} \bullet R_{JA} \quad (8)$$

Where:

T_A is the ambient temperature

P_{DIS} is the sum of losses in all converters

R_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on the board layout

Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place VOUT, and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area sould be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS65252 device to provide a thermal path from the Powerpad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the COMP pins. The COMP and OSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65252RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65252	Samples
TPS65252RHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65252	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

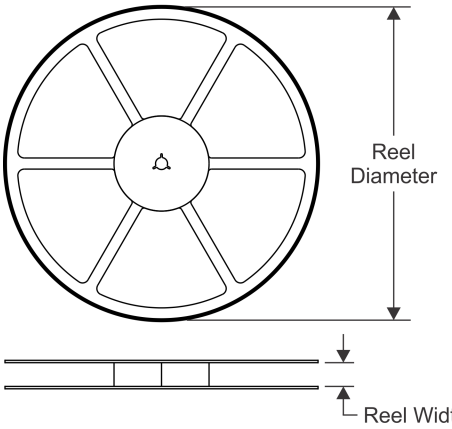
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

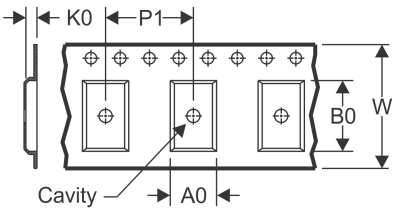
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

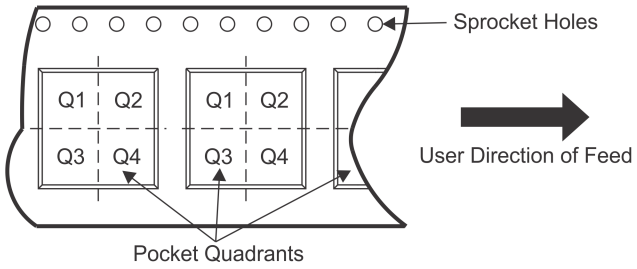


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

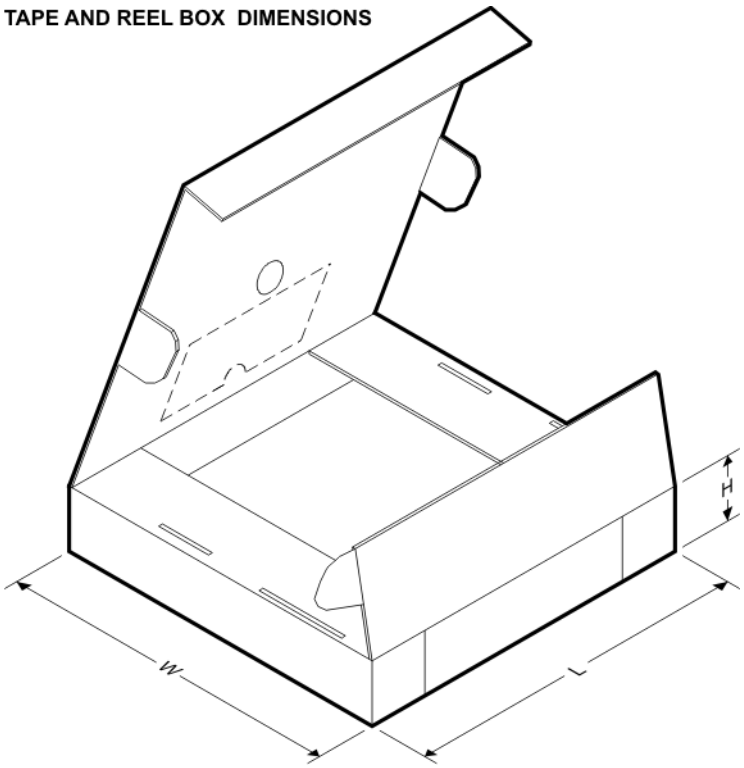
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65252RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65252RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65252RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
TPS65252RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

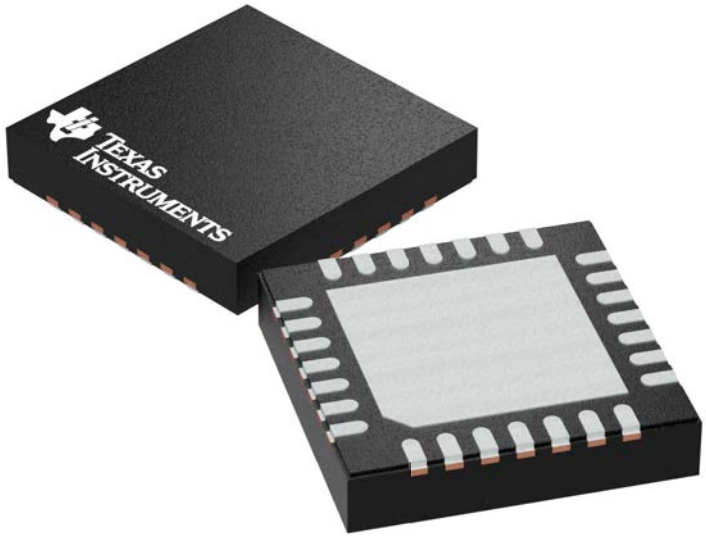
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

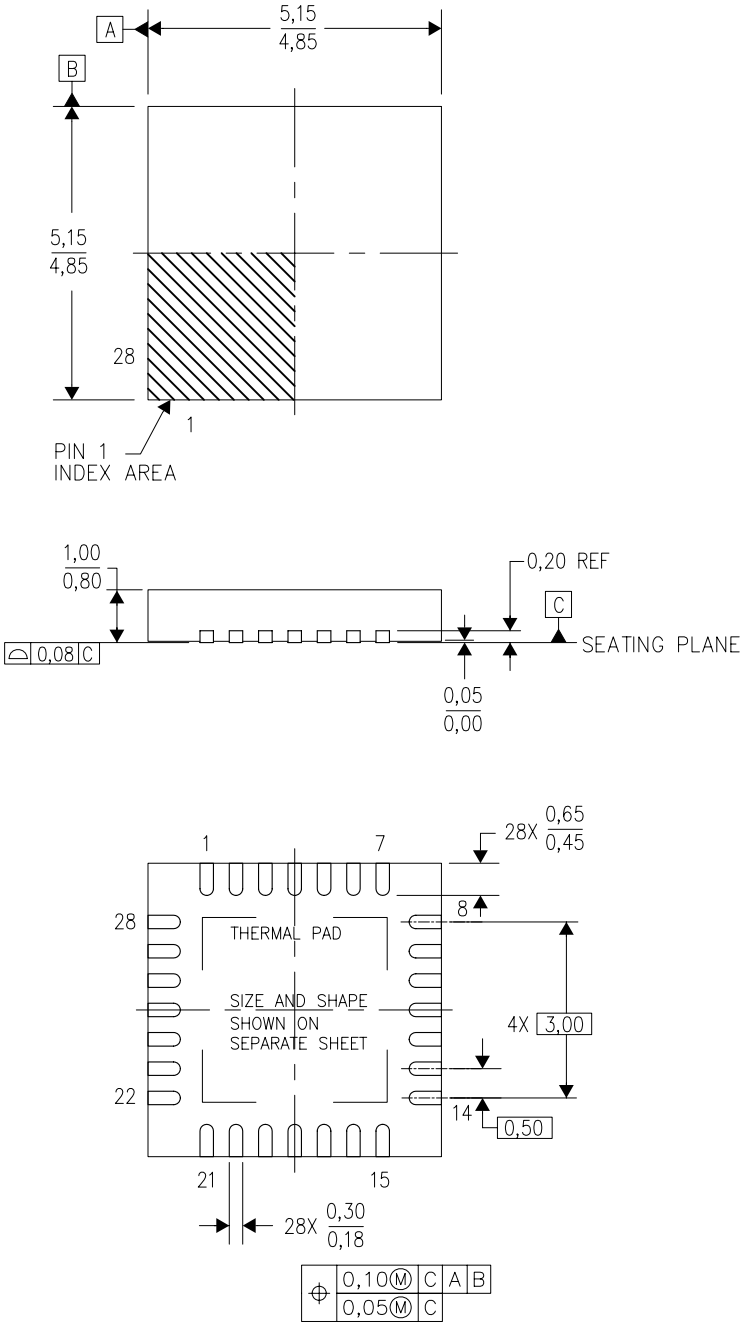
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204400/G

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

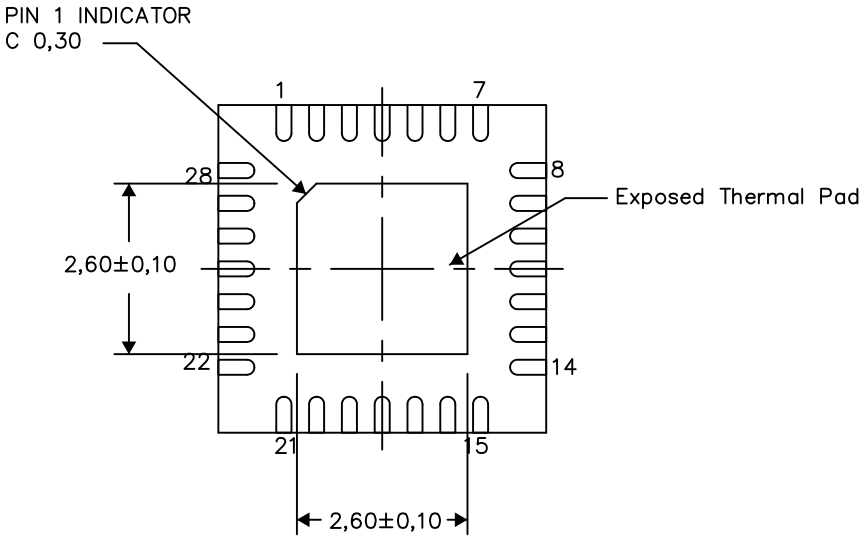
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206358–3/L 05/15

NOTE: All linear dimensions are in millimeters

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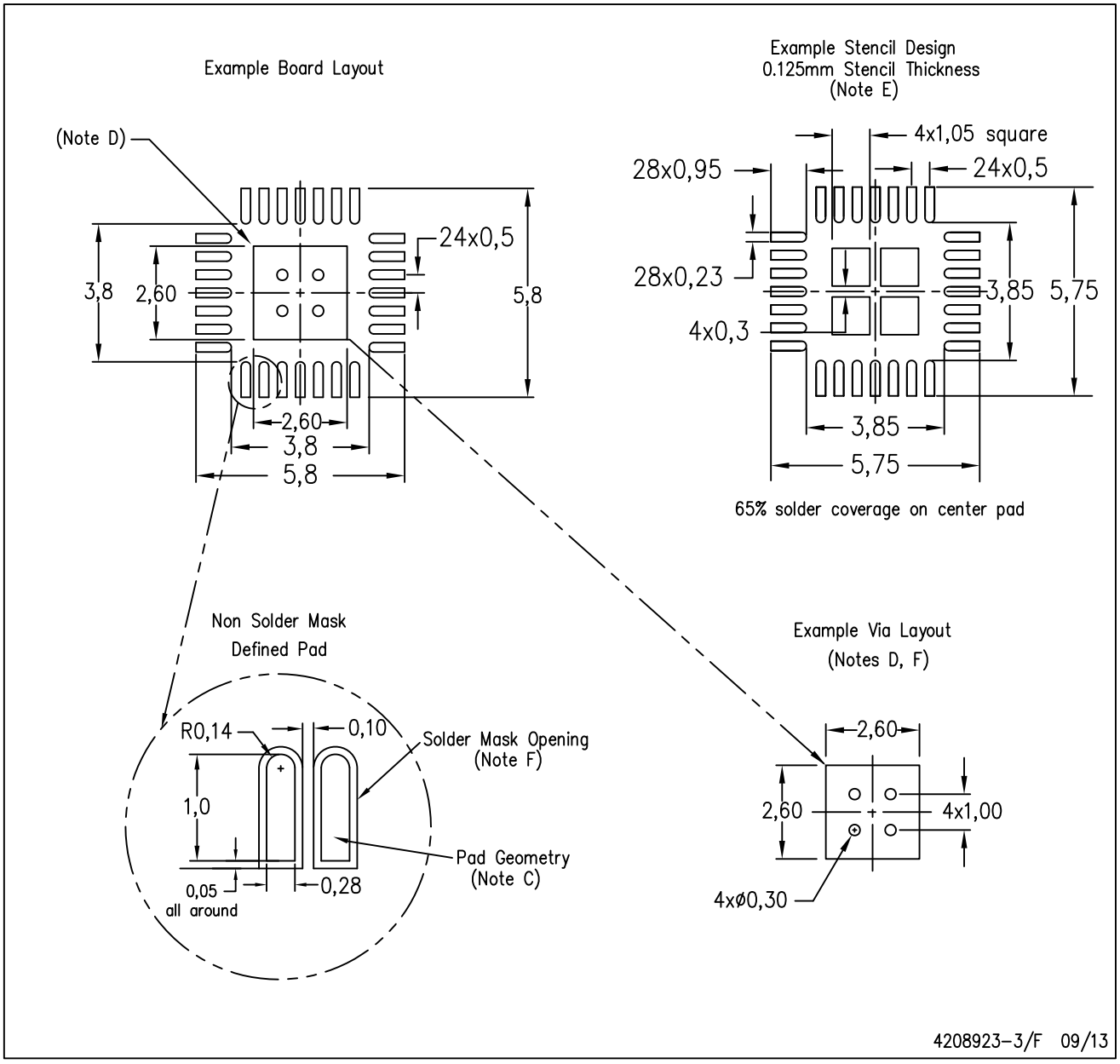

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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