

P-Channel Enhancement Mode MOSFET

TDM3405

DESCRIPTION

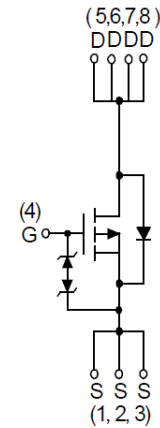
The TDM3405 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

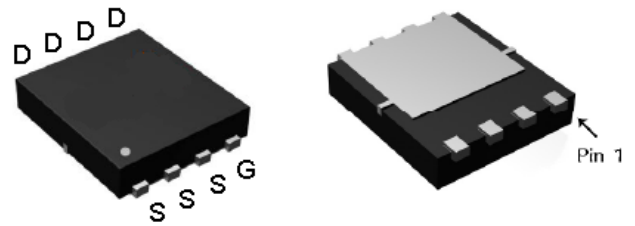
- -40V/-55A
- RDS(ON) < 15mΩ @ VGS=-4.5V
RDS(ON) < 9.4mΩ @ VGS=-10V
RDS(ON) < 8mΩ @ VGS=-20V
- Reliable and Rugged
- HBM ESD capability level of 8KV typical
- Lead free product is available
- DFN5X6 Package

Application

- PWM applications
- Load switch
- Power management



P-Channel MOSFET



DFN5x6-8

ABSOLUTE MAXIMUM RATINGS(TA=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V _{DS}	-40	V
Gate-Source Voltage	V _{GS}	±25	V
Continuous Drain Current(V _{GS} =-10V) note1	I _D (T _A =25°C)	-17	A
	I _D (T _A =70°C)	-14	A
300µs Pulsed Drain Current Tested note1	I _{DP} (T _A =25°C)	-69	A
Continuous Drain Current (V _{GS} =-10V) note2	I _D (T _C =25°C)	-55	A
	I _D (T _C =100°C)	-35	A
300µs Pulsed Drain Current Tested note2	I _{DP} (T _C =25°C)	-222	A
Diode Continuous Forward Current note2	I _S	-27	A
Maximum Power Dissipation note1	P _D (T _A =25°C)	5	W
	P _D (T _A =70°C)	3.2	W
Maximum Power Dissipation note2	P _D (T _C =25°C)	52	W
	P _D (T _C =100°C)	20	W

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Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C
Thermal Resistance-Junction to Ambient <small>note1</small>	$R_{\theta JA}$	60	°C/W
Thermal Resistance-Junction to Case <small>note2</small>	$R_{\theta JC}$	2.4	°C/W

NOTES:

- Surface Mounted on 1in^2 pad area, $t \leq 10\text{sec}$. $R_{\theta JA}$ steady state $t = 999\text{s}$.
- The power dissipation P_D is based on $T_{J(\text{MAX})} = 150^\circ\text{C}$, and it is useful for reducing junction-to-case thermal resistance ($R_{\theta JC}$) when additional heat sink is used.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-32, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.5	-2	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_{DS}=-15A$	-	11	15	$m\Omega$
		$V_{GS}=-10V, I_{DS}=-25A$	-	7.5	9.4	$m\Omega$
		$V_{GS}=-20V, I_{DS}=-25A$	-	6.6	8	$m\Omega$
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V, F=1.0\text{MHz}$	-	2780	3610	PF
Output Capacitance	C_{oss}		-	425	-	PF
Reverse Transfer Capacitance	C_{rss}		-	330	-	PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=20\Omega, V_{GEN}=-10V, R_G=6\Omega, I_{DS}=-1A$	-	17	30	nS
Turn-on Rise Time	t_r		-	14	25	nS
Turn-Off Delay Time	$t_{d(off)}$		-	59	106	nS
Turn-Off Fall Time	t_f		-	22	40	nS
Total Gate Charge	Q_g	$V_{DS}=-20V, I_{DS}=-25A, V_{GS}=-10V$	-	59	83	nC
Gate-Source Charge	Q_{gs}		-	8	-	nC
Gate-Drain Charge	Q_{gd}		-	16	-	nC
Body Diode Reverse Recovery Time	T_{rr}	$I_{DS}=-25A, di/dt=100A/\mu s$	-	23	-	nS
Body Diode Reverse Recovery Charge	Q_{rr}		-	10	-	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage <small>(Note 3)</small>	V_{SD}	$V_{GS}=0V, I_{SD}=-1A$	-	-0.7	-1	V

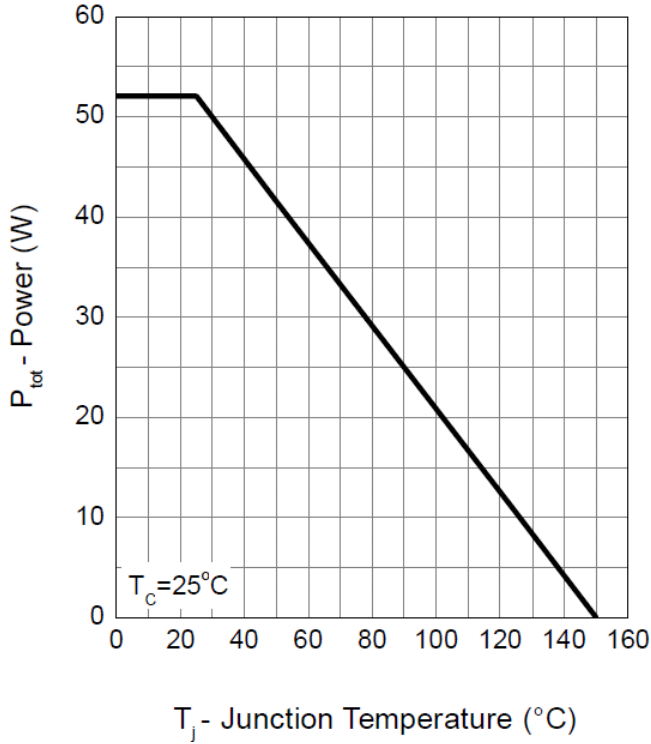
NOTES:

- Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing

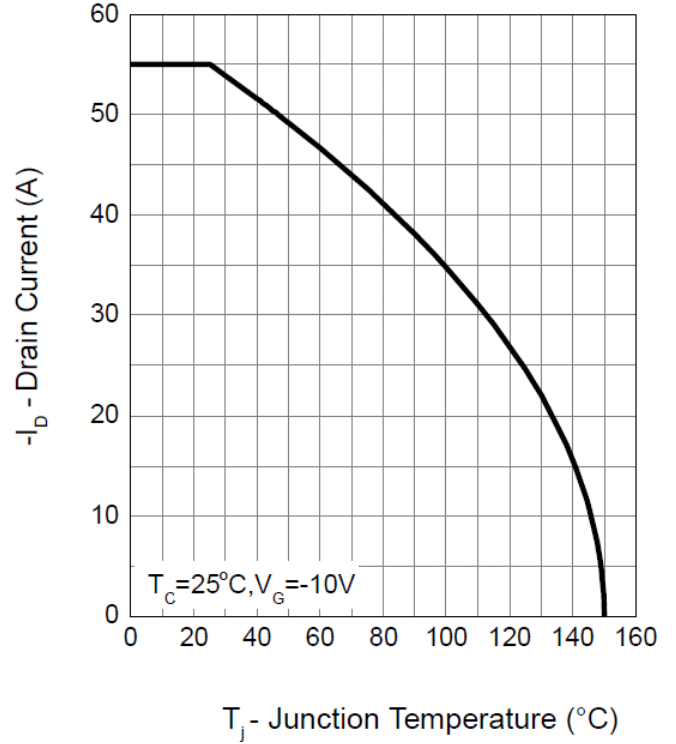
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Typical Operating Characteristics

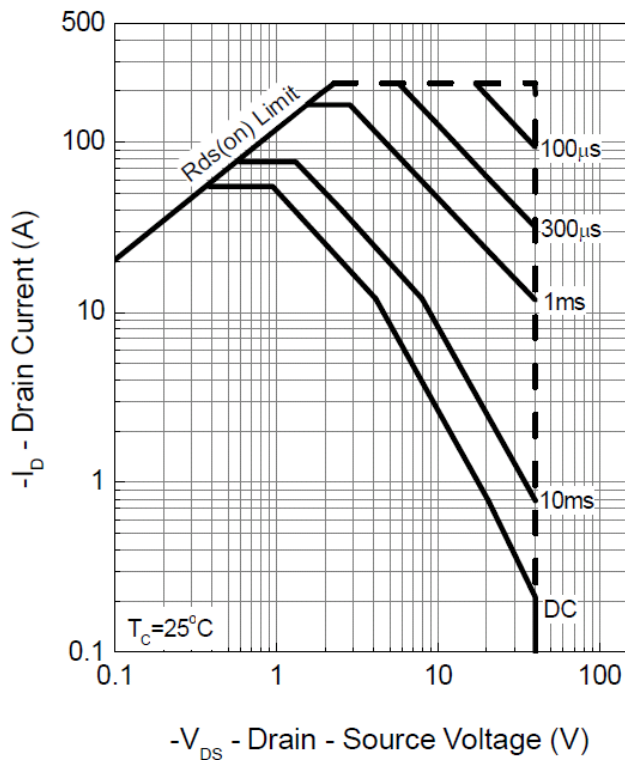
Power Dissipation



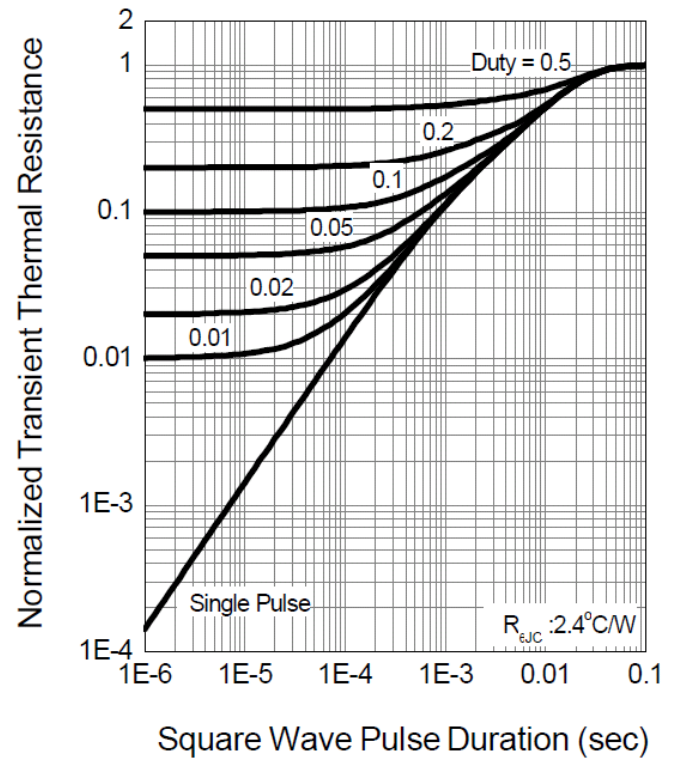
Drain Current



Safe Operation Area



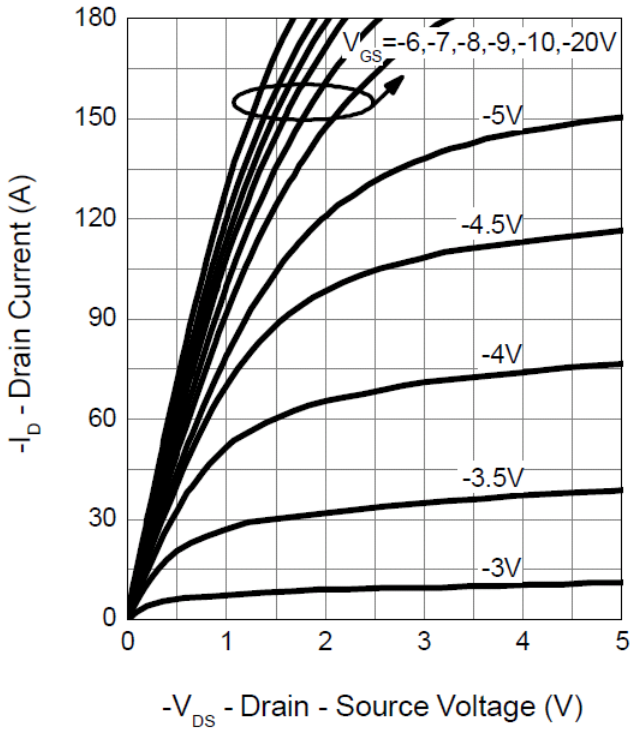
Thermal Transient Impedance



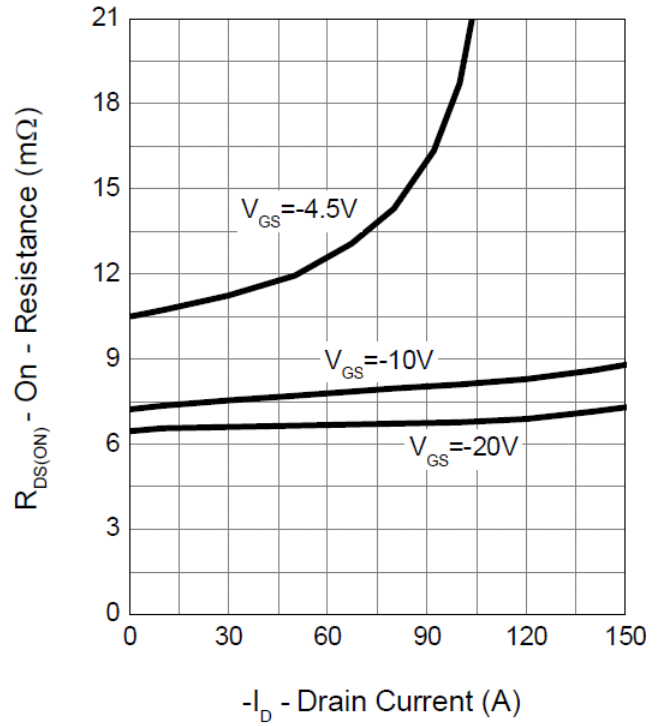
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Typical Operating Characteristics(Cont.)

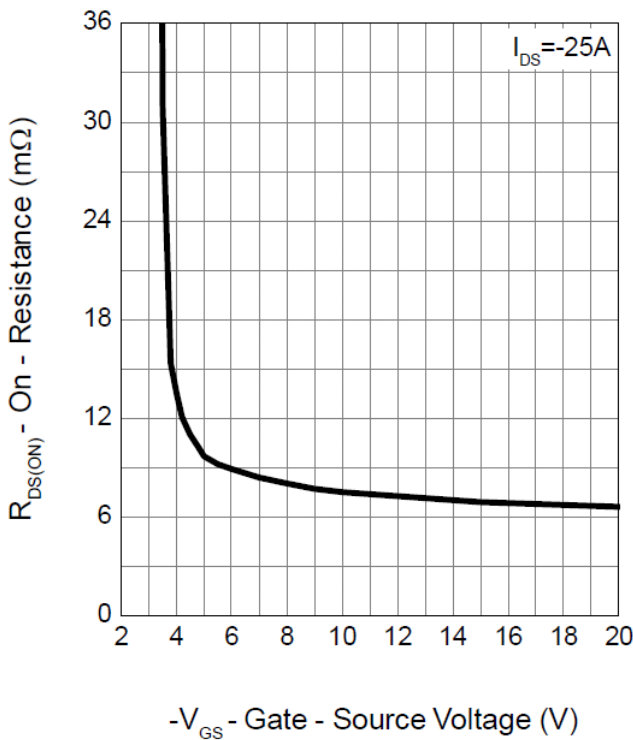
Output Characteristics



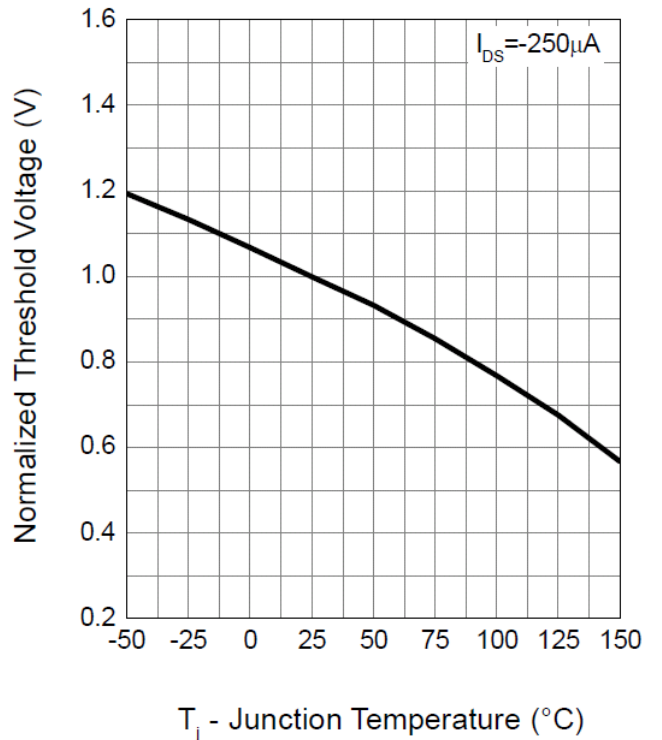
Drain-Source On Resistance



Gate-Source On Resistance

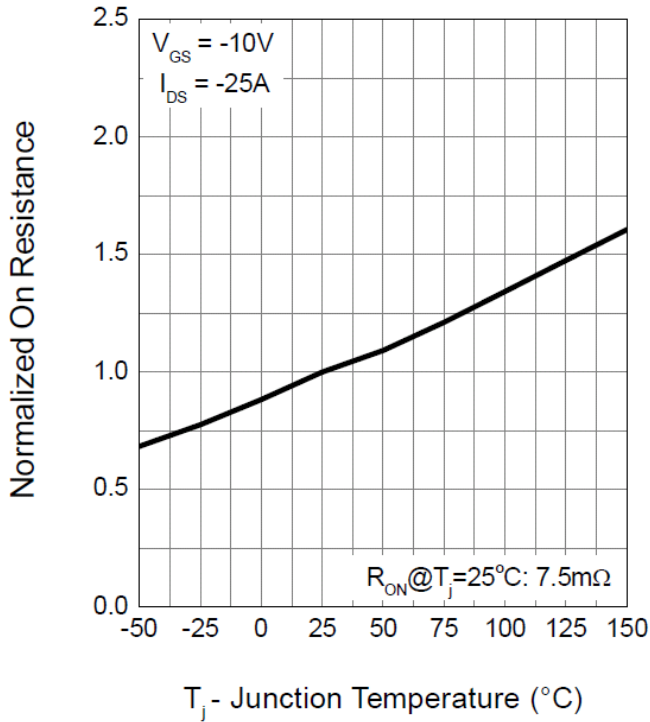


Gate Threshold Voltage

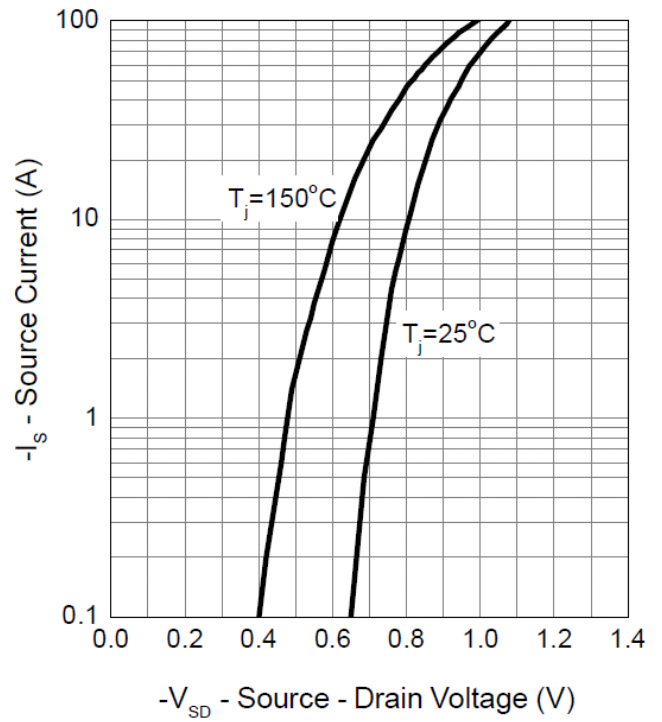


Typical Operating Characteristics (Cont.)

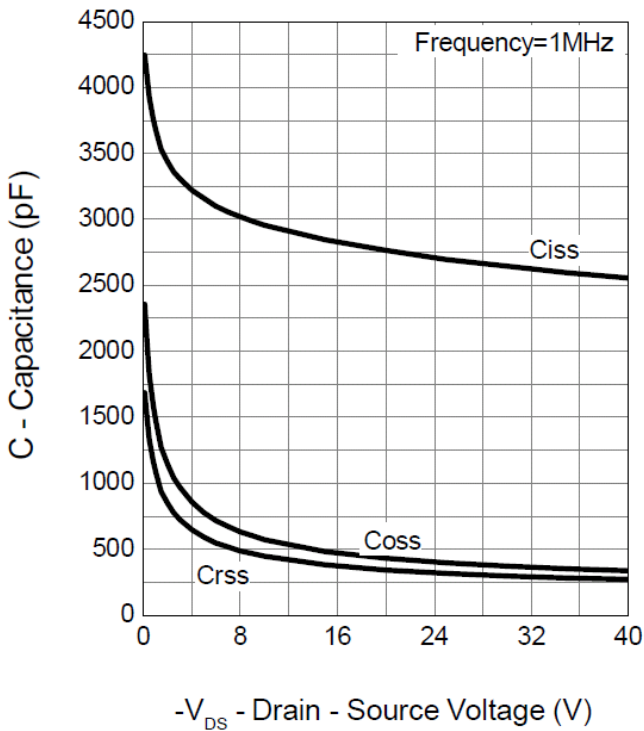
Drain-Source On Resistance



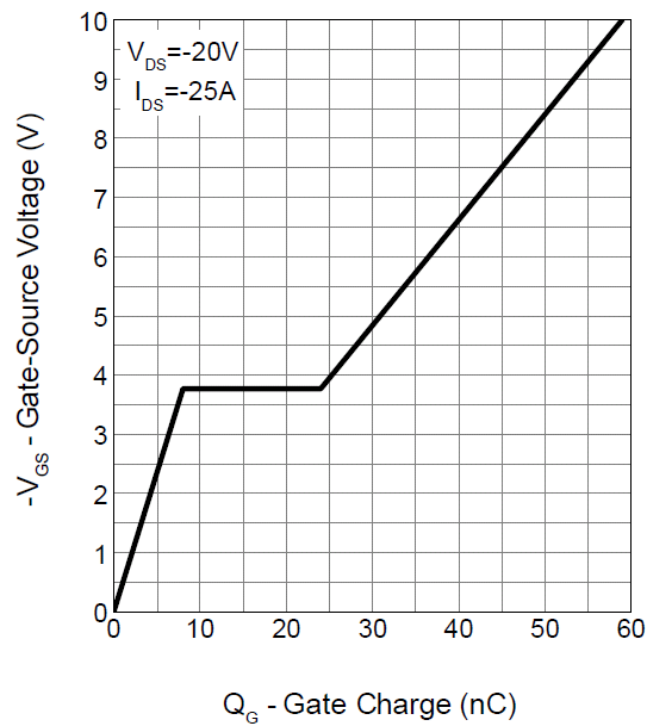
Source-Drain Diode Forward



Capacitance

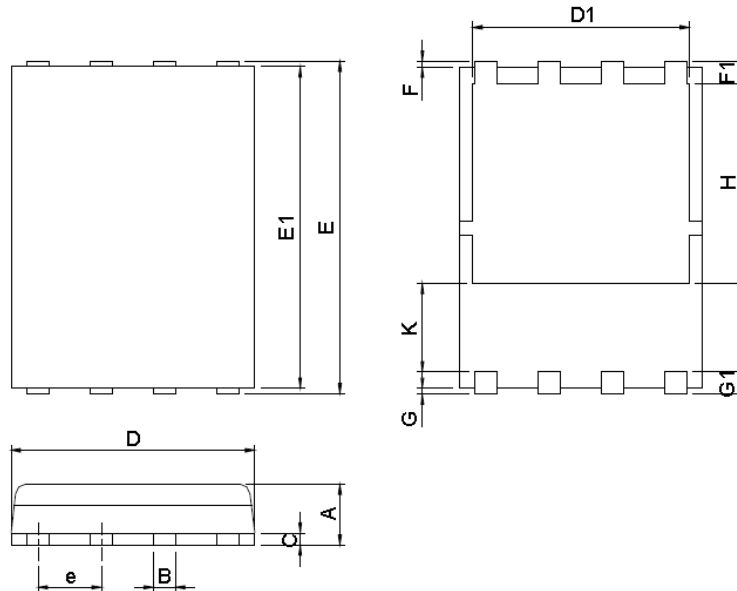


Gate Charge



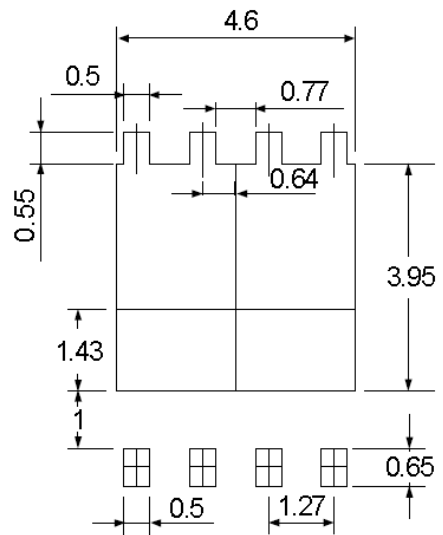
Package Information

DFN5*6-8 Package



DIMENSIONS	DFN5x6-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.20	0.035	0.047
B	0.3	0.51	0.012	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.30	0.189	0.209
D1	4.00	4.40	0.157	0.173
E	5.90	6.20	0.232	0.244
E1	5.50	5.80	0.217	0.228
e	1.27 BSC		0.050 BSC	
F	0.05	0.30	0.002	0.012
F1	0.35	0.75	0.014	0.030
G	0.05	0.30	0.002	0.012
G1	0.35	0.75	0.014	0.030
H	3.34	3.9	0.131	0.154
K	0.762	-	0.03	-

RECOMMENDED LAND PATTERN



UNIT: mm

Note : 1.Dimension D, D1,D2 and E1 do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed 10 mil.

Design Notes