

SE40120A

**N-Channel Enhancement-Mode MOSFET**

Revision: A

**General Description**

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

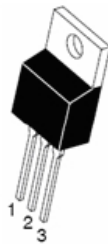
**Features**

For a single MOSFET

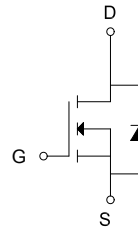
- $V_{DS} = 40V$
- $R_{DS(ON)} = 3.2m\Omega @ V_{GS}=10V$

**Pin configurations**

See Diagram below



TO-220



**Absolute Maximum Ratings**

Parameter		Symbol	Rating	Units
Drain-Source Voltage		$V_{DS}$	40	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	120	A
	Pulsed		330	
Single Pulse Avalanche Energy		$E_{AS}$	1080	mJ
Peak Diode Recovery		$dv/dt$	5	V/ns
Total Power Dissipation	@TA=25°C	$P_D$	130	W
Operating Junction Temperature Range		$T_J$	-55 to 150	°C

**Thermal Resistance**

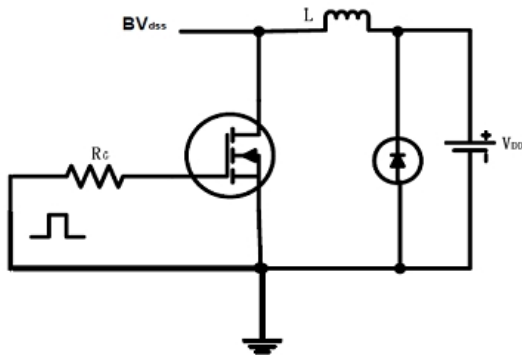
Symbol	Parameter	TO-220	Units
$R_{\theta JC}$	Junction to Case	0.6	°C/W
$R_{\theta JA}$	Junction to Ambient ( $t \leq 10s$ )	60	°C/W

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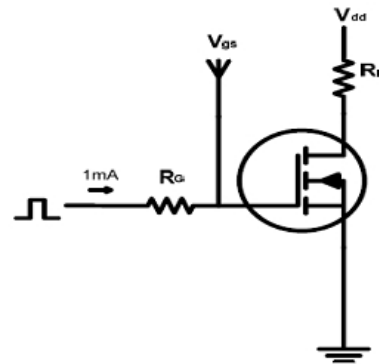
Electrical Characteristics (T <sub>J</sub> =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS (Note 2)</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0 V	40	45		V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =20 V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2		2.5	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		3.2	4.0	mΩ
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		5400		pF
C <sub>oss</sub>	Output Capacitance			970		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			380		pF
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	V <sub>GS</sub> =10V, V <sub>DS</sub> =80V, I <sub>D</sub> =20A		68		nC
Q <sub>gs</sub>	Gate Source Charge			17		nC
Q <sub>gd</sub>	Gate Drain Charge			16		nC
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =80V, R <sub>GEN</sub> =3.9Ω I <sub>D</sub> =20A		15		ns
t <sub>d(off)</sub>	Turn-Off Delay Time			52		ns
t <sub>d(r)</sub>	Turn-On Rise Time			18		ns
t <sub>d(f)</sub>	Turn-Off Fall Time			23		ns

Test Circuits and Waveform

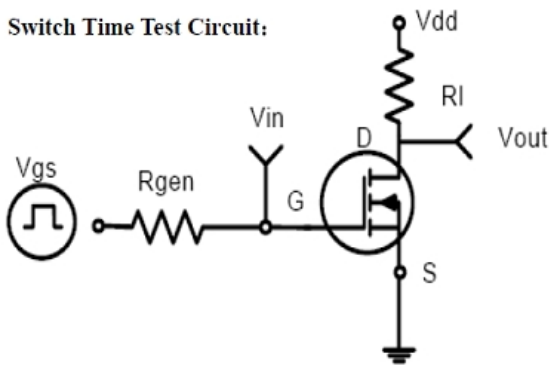
EAS test circuits:



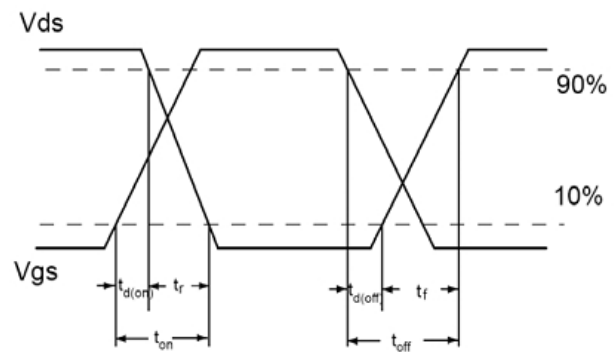
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Typical Characteristics

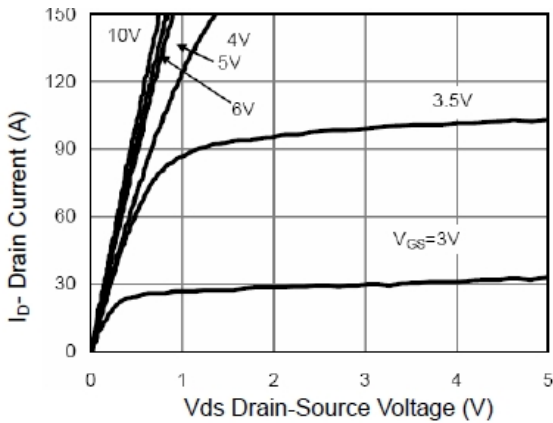


Figure 1 Output Characteristics

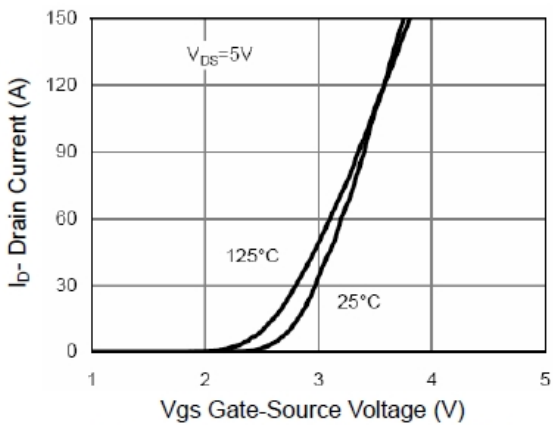


Figure 2 Transfer Characteristics

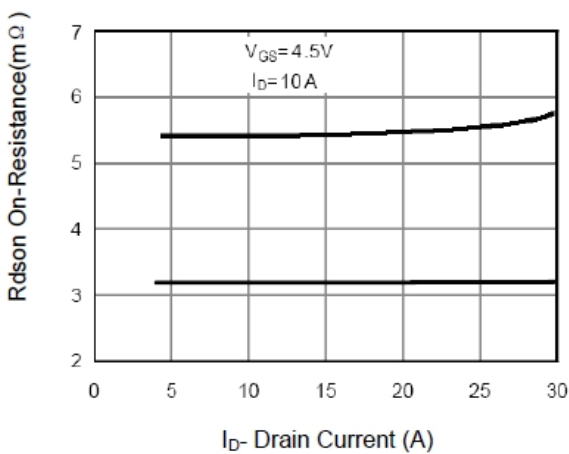


Figure 3  $R_{DS(on)}$ - Drain Current

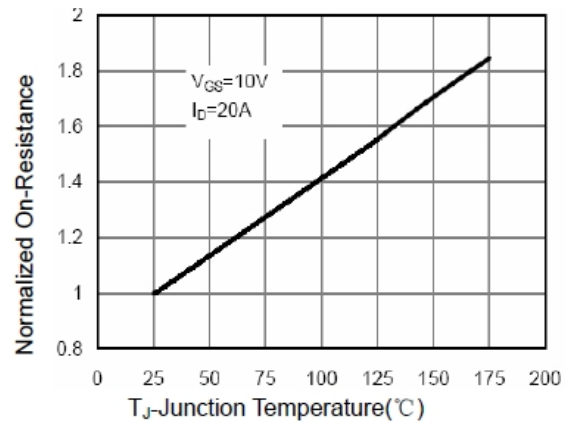


Figure 4  $R_{DS(on)}$ -Junction Temperature

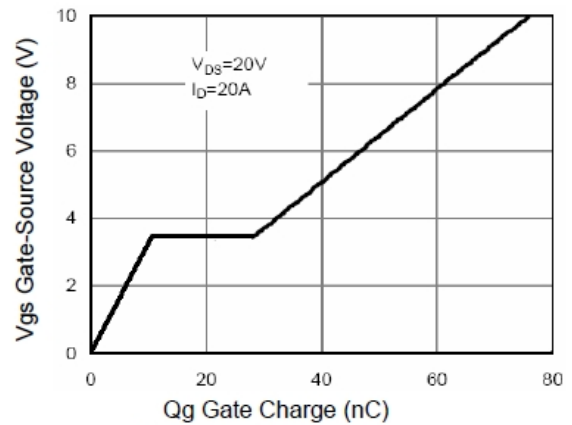


Figure 5 Gate Charge

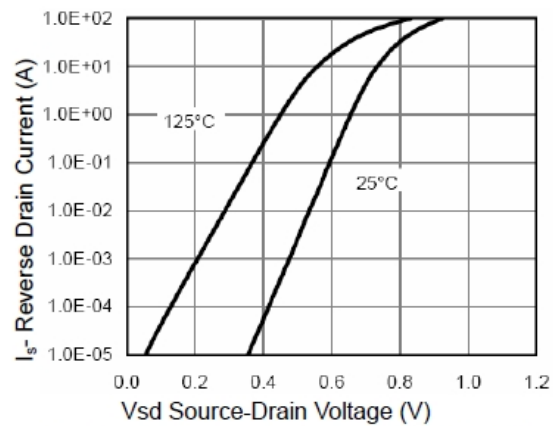


Figure 6 Source- Drain Diode Forward

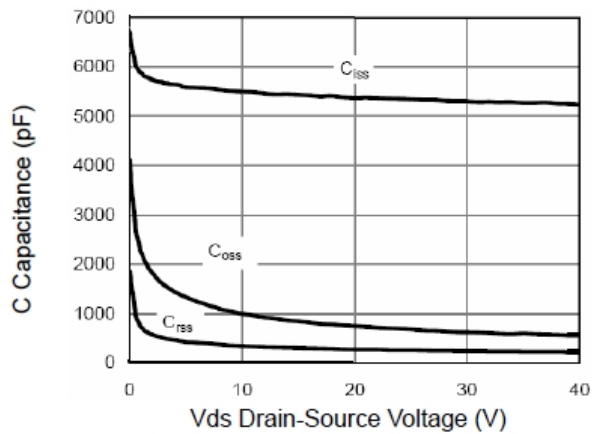


Figure 7 Capacitance vs Vds

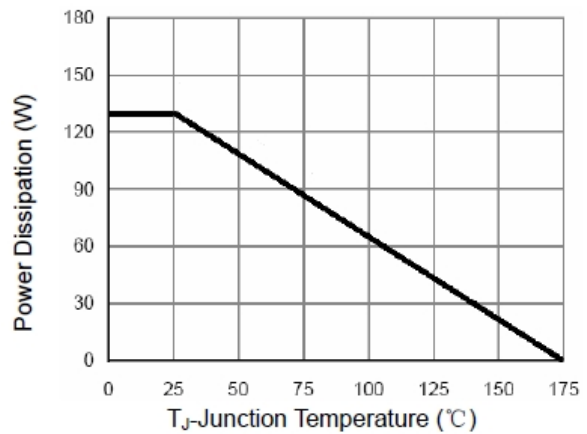


Figure 9 Power De-rating

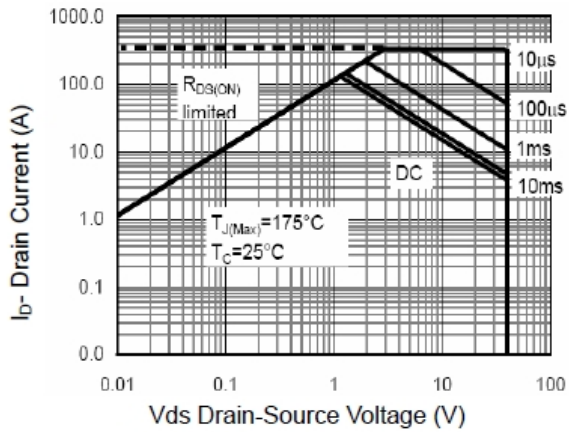


Figure 8 Safe Operation Area

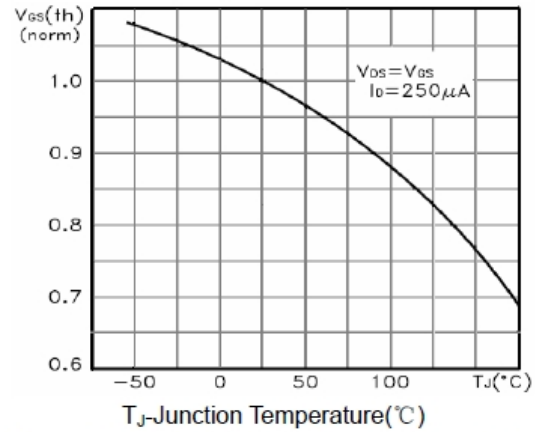


Figure 10  $V_{GS(th)}$  vs Junction Temperature

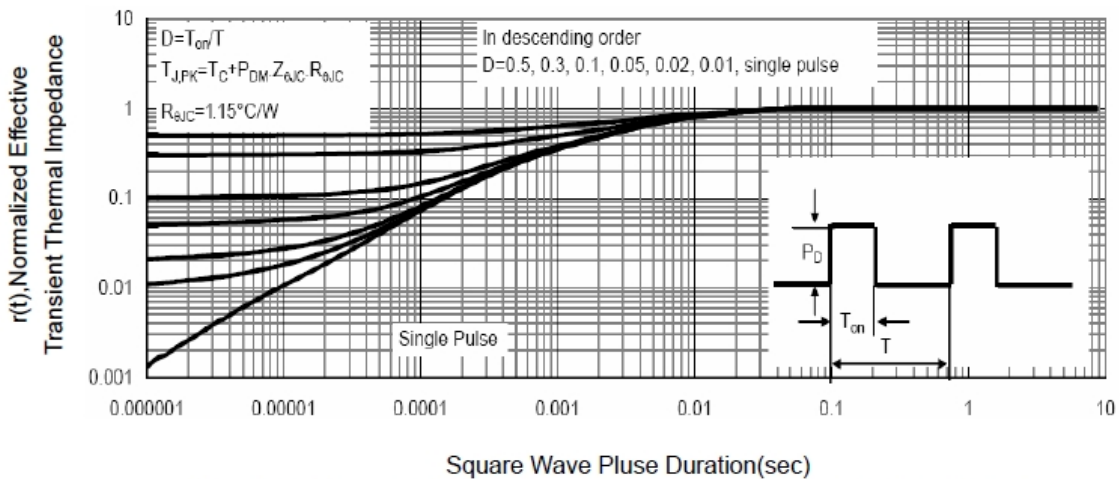
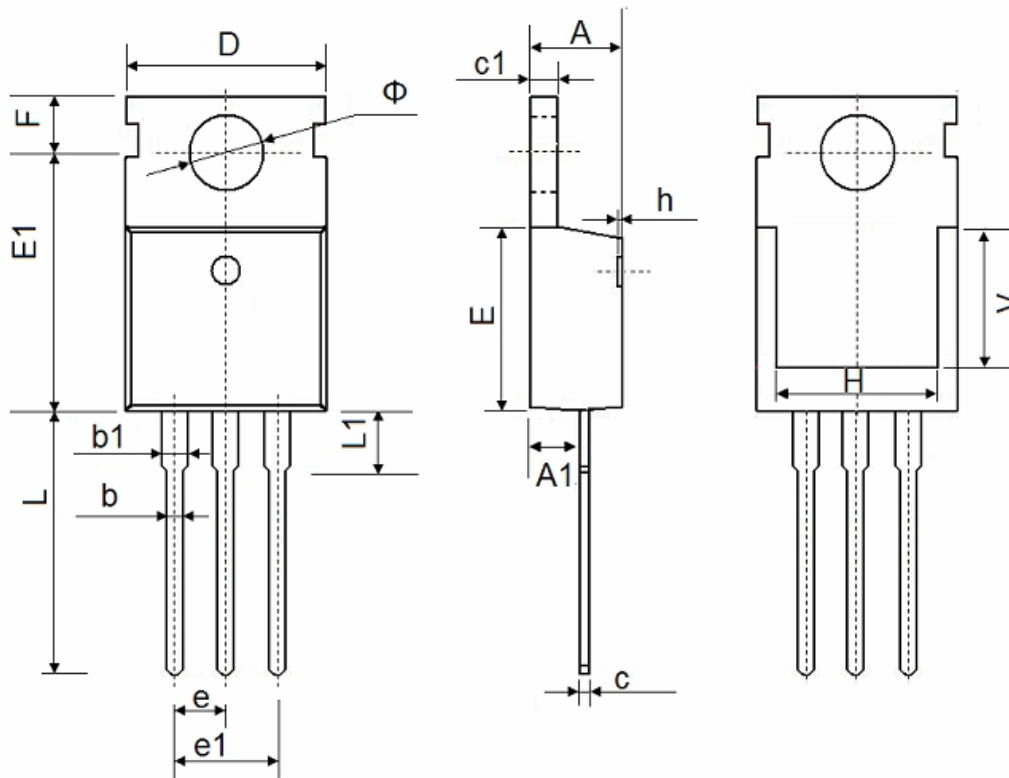


Figure 11 Normalized Maximum Transient Thermal Impedance

# SE40120A

## Package Outline Dimension

### TO-220



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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