SI2300

PUOLOP 迪浦

20V N-Channel Enhancement Mode MOSFET

VDS= 20V

RDS(ON), Vgs@ 4.5V, Ids@ 3.6A ＜70mΩ

RDS(ON), Vgs@ 2.5V, Ids@ 3.1A ＜80mΩ

Features

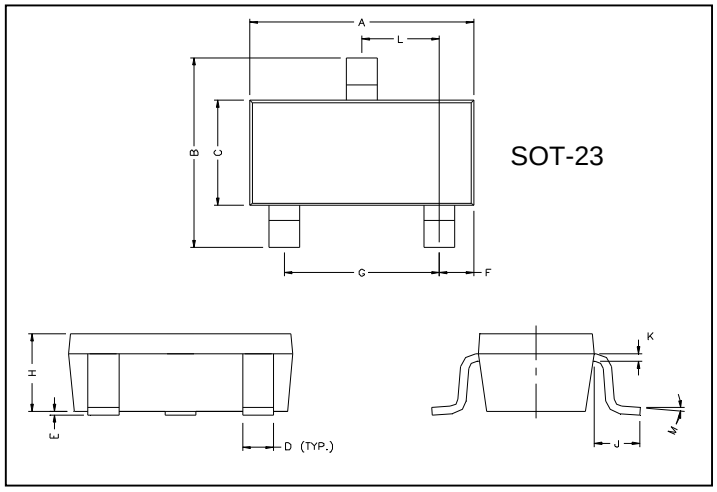
Advanced trench process technology

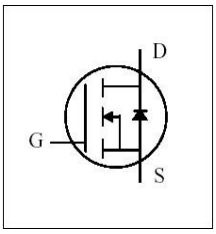
High Density Cell Design For Ultra Low On-Resistance

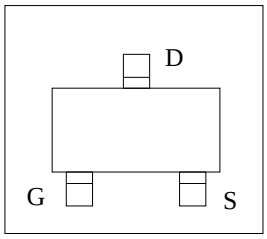
High Power and Current handing capability

Ideal for Li ion battery pack applications

Package Dimensions







REF.	Millimeter		REF.	Millimete	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current		I_D	3.6	A
Pulsed Drain Current [1]		I_{DM}	8	
Maximum Power Dissipation	TA = 25°C	P_D	1.25	W
	TA = 75°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		$R_{\theta JA}$	78	°C/W

Notes

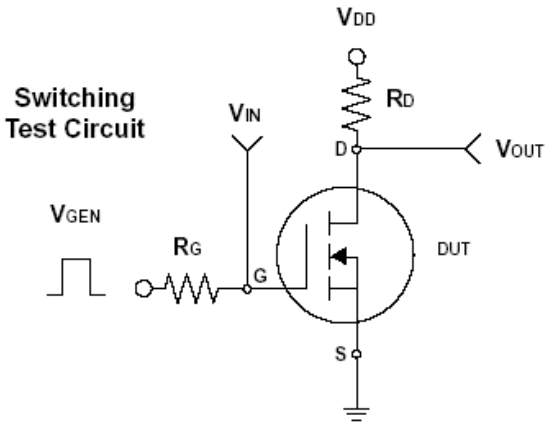
[1] Pulse width limited by maximum junction temperature.

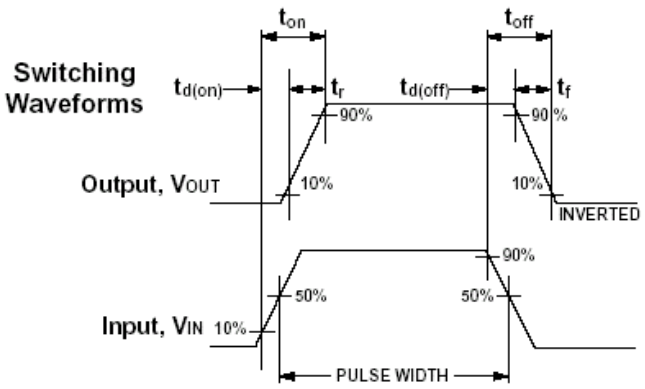
[2] Surface Mounted on FR4 Board, t ≤ 5 sec.

ELECTRICAL CHARACTERISTICS (TA = 25oC unless otherwise noted)

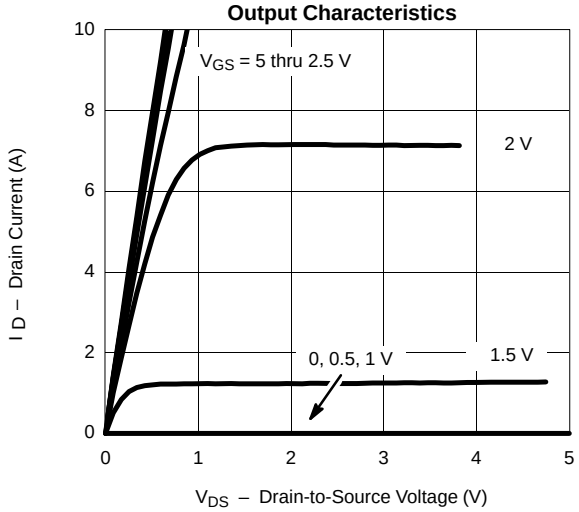
Parameter	Symbol	Test Condition	Min.	Typ.	Miax.	Unit
Static [3]						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	20			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 2.5V, I_D = 3.1A		70.0	80.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 3.6A		60.0	70.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = 250uA	0.5	0.76	1.5	V
Zero Gate Voltage Drain Current 0	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0V			±100	nA
Forward Transconductance	g_{fs}	V_{DS} = 5V, I_D = 4.2A		5	__	S
Dynamic[4]						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 3.6A V_{GS} = 4.5V		5.4		nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, R_G = 6Ω I_D = 1A, V_{GS} = 4.5V RL = 5.5Ω		12		ns
Turn-On Rise Time	t_r			36		
Turn-Off Delay Time	$t_{d(off)}$			34		
Turn-Off Fall Time	t_f			10		
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V f = 1.0 MHz		340		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			33		
Source-Drain Diode						
Max. Diode Forward Current	I_S				1.6	A
Diode Forward Voltage	V_{SD}	I_S = 1.0A, V_{GS} = 0V			1.0	V

Notes
3) Short duration test pulse used to minimize self-heating effect.
4) Pulse test pulse width<=300us,duty cycle<= 2%.

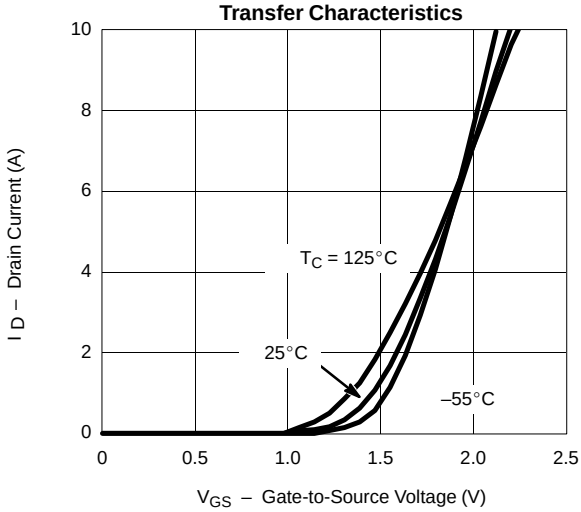




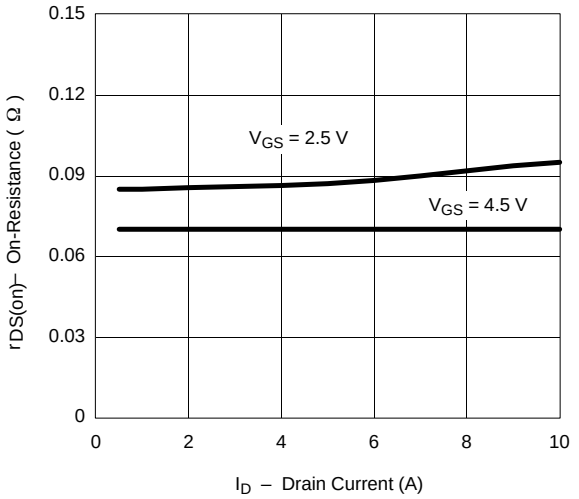
Output Characteristics



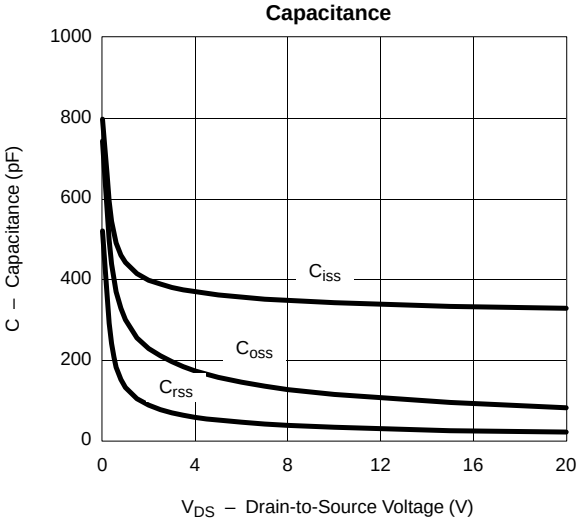
Transfer Characteristics



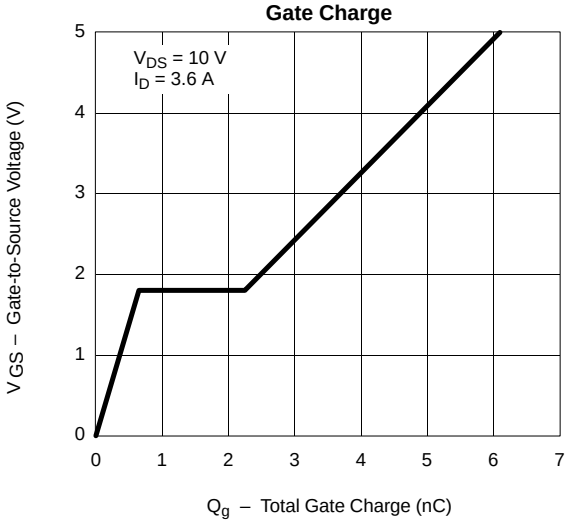
On-Resistance vs. Drain Current



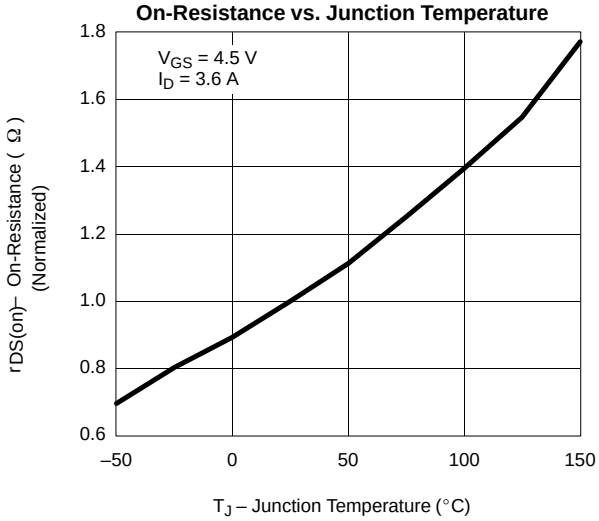
Capacitance



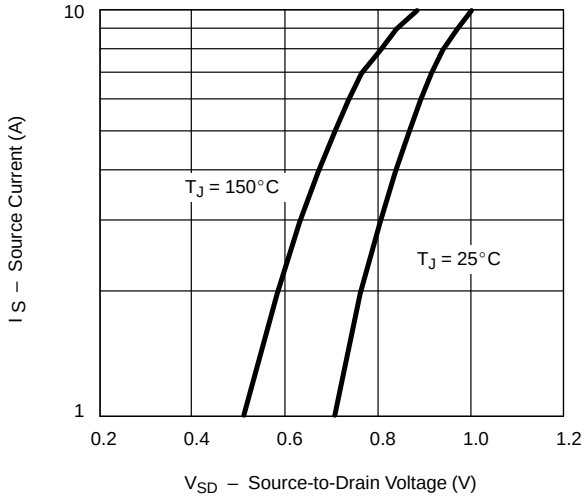
Gate Charge



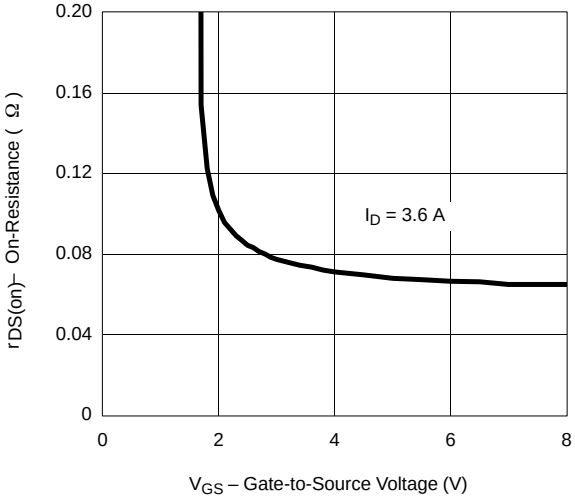
On-Resistance vs. Junction Temperature



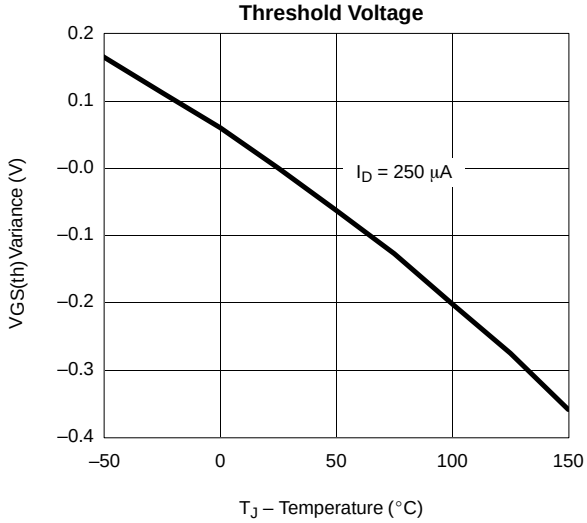
Source-Drain Diode Forward Voltage



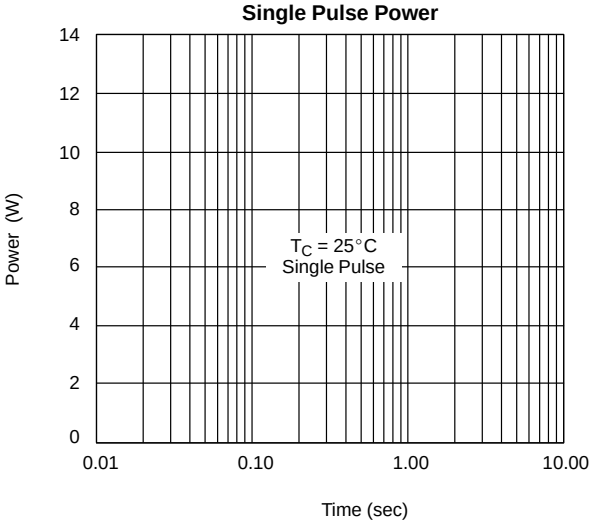
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient