



#### 20V N-Channel Enhancement Mode MOSFET - ESD Protected

Voltage

20 V

Current

1A

#### **Features**

- RDS(ON), VGS@4.5V, ID@1.0A<150mΩ</li>
- RDS(ON), VGS@2.5V, ID@0.7A<215mΩ</li>
- RDS(ON), VGS@1.8V, ID@0.3A<400mΩ</li>
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std.(Halogen Free)

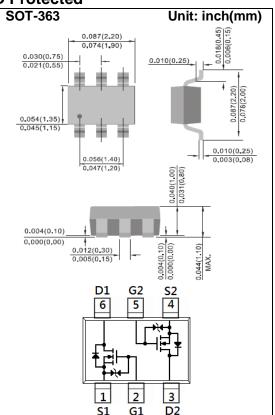
#### **Mechanical Data**

Case: SOT-363 Package

Terminals: Solderable per MIL-STD-750, Method 2026

Approx. Weight: 0.0002 ounces, 0.006 grams

Marking: T00



### **Maximum Ratings and Thermal Characteristics** (T<sub>A</sub>=25 °C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	<u>+</u> 8	V
Continuous Drain Current		I <sub>D</sub>	1	Α
Pulsed Drain Current (Note 4)		I <sub>DM</sub>	4	Α
Power Dissipation	T <sub>a</sub> =25°C	P <sub>D</sub>	350	mW
	Derate above 25°C		2.8	mW/°C
Operating Junction and Storage Temperature Range		$T_{J}, T_{STG}$	-55~150	°C
Typical Thermal resistance				
- Junction to Ambient (Note 3)		$R_{\theta JA}$	357	°C/W





## **Electrical Characteristics** (T<sub>A</sub>=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	-	1	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250uA$	0.5	0.8	1.0	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	$V_{GS}$ =4.5V, $I_D$ =1A	-	120	150	mΩ
		$V_{GS}$ =2.5V, $I_{D}$ =0.7A	-	160	215	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =0.3A	-	260	400	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ =20V, $V_{GS}$ =0V	-	0.01	1	uA
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\underline{+}8V, V_{DS}=0V$	-	<u>+</u> 2	<u>+</u> 10	uA
Dynamic <sup>(Note 5)</sup>						
Total Gate Charge	$Q_g$	V <sub>DS</sub> =10V, I <sub>D</sub> =1A, V <sub>GS</sub> =4.5V <sup>(Note 1,2)</sup>	-	1.6	-	nC
Gate-Source Charge	$Q_gs$		-	0.31	1	
Gate-Drain Charge	$Q_{gd}$		-	0.41	ı	
Input Capacitance	Ciss	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1.0MHZ	-	92	-	pF
Output Capacitance	Coss		-	25	-	
Reverse Transfer Capacitance	Crss	I=1.0IVIIIZ	-	9.1	-	
Turn-On Delay Time	td <sub>(on)</sub>	\/ 40\/   40	-	5.8	-	
Turn-On Rise Time	tr	$V_{DD}=10V, I_{D}=1A,$	-	25.8	-	ns
Turn-Off Delay Time	td <sub>(off)</sub>	$V_{GS}$ =4.5 $V$ , $R_G$ =6 $\Omega$ (Note 1,2)	-	42	-	
Turn-Off Fall Time	tf	K <sub>G</sub> =012	-	32	1	
Drain-Source Diode						
Maximum Continuous Drain-Source					1	A
Diode Forward Current	I <sub>S</sub>	3		-	ı	А
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =1.0A, V <sub>GS</sub> =0V	-	0.85	1.2	V

#### NOTES:

- 1. Pulse width<a></a>300us, Duty cycle<a></a>2%
- 2. Essentially independent of operating temperature typical characteristics.
- 3. R<sub>OJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper
- 4. The maximum current rating is package limited
- 5. Guaranteed by design, not subject to production testing.





#### TYPICAL CHARACTERISTIC CURVES

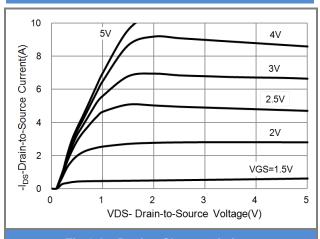
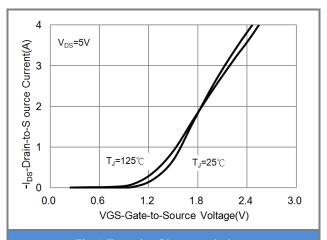


Fig.1 On-Region Characteristics



**Fig.2 Transfer Characteristics** 

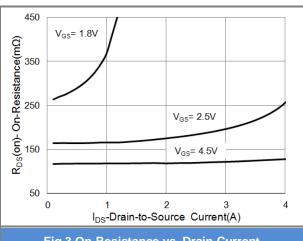


Fig.3 On-Resistance vs. Drain Current

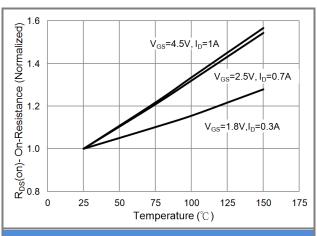
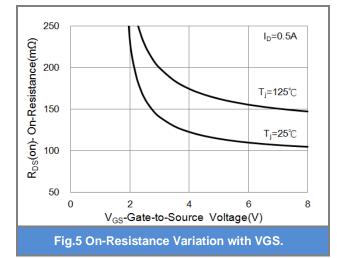
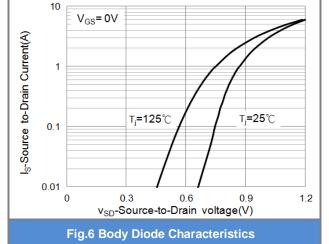


Fig.4 On-Resistance vs. Junction temperature

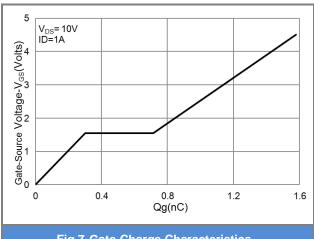








#### **TYPICAL CHARACTERISTIC CURVES**



**Fig.7 Gate-Charge Characteristics** 

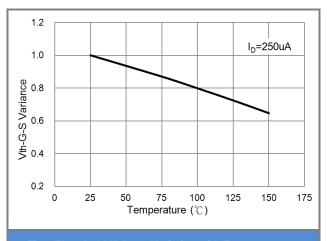


Fig.8 Threshold Voltage Variation with Temperature.

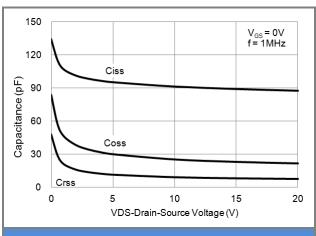


Fig.9 Capacitance vs. Drain-Source Voltage.

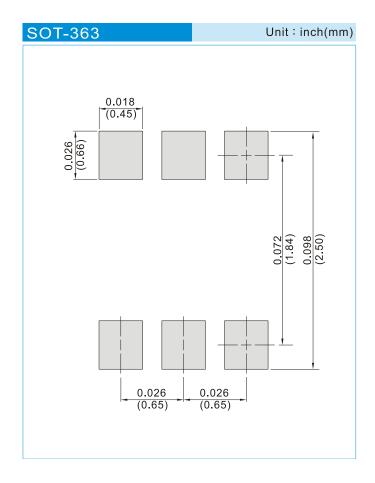




#### PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJT7800_R1_00001	SOT-363	3K pcs / 7" reel	T00	Halogen free
PJT7800_R2_00001	SOT-363	10K pcs / 13" reel	T00	Halogen free

#### **MOUNTING PAD LAYOUT**







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