



X-DPDT Switch for 0.4 to 3.8G Applications

Description

The MXD8546FA is a CMOS, Silicon-On-Insulator (SOI) double-pole, double-throw (DPDT) switch. The switch provides high linearity performance, low insertion loss and high isolation.

Switching is controlled by one control voltage. Depending on the logic voltage level applied to this pin, the RF1 and RF2 pins connect to one of the two other RF port pins (RF3 or RF4) through a low insertion loss path, while maintaining a high isolation path to the alternate port. No external DC blocking capacitors are required on the RF path as long as no DC voltage is applied externally.

The MXD8546FA DPDT switch is provided in a compact Quad Flat No-Lead (QFN) 2 x 2 mm package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 1 too. Signal pin assignments and functional pin descriptions are provided in Table 1.

Applications

- Simultaneous voice and LTE systems
- Diversity Antenna switching

Features

- Broadband frequency range: 0.4 to 3.8GHz
- Excellent insertion loss: 0.35dB @2.7GHz
- Input 0.1dB compression point: 39dBm
- Low harmonic generation
- High ESD robustness
- Wide power supply voltage range: 1.7 to 3.3V
- Positive control voltage range: 1.5V to VDD
- Small, QFN (12-pin, 2 x 2 mm) package, MSL1
- RoHS compliant package

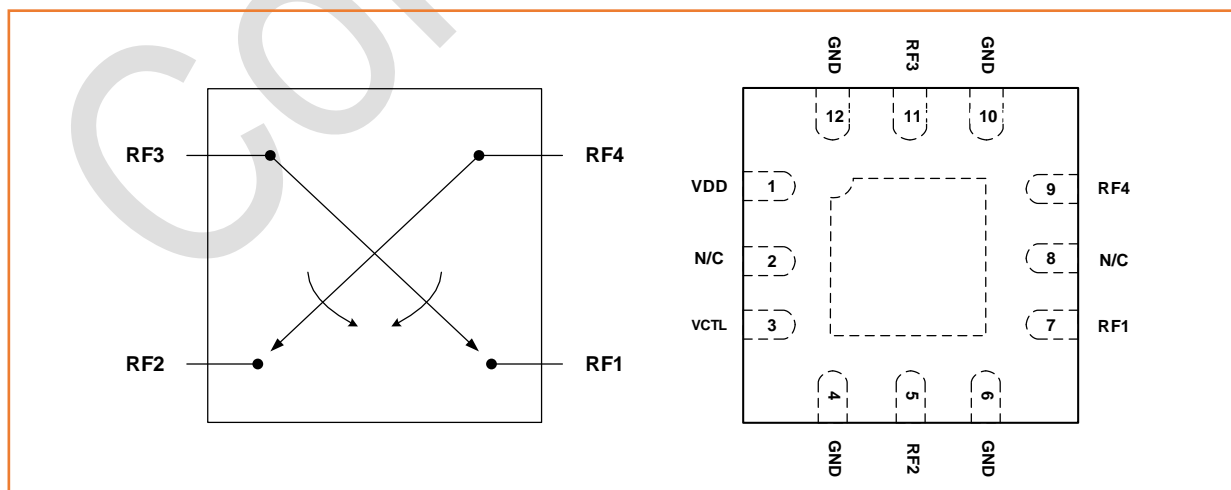


Figure 1 Functional Block and Pin Diagram

Function Characteristics

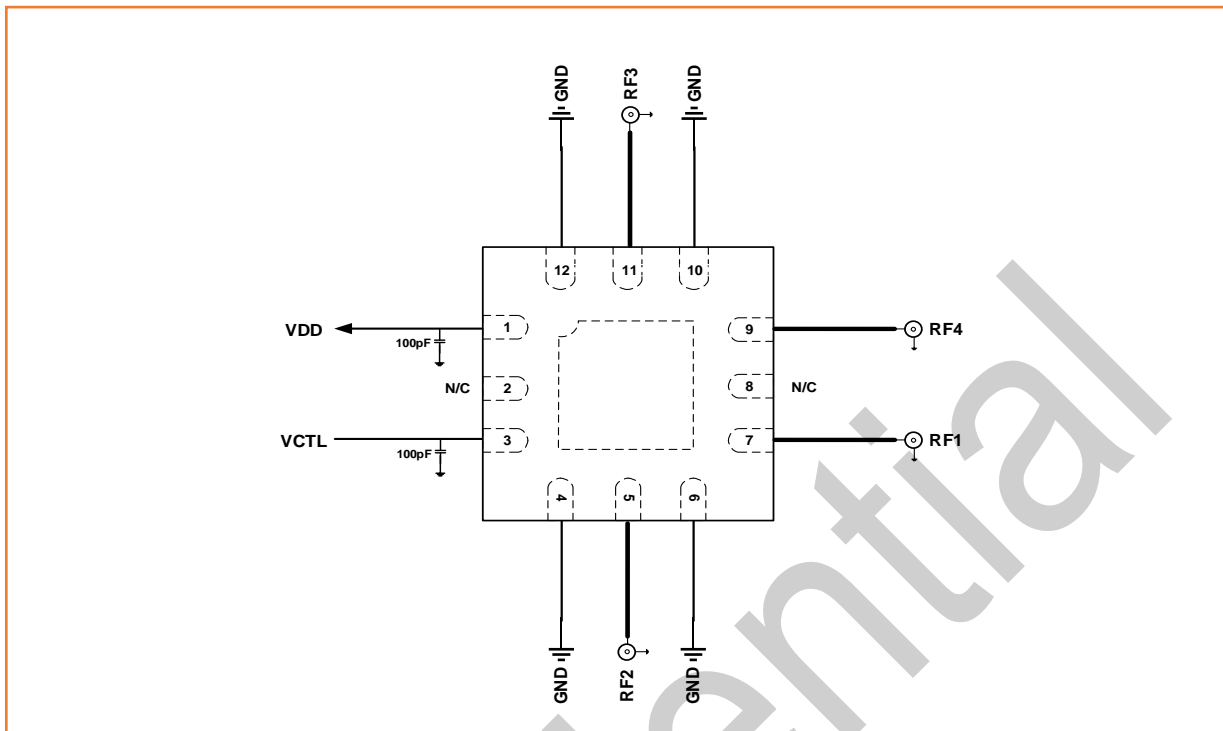


Figure 2 Application Circuit

Table 1 Pin Descriptions

No.	Name	Description	No.	Name	Description
1	VDD	DC Power Supply	7	RF1	RF Port1
2	N/C	Not Connected	8	N/C	Not Connected
3	VCTL	DC Control Pin	9	RF4	RF Port4
4	GND	Ground	10	GND	Ground
5	RF2	RF Port2	11	RF3	RF Port3
6	GND	Ground	12	GND	Ground

Table 2 VCTL Truth Table for RF Channel Operating Mode

VCTL	RF Channel Operating Mode
High	RF3 to RF1, RF4 to RF2
Low	RF3 to RF2, RF4 to RF1

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
DC Supply Voltage	V_{DD}	-0.3	3.6	V	$T_A=25^{\circ}\text{C}$
Logic Control Voltage	V_{CTL}	-0.3	3.6		$T_A=25^{\circ}\text{C}$
MAX RF Input Power (RF1/RF2/RF3/RF4 to GND)	P_{IN}		37	dBm	$F_0=950\text{MHz}$, 20% DC, $Z_0=50\Omega$, $V_{DD}=2.8\text{V}$, $T_A=25^{\circ}\text{C}$
	P_{IN}		39		$F_0=950\text{MHz}$, CW, $Z_0=50\Omega$, $V_{DD}=2.8\text{V}$, $T_A=25^{\circ}\text{C}$
Device Operating Temperature	T_{OP}	-40	90	$^{\circ}\text{C}$	
Device Storage Temperature	T_{STG}	-55	150		
Electrostatic Discharge (All Pins)	$V_{ESD(HBM)}$	1000		V	Human Body Model
	$V_{ESD(CDM)}$	500			Charged Device Model

Notice

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	0.4		3.8	GHz
DC Supply Voltage	V_{DD}	1.7	2.8	3.3	V
Control Voltage High	V_{CTLH}	1.5	1.8	VDD	V
Control Voltage Low	V_{CTLL}	0	0	0.3	V

Table 5 Nominal Operating Parameters

Parameter	Symbol	Specification			Unit	Condition
		MIN	TYP	MAX		
Normal Condition	$V_{DD}=2.8V, V_{CTLH}=1.8V, V_{CTL}=0V, P_{IN}=0dBm, Z_0=50\Omega, T_A=25^\circ C$, Unless Otherwise Stated					
DC Performances						
DC Supply Current	I_{DD}		90	120	uA	
Current on VCTL	I_{CTL}		1	5		
Timing Performances						
Startup Time	T_{ON}			10	us	50% of VDD to 90% of RF power
RF Path Switching Time	T_{SW}		2	3		50% of VCTL to 90% of RF power
RF Performances						
Insertion Loss (RF1/RF2 to RF3/RF4)	IL		0.26	0.30		$F_0=0.4$ to 1.0GHz
			0.30	0.35		$F_0=1.1$ to 2.2GHz
			0.35	0.40		$F_0=2.5$ to 2.7GHz
			0.42	0.50		$F_0=3.4$ to 3.8GHz
Isolation (RF1/RF2 to RF3/RF4, RF1 to RF2, RF3 to RF4)	ISO	30	33		dB	$F_0=0.4$ to 1.0GHz
		25	30			$F_0=1.1$ to 2.2GHz
		21	25			$F_0=2.5$ to 2.7GHz
		16	18			$F_0=3.4$ to 3.8GHz
Input Return Loss (RF1/RF2 to RF3/RF4)	RL	10	15			$F_0=0.4$ to 3.8GHz
Input 0.1dB Compression Point(RF1/RF2 to RF3/RF4)	$P_{0.1dB}$		39		dBm	$F_0=950MHz$, 20% DC
2nd Order Harmonic (RF1/RF2 to RF3/RF4)	$2F_0$		-95	-85	dBc	$F_0=824$ to 915MHz @35dBm
3rd Order Harmonic (RF1/RF2 to RF3/RF4)	$3F_0$		-95	-85		$F_0=824$ to 915MHz @35dBm
2nd Order Intermodulation	IMD2		-115	-110	dBm	Reference to Table 6
3rd Order Intermodulation	IMD3		-115	-110		Reference to Table 7

Table 6 IMD2 Test Conditions

Band	In-Band Frequency	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 Low	2140	1950	20	190	-15
1 High	2140	1950	20	4090	-15
5 Low	881.5	836.5	20	45	-15
5 High	881.5	836.5	20	1718	-15

Table 7 IMD3 Test Conditions

Band	In-Band Frequency	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 LOW	2140	1950	20	1760	-15
5 HIGH	881.5	836.5	20	791.5	-15

Package Outline Dimensions

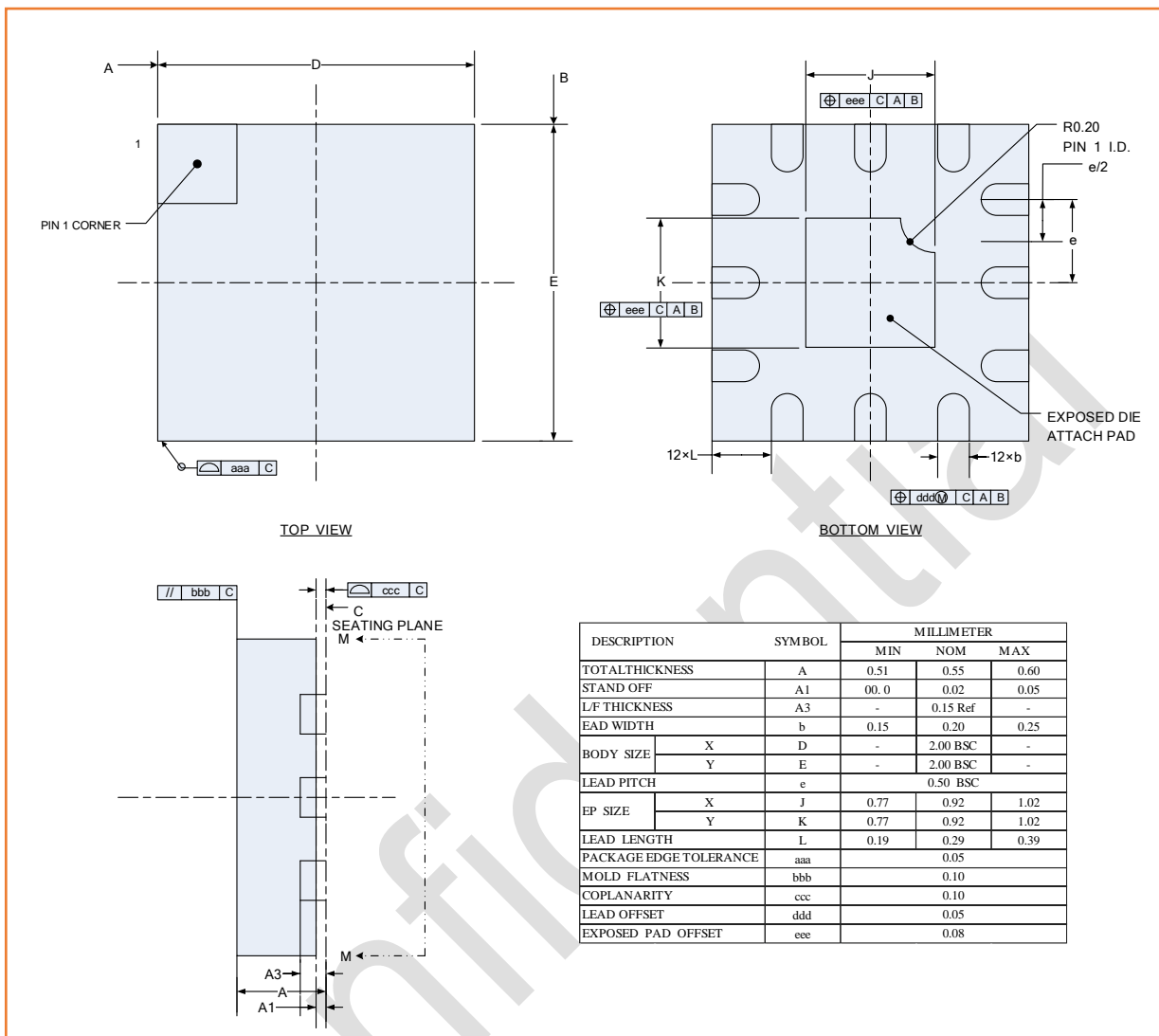


Figure 3 Package Outline Dimension

Marking Specification

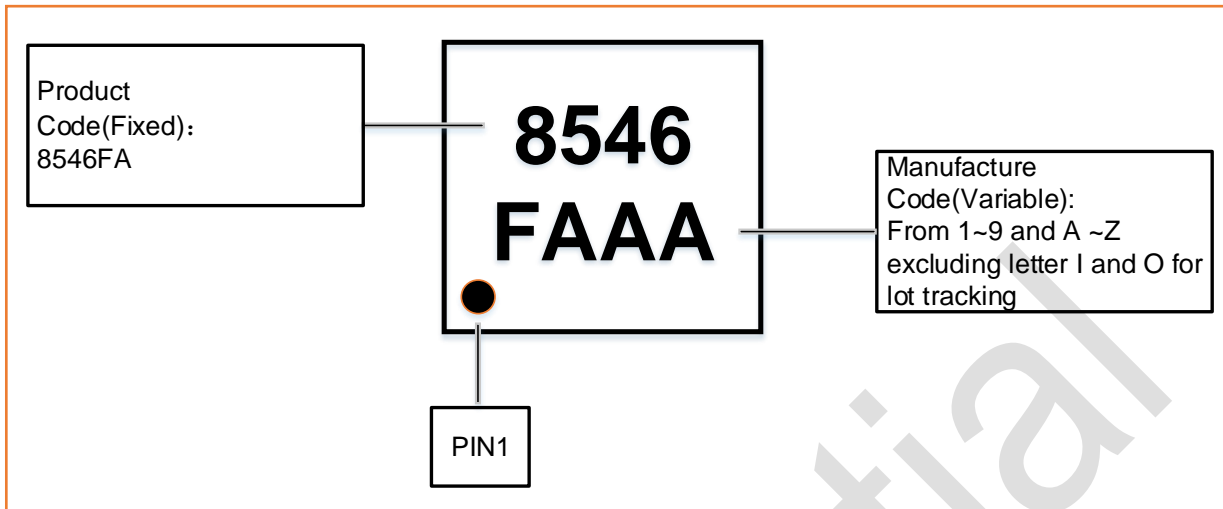


Figure 4 Marking Specification(Top View)

Tape and Reel Dimensions

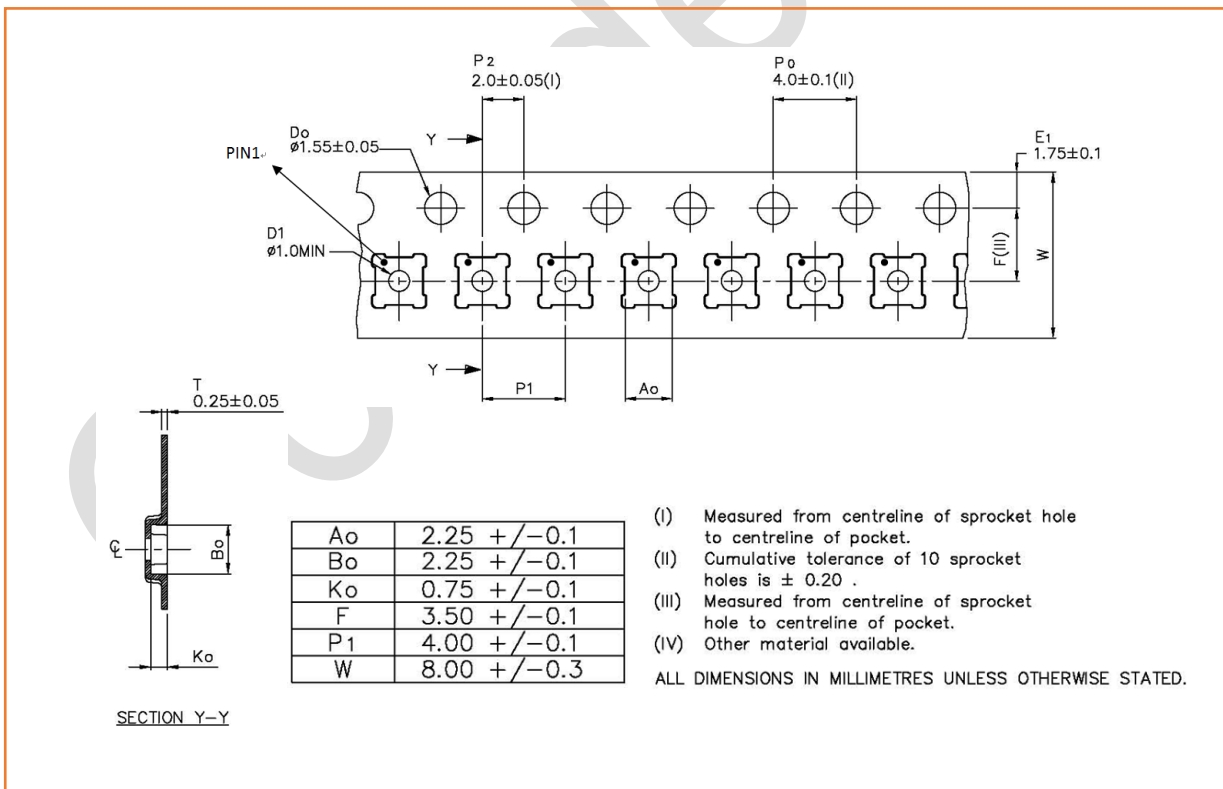


Figure 5 Tape and Reel Dimensions

Reflow Chart

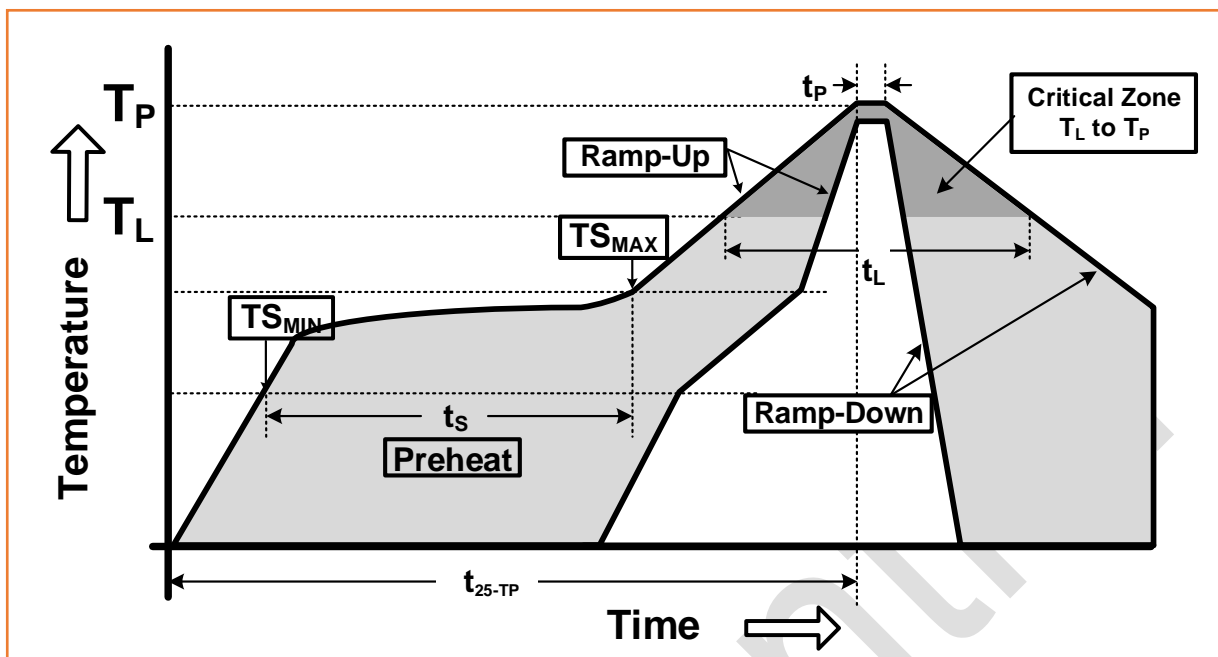


Figure 6 Recommended Lead-Free Reflow Profile

Table 8 Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(TS_{MIN} to TS_{MAX})	150°C to 200°C
Preheat Time(t_s)	60 to 180 Seconds
Ramp-Up Rate(TS_{MAX} to T_P)	3°C/s MAX
Time Above T_L 217°C(t_L)	60 to 150 Seconds
Peak Temperature (T_P)	260°C
Time within 5°C of Peak Temperature(t_p)	20 to 40 Seconds
Ramp-Down Rate(TS_{MAX} to T_P)	6°C/s MAX
Time for 25°C to Peak Temperature(t_{25-TP})	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operating.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and is considered RoHS compliant.