QC 11 APPROVED

0.4~3.8GHz 3xSPST Antenna Tuning Switch

Description

The MXD8533B is a CMOS silicon-on-insulator (SOI), three single-pole, single-throw (3xSPST) switch. The high linearity and ruggedness performance and extremely low R_{ON} and C_{OFF} makes the device an ideal choice for GSM/WCDMA/LTE handset antenna tuning application.

The MXD8533B 3xSPST switch is provided in a compact 1.75mm x 1.66mm x 0.37mm package. A functional block diagram, the pin configuration and package are shown in Figure 1. Signal pin assignments and functional pin descriptions are provided in Table 1.

Features

- Broadband frequency range: 0.4 to 3.8 GHz
- Input 0.1dB Compression Point: 48dBm
- RFFE serial control interface
- No DC blocking capacitors required
- Ultra small package, LGA 11-pin (1.75mm x 1.66mm x 0.37mm), MSL1

Applications

- GSM/WCDMA/LTE band and mode switching
- Antenna tuning switching

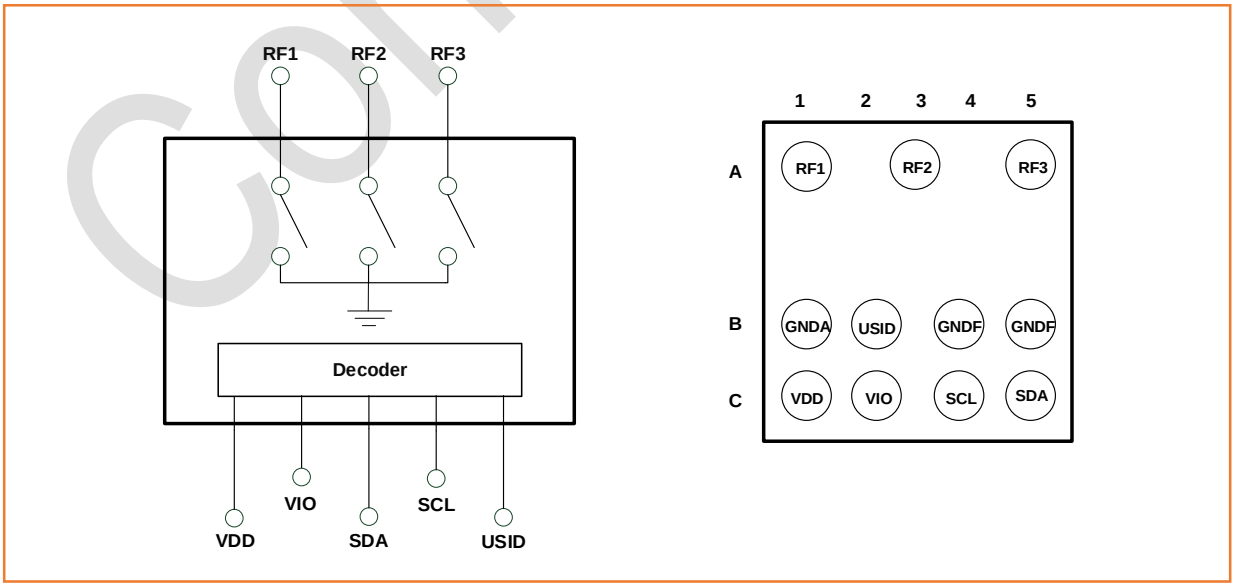


Figure 1 Functional Block Diagram

Function Characteristics

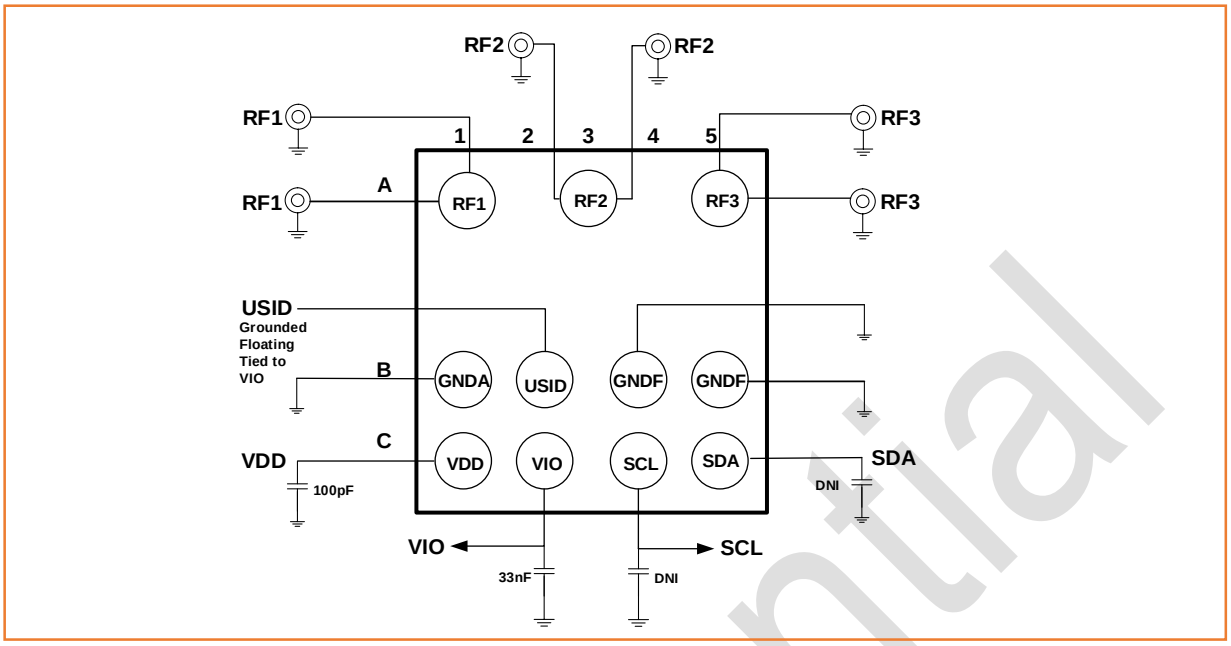


Figure 2 Application Circuit

Table 1 Pin Descriptions

NO.	Name	Description	NO.	Name	Description
A1	RF1	RF Port1	B5	GNDF	RF Ground
A3	RF2	RF Port2	C1	VDD	DC Supply Voltage
A5	RF3	RF Port3	C2	VIO	Supply Voltage for MIPI
B1	GNDA	Analog Ground	C4	SCL	MIPI Clock
B2	USID	Unique Salve ID	C5	SDA	MIPI Data Input/output
B4	GNDF	RF Ground			

Table 2 Register_0[7:0] (MIPI Data) for RF Operating Mode

State	Mode	Register_0							
		D7	D6	D5	D4	D3	D2	D1	D0
1	All On	0	0	0	0	0	1	1	1
2	RF1 On	0	0	0	0	0	1	0	0
3	RF2 On	0	0	0	0	0	0	1	0
4	RF3 On	0	0	0	0	0	0	0	1
5	RF1+RF2 On	0	0	0	0	0	1	1	0
6	RF1+RF3 On	0	0	0	0	0	1	0	1
7	RF2+RF3	0	0	0	0	0	0	1	1
8	All Off	0	0	0	0	0	0	0	0

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	-0.3	3.6	V
Supply Voltage for MIPI	V_{IO}	-0.3	+2.5	
MIPI Control Voltage(SDA, SCL)	V_I	-0.3	+2.5	
RF Input Peak Power(VSWR 1:1,20% DC)	P_{IN}		+48.5	dBm
Device Operating Temperature	T_{OP}	-40	+90	℃
Device Storage Temperature	T_{STG}	-55	+150	
Electrostatic Discharge				
Human Body Model (HBM), Class 1C	$V_{ESD(HBM)}$	1000		V
Charged Device Model (CDM), Class III	$V_{ESD(CDM)}$	500		

Notice

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	0.4		3.8	GHz
DC Supply Voltage	V_{DD}	1.7	2.8	3.3	V
Power Supply for MIPI	V_{IO}	1.62	1.8	1.98	
MIPI Control Voltage(SDA, SCL) High	V_{IH}	0.8*VIO	VIO	VIO	
MIPI Control Voltage(SDA, SCL) Low	V_{IL}	0	0	0.3	

Table 5 Nominal Operating Parameters

Parameter	Symbol	Specification MIN	TYP	MAX	Unit	Condition
Normal Condition	V_{DD}=2.8V, V_{IO}=1.8V, V_{IH}=1.8V, V_{IL}=0V, P_{IN}=0dBm, Z_O=50Ω, T_A=25℃, Unless Otherwise Stated					
DC Performances						
DC Supply Current	I_{DD}		100	200	μA	
Current on VIO	I_{IO}		5	10	μA	
Timing Performances						
Switching Speed	T_{SW}		15	25	μs	End of MIPI Command to 90%/10% RF
Startup Time	T_{ON}		30		μs	MIPI Low Power State to any RF
RF Performances						
Isolation (All off mode, RFx to RFy)	ISO	40 35 33 29	45 38 36 32		dB	F_0=0.8 to 1.0GHz F_0=1.0 to 2.2GHz F_0=2.2 to 3.0GHz F_0=3.4 to 3.8GHz
On Resistance	R_{ON}		1.9	2.0	Ω	Switch on Path @DC
OFF Capacitance	C_{OFF}		100	120	fF	Switch off Path @500MHz
Input 0.1dB Compression Point	$P_{0.1dB}$		+48		dBm	F_0=950MHz, 20% DC
Peak RF Operating Voltage	V_{RF}		80		V	F_0=950MHz, until $3F_0$ Nonlinear Isolation Mode
LTE TX Harmonic	$2F_0$	-70	-85		dBm	F_0=700 to 2700MHz @+26dBm
	$3F_0$	-70	-85		dBm	
GSM LB Harmonic	$2F_0$	-55	-65		dBm	F_0=824 to 915MHz @+35dBm
	$3F_0$	-55	-65		dBm	
GSM HB Harmonic	$2F_0$	-55	-65		dBm	F_0=1710 to 2690MHz @+33dBm
	$3F_0$	-55	-65		dBm	
2nd Order Intermodulation	IMD2	-105	-115		dBm	Reference to Table 6
3rd Order Intermodulation	IMD3	-105	-115		dBm	Reference to Table 7

Table 6 IMD2 Test Conditions

Band	In-band Frequency	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 Low	2140	1950	+20	190	-15
1 High	2140	1950	+20	4090	-15
5 Low	881.5	836.5	+20	45	-15
5 High	881.5	836.5	+20	1718	-15

Table 7 IMD3 Test Conditions

Band	In-band Frequency	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 LOW	2140	1950	+20	1760	-15
5 HIGH	881.5	836.5	+20	791.5	-15

MIPI Read and Write Timing

MIPI supports the following Command Sequences:

- Register Write
- Register Read
- Register_0 Write

Figure 3 and Figure 4 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 5 describes the Register_0 write command sequence.

Other information such as MIPI USID programming sequences, MIPI bus specifications, etc. can be referred to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V1.10 (26 July 2011) and the subsequent versions.

In the below timing figures, SA[3:0] is the slave address. A[4:0] denotes the register address. D[7:0] means the data. “P” is a parity bit.

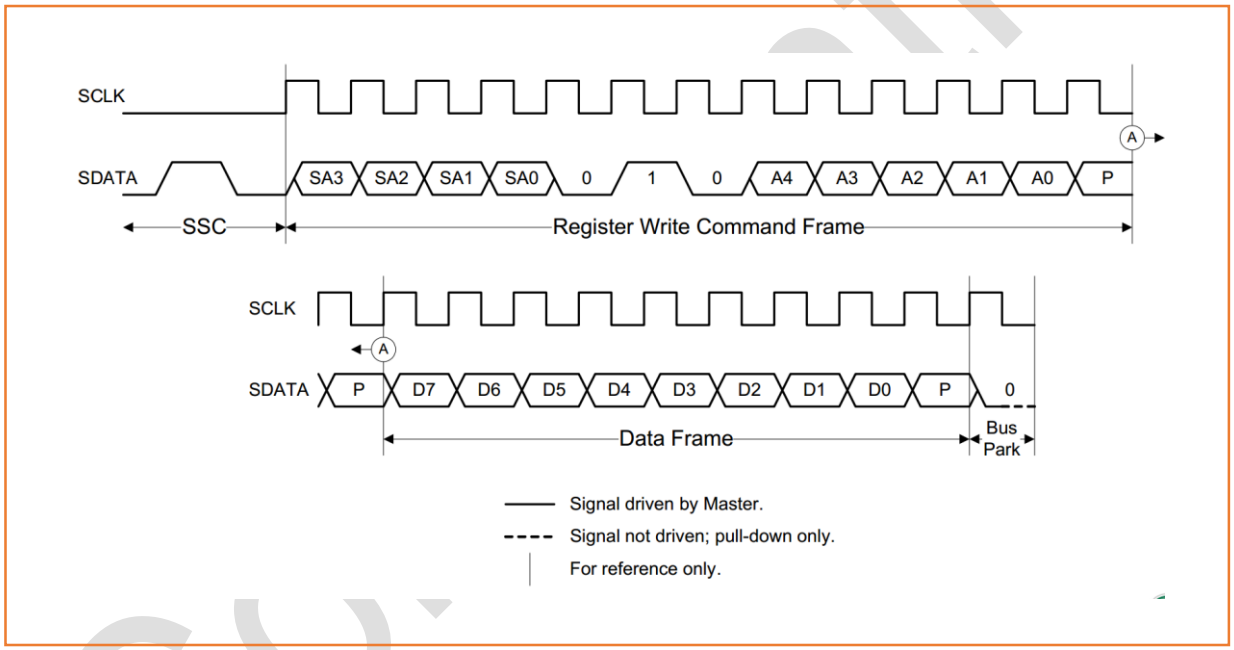


Figure 3 Register Write Command Sequence

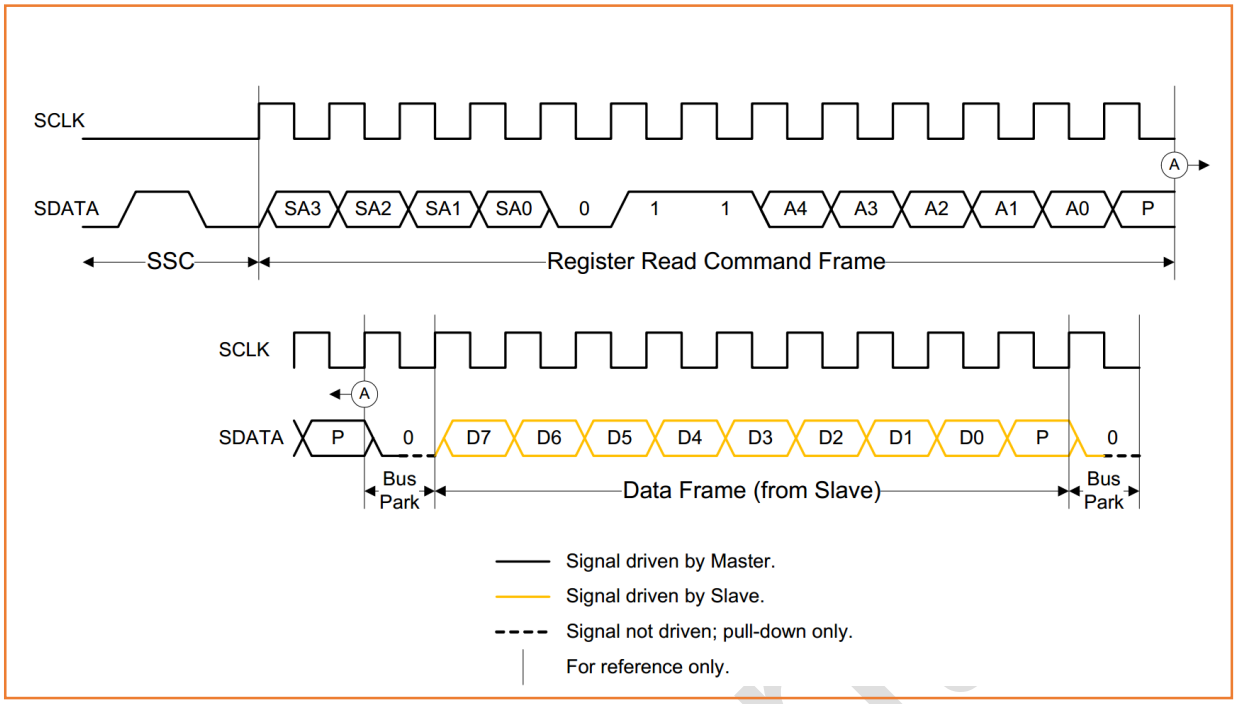


Figure 4 Register Read Command Sequence

Register_0 Write Command Sequence

Figure 5 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and a 7-bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle

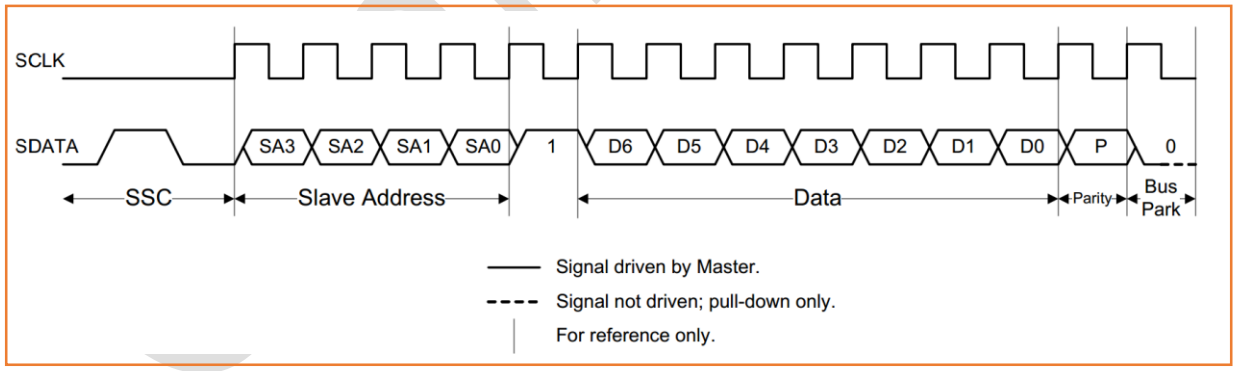


Figure 5 Register_0 Write Command Sequence

Register Definition

Table 8 Register definition table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x0000	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table: Table 2	0x00	No	Yes
0x001A	RFFE_STATUS	7	R/W	SOFTWARE RESET	0: Normal operation 1: Software reset Note: On software reset, this register and all configurable registers are reset except for USID, GSID, and PM_TRIG.	0b0	No	No
		6	R/W	COMMAND_FRAME_PARITY_ERR	Command Frame with parity error	0b0	No	No
		5	R/W	COMMAND_LENGTH_ERR	Command Sequence with incorrect length	0b0	No	No
		4	R/W	ADDRESS_FRAME_PARITY_ERR	Address Frame with parity error	0b0	No	No
		3	R/W	DATA_FRAME_PARITY_ERR	Data Frame with parity error	0b0	No	No
		2	R/W	READ_UNUSED_REG	Read Command Sequence to an invalid address	0b0	No	No
		1	R/W	WRITE_UNUSED_REG	Write Command Sequence to an invalid address	0b0	No	No
		0	R/W	BID_GID_ERR	Read Command Sequence with a BSID or GSID Note: Reading this register resets this register.	0b0	No	No
0x001B	GROUP_SID	7:4	R	RESERVED		0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
0x001C	PM_TRIG	7:6	R/W	PWR_MODE	00: Normal Operation (ACTIVE) 01: Reset all registers to default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved Note: Write PWR_MODE[1:0]=0b01 will reset all register, and then automatically put the device into ACTIVE state.	0b00	Yes	No
		5	R/W	Trigger_Mask_2	If this bit is set, trigger 2 is disabled	0b0	No	No

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
		4	R/W	Trigger_Mask_1	If this bit is set, trigger 1 is disabled	0b0	No	No
		3	R/W	Trigger_Mask_0	If this bit is set, trigger 0 is disabled Note: When all triggers are disabled, writing to a register that is associated with trigger 0, 1, or 2, causes the data to go directly to the destination register.	0b0	No	No
		2	W	Trigger_2	A write of a one to this bit loads trigger 2's registers	0b0	Yes	No
		1	W	Trigger_1	A write of a one to this bit loads trigger 1's registers	0b0	Yes	No
		0	W	Trigger_0	A write of a one to this bit loads trigger 0's registers Note: Trigger processed immediately then cleared. Trigger 0, 1, and 2 will always read as 0.	0b0	Yes	No
0x001D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x34	No	No
0x001E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x81	No	No
0x001F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0b11	No	No
		3:0	R/W	USID	User Identification, with USID tied to GND	0x6	No	No
					User Identification, with USID floated	0x7	No	No
					User Identification, with USID tied to VIO	0x9	No	No

Power On and Off Sequence

Here is the recommendation for power-on and power-off sequence in order to avoid damaging to the device.

Power On

1) Apply voltage supply - VDD
2) Apply logic supply - VIO
3) Wait 30μs or longer and then apply MIPI bus signals – SCL and SDA
4) Wait 25μs or longer after MIPI bus goes idle and then apply the RF Signal

Power Off

1) Remove the RF Signal
2) Remove MIPI bus – SCL and SDA
3) Remove logic supply - VIO
4) Remove voltage supply - VDD

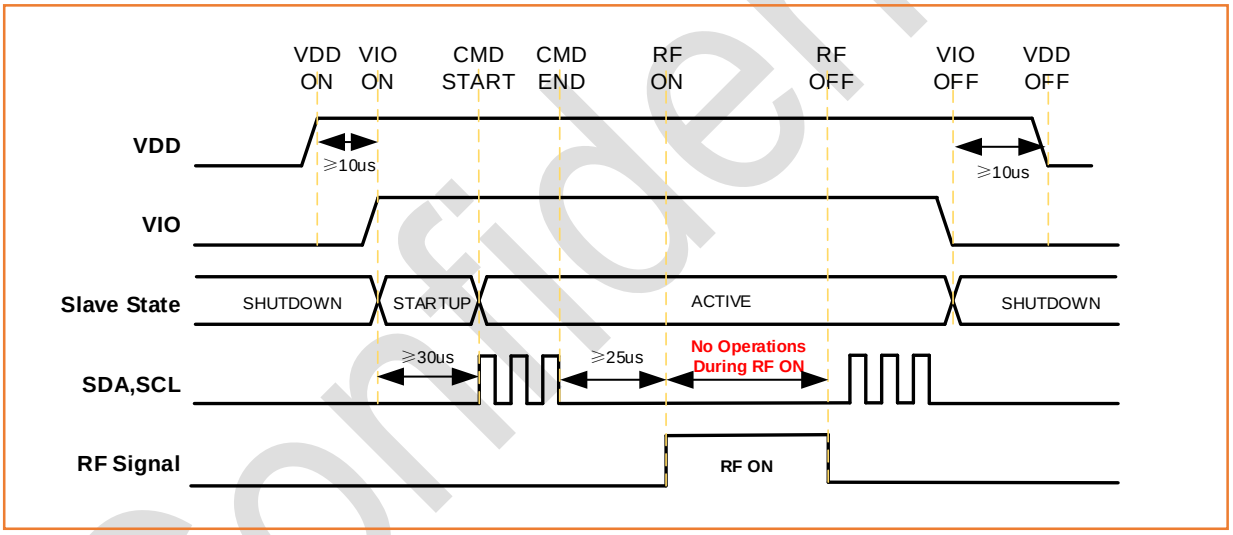
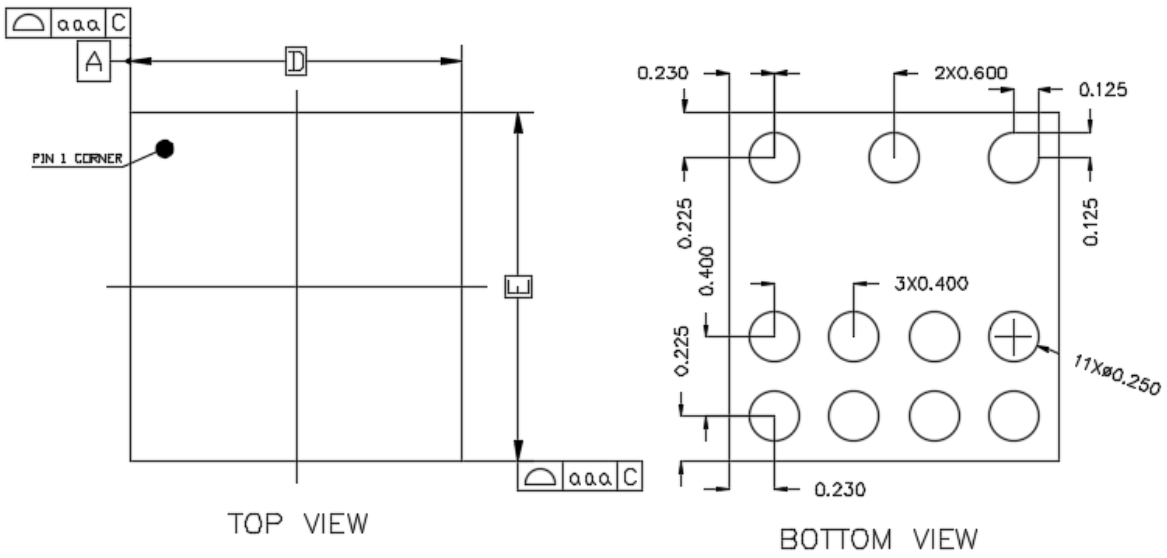


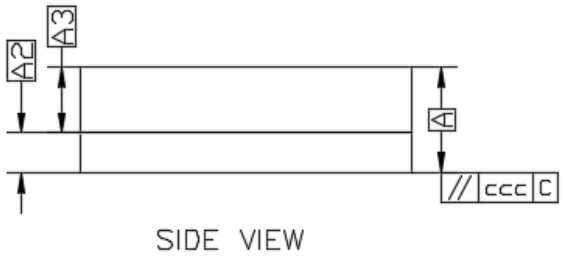
Figure 6 Power On and Off Sequence

Notice

- *VIO can also be applied to the device before VDD or removed after VDD.*
- *It is important not to send any SDA until a 10us or longer waiting time following the VDD and VIO startup to ensure corrective data transmission.*
- *Operations of SDA or SCL are strictly prohibited during RF On period so as to prevent the device being damaged.*
- *The minimum time between a power up and power down sequence (and vice versa) shall be 100us or longer.*

Package Outline Dimensions





SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	0.340	0.370	0.400
A2	---	0.130	---
A3	---	0.240	---
D	1.620	1.660	1.700
E	1.700	1.750	1.800
e	0.400		
aaa	0.100		
ccc	0.050		

Figure 7 Package Outline Dimensions

Marking Specification

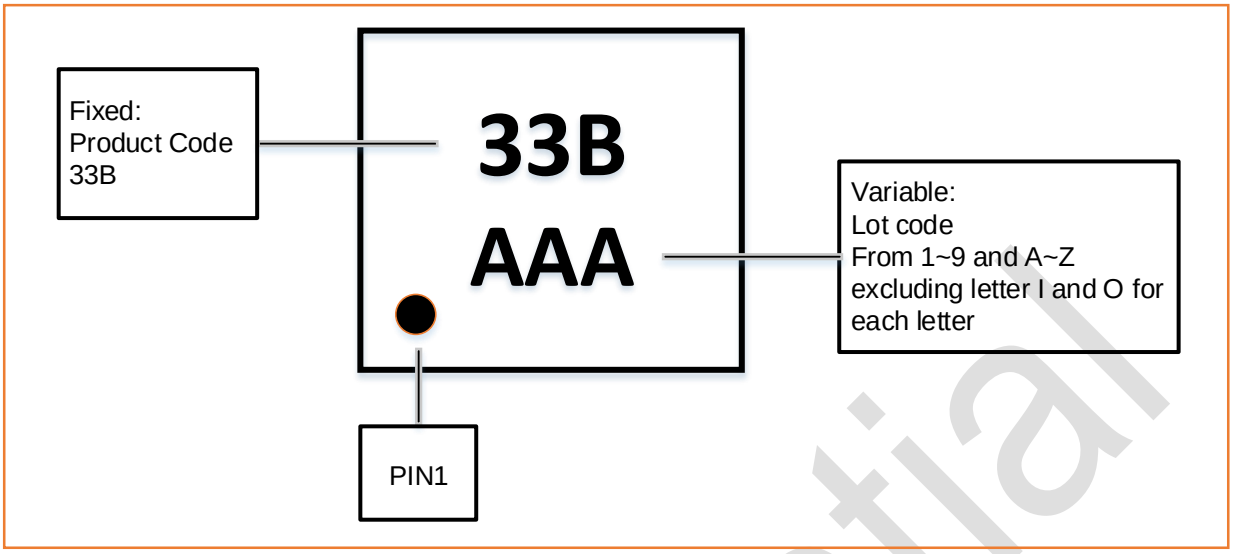
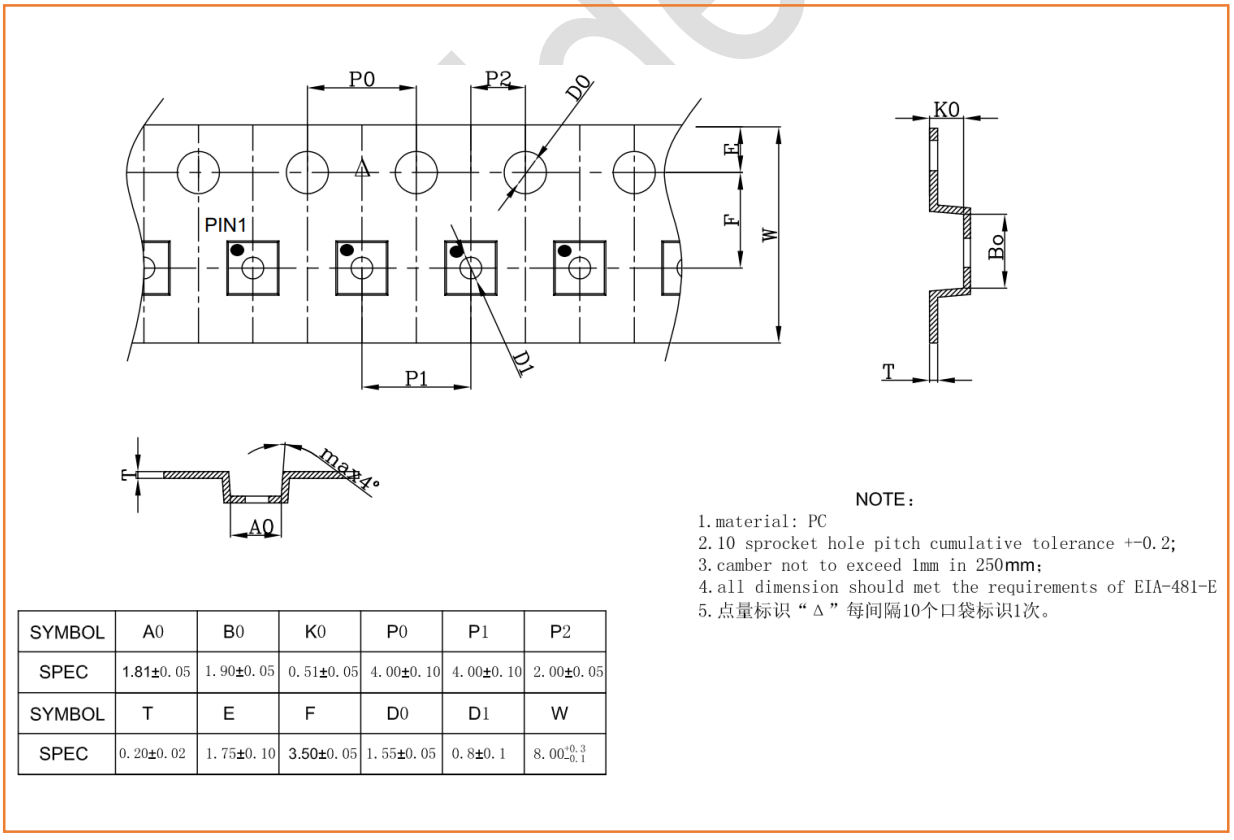


Figure 8 Marking Specification (Top View)

Tape and Reel Dimensions



SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	1.81±0.05	1.90±0.05	0.51±0.05	4.00±0.10	4.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.20±0.02	1.75±0.10	3.50±0.05	1.55±0.05	0.8±0.1	$8.00^{+0.3}_{-0.1}$

NOTE:
1. material: PC
2. 10 sprocket hole pitch cumulative tolerance +-0.2;
3. camber not to exceed 1mm in 250mm;
4. all dimension should met the requirements of EIA-481-E
5. 点量标识“Δ”每间隔10个口袋标识1次。

Figure 9 Tape and Reel Dimensions

Reflow Chart

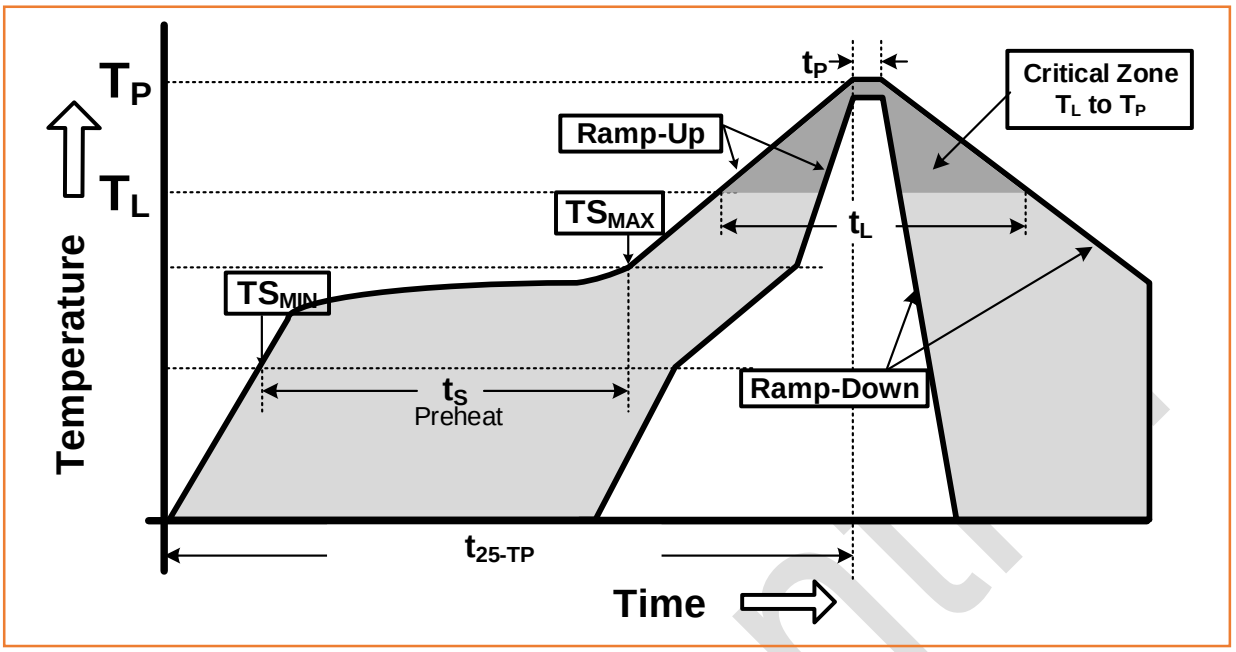


Figure 10 Recommended Lead-Free Reflow Profile

Table 9 Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(TS_{MIN} to TS_{MAX})	150℃ to 200℃
Preheat Time(ts)	60 to 180 Seconds
Ramp-Up Rate(TS_{MAX} to T_P)	3℃/s MAX
Time Above T_L 217℃(t_L)	60 to 150 Seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of Peak Temperature(t_P)	20 to 40 Seconds
Ramp-Down Rate(TS_{MAX} to T_P)	6℃/s MAX
Time for 25℃ to Peak Temperature($t_{25\text{-}TP}$)	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.