Transition-Mode PFC and Quasi-Resonant Current Mode PWM Controller

REV: 04

General Description

The LD7791/A/B/C features transition mode Power Factor correction (PFC) controller and Quasi-Resonant (QR) current mode controller for cost effective and fewer external components design of high power application.

The intelligent PFC switching ON/OFF, zero current detection (ZCD) and frequency limitation mechanism enable it to reach better efficiency under any load conditions.

The device also integrates several functions of protection, such as X-CAP discharge, Brown-in/out protection, Over Load protection (OLP), Over Temperature Protection (OTP), Over Voltage Protection (OVP) and Over Current Protection (OCP) with High / Low Line Compensation. Therefore it can protect the system from being damaged due to occasional failure.

The LD7791/A/B/C is available in a SOP-16 package.

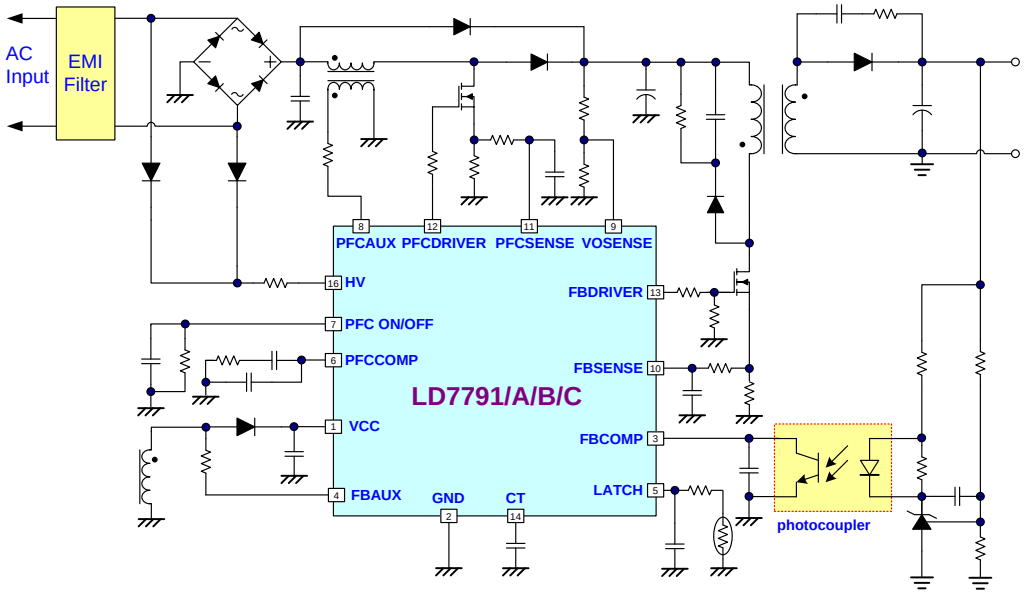
Features

- Integrate PFC and QR Flyback Controller
- Transition Mode PFC Controller
- Quasi-Resonant Operation for Flyback
- Built-in X-CAP Discharging
- Brown In/Out Protection
- Internal Soft-Start Function
- Adjustment OLP De-bounce time
- External Latch Protection
- PFC Light Load Turn-off Control
- OVP (Over Voltage Protection)
- OCP (Cycle by cycle current limiting)
- 500mA/-1200mA Driving Capability
- Internal OTP function

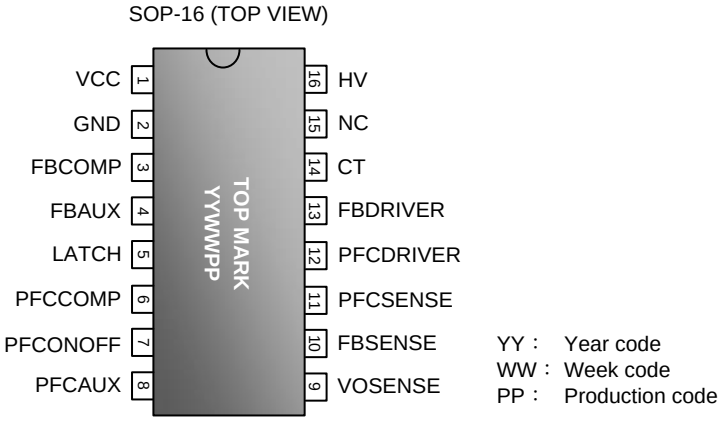
Applications

- AC-DC High Power Adapter
- Open Frame SMP

Typical Application



Pin Configuration



Ordering Information

Part number	Package	Top Mark	Shipping
LD7791 GS	SOP-16	LD7791 GS	2500 /tape & reel
LD7791A GS	SOP-16	LD7791A GS	2500 /tape & reel
LD7791B GS	SOP-16	LD7791B GS	2500 /tape & reel
LD7791C GS1	SOP-16	LD7791C GS1	2500 /tape & reel

The LD7791/A/B/C is ROHS compliant/ green packaged.

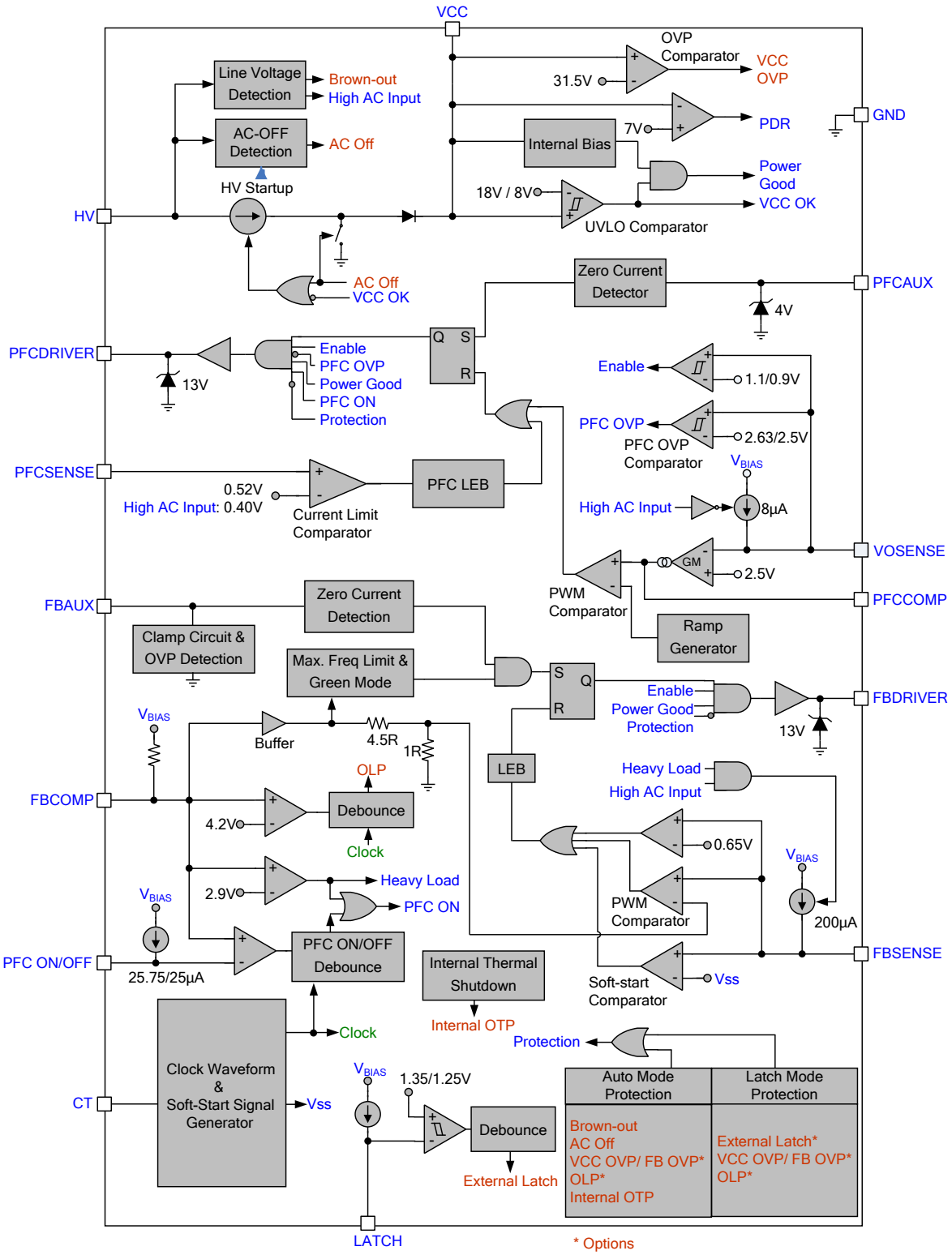
Options & Protection Mode

Product Name	PFC Turn-off De-bounce (CT w/ 47nF)	Flyback burst Mode trip	Brown-in Level	OVP (VCC & FBAUX)	OLP	External Latch	Internal OTP
LD7791	1sec	On: 0.8V Off: 0.6V	105	Auto	Auto	Latch	Auto
LD7791A	1sec	On: 0.8V Off: 0.6V	105	Latch	Auto	Latch	Auto
LD7791B	8sec	On: 1.1V Off: 0.9V	102	Latch	Latch	Latch	Auto
LD7791C	1sec	On: 0.8V Off: 0.6V	105	Latch	Auto	Auto	Auto

Pin Descriptions

Pin	NAME	FUNCTION
1	VCC	Supply voltage pin.
2	GND	Ground.
3	FBCOMP	Voltage feedback pin for flyback stage. Connect a photo-coupler to close the control loop and achieve the regulation.
4	FBAUX	Zero current detection and over voltage protection for flyback stage.
5	LATCH	External latch protection pin.
6	PFCCOMP	Output of the error amplifier for PFC voltage loop compensation.
7	PFCONOFF	Threshold voltage setting of FBCOMP for PFC ON/OFF loading control.
8	PFCAUX	Zero current detection for PFC stage.
9	VOSENSE	Voltage sense for PFC output, regulation voltage is 2.5V.
10	FBSENSE	Current sense pin. Connect it to sense the Flyback MOSFET current.
11	PFCSENSE	Current sense pin. Connect it to sense the PFC MOSFET current.
12	PFCDRIVER	Gate drive output to drive the external MOSFET for PFC.
13	FBDRIVER	Gate drive output to drive the external MOSFET for Flyback.
14	CT	Timer setting for Open Loop Protection, PFC light-load turn-off and flyback soft-start.
15	NC	Unconnected Pin.
16	HV	Connect this pin to Line/Neutral of AC main voltage through a resistor to provide the startup current for the controller. When VCC voltage increases to trip the point of UVLO(ON), this HV loop will be turned off to reduce the power loss over the startup circuit. HV pin Internal circuit will detect the AC peak voltage, providing Brown in/out and High / Low Line Detection function. HV pin internal circuit will discharge X-CAP's energy through HV current source when AC line is disconnected.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3V~ VCC OVP
HV	-0.3V~ 500V
FBCOMP, PFCCOMP, FBSENSE, PFCSENSE, FBAUX, PFCAUX, VOSENSE, LATCH, CT, PFCONOFF	-0.3V ~ 6V
FBDRIVER, PFCDRIVER	-0.3V ~ VCC+0.3V
Power Dissipation	600mW
Package Thermal Resistance SOP-16, θ_{JA}	110°C/W
Package Thermal Resistance SOP-16, θ_{JC}	36°C/W
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec)	260°C
Storage Temperature Range	-55°C ~ 150°C
ESD Voltage Protection, Human Body Model, (Pin 3~11 and Pin 14)	3.5KV
ESD Voltage Protection, Human Body Model, (Pin 1, 12, 13)	2.5KV
ESD Voltage Protection, Human Body Model, (Pin 16)	1.0KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
Gate Output Current	+500mA/-1200mA

Recommended Operating Conditions

Supply Voltage VCC	10V ~ 29.5V
VCC Capacitor	47µF ~ 100µF
HV Pin Resistor	10 kΩ ~ 50kΩ
FBCOMP Capacitor Value	1nF ~10nF
VOSENSE Capacitor Value	1nF ~10nF
PFCAUX Pin Resistor	10kΩ ~ 30kΩ
PFCAUX Sink and Source Current Setting	1mA
Operating Ambient Temperature	-40°C ~ 85°C
Operating Junction Temperature Range	-40°C ~ 125°C

Note:

1. It's essential to connect COMP pin with a capacitor to filter out the undesired switching noise for stable operation.
2. Place the small signal components closed to IC pin as possible.

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)							
High-Voltage Current Source for VCC Startup	VCC < PDR, VHV = 80V		I_{HV1}	1.20	1.50	1.80	mA
	VCC > PDR, VHV = 80V		I_{HV3}	2.00	3.00	4.00	mA
Off-State Leakage Current	After UVLO(ON), VHV = 500V		$I_{HVOFF500}$			32	μA
Line Voltage Detection (HV Pin)							
X-CAP Discharge Current*			I_{HVXCAP}		3		mA
Brown-in Level		LD7791/A/C	V_{BNI}	98	105	112	V
		LD7791B			102		
Brown-out Level			V_{BNO}	89	95	101	V
Brown-in – Brown-Out Level*		LD7791/A/C	V_{BNHYS}		10		V
		LD7791B			7		
Brown-Out Debounce Time *			T_{DBNO}	500	570		ms
High Line Trip Level			V_{HLINE}			220	V
Low Line Trip Level			V_{LLINE}	184			V
High Line Threshold - Low Line Level			V_{LINHYS}	5			V
Supply Voltage (VCC Pin)							
Holding Current Before UVLO (ON)	VCC < UVLO (ON)		I_{VCCST}		150		μA
	VCC < UVLO (ON), VLATCH = 0V		I_{VCCLCH}		300		μA
Operating Current	VFBCOMP = 0V, PFC & Flyback OFF		I_{VCCBST}			1.3	mA
	VFBCOMP = 3V, PFC & Flyback ON		I_{VCC3}			2	mA
UVLO (OFF)	(-20°C ~125°C)		V_{UVOFF}	7.5	8.0	8.5	V
UVLO (ON)	(-20°C ~125°C)		V_{UVON}	17.0	18.0	19.0	V
VCC OVP Level			V_{CCOVP}	30.5	31.5	32.5	V
VCC OVP De-bounce Time*			$T_{DVCCOVP}$		64		μs
Power Down Reset Voltage (PDR)			PDR	6	7	8	V

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
PFC OFF & Open Loop Protection Debounce Timer Setting (CT Pin)							
OLP Debounce Time*	CT=0.047μF, VFBCOMP > VOLP, after start-up		T_{DOLP}		64		ms
	CT=0.047μF, VFBCOMP > VOLP, at start-up		T_{DOLPST}		74		ms
FB Soft Start Time*	CT=0.047μF		T_{FBSS}		10		ms
VCC OSCP Debounce Time	CT=0.047μF, VFBCOMP > VOLP, VCC = UVLO (OFF) + 1V, after start-up		T_{DOSCP}		16		ms
PFC Turn-off Debounce Time	VFBCOMP < VPFC ON/OFF, CT=0.047μF	LD7791/A/C	$T_{DPFCOFF}$		1		s
		LD7791B			8		
External Latch (LATCH Pin)							
LATCH Pin Source Current			I_{LCH}	75	80	85	μA
Turn-On Trip Level			$V_{LATCHON}$	1.30	1.35	1.40	V
Turn-Off Trip Level			$V_{LATCHOFF}$	1.20	1.25	1.30	V
OTP LATCH pin de-bounce time	Disable (High to Low)		$T_{DLATCHOFF}$	400	500	600	μs
On Chip OTP (Internal Thermal Shutdown)							
OTP Level *			$T_{SHUTDOWN}$		140		°C
OTP Hysteresis *			$T_{RESTART}$		40		°C
PFC Output Voltage Sensing (VOSENSE pin)							
Reverence Input Voltage, V_{REF}	(-20°C ~125°C)		V_{FBREF}	2.47	2.50	2.53	V
PFC OVP Trip Level			V_{PFCOVP}	2.59	2.63	2.67	V
	OVP Hysteresis		$V_{PFCOVPHYS}$	0.115	0.130	0.145	V
	Debounce time*		$T_{DPFCOVP}$		50		μs
Source Current of VOSENSE	VHV_{PEAK} = 150V		$I_{FOLBTLV}$		8		μA
	VHV_{PEAK} = 250V		$I_{FOLBTHV}$		0.1		μA
Enable and Disable Threshold Voltage	PFC & Flyback Enable Threshold		V_{PFCEN}	1.0	1.1	1.2	V
	PFC Disable Threshold		V_{PFCENL}	0.8	0.9	1.0	V
	Debounce Time*		T_{DPFCEN}		50		μs
VOSENSE Pull Down Resistance			$R_{VOSENSE}$	5	6	7	MΩ

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX	UNITS
PFC Error Amplifier (PFCCOMP Pin)						
Transconductance		gm	60	80	100	μmho
Output Upper Clamp Voltage	VOSENSE = V_{REF} -0.1V	$V_{PCOMPMAX}$	5.0	5.2	5.4	V
Output Minimum Clamp Voltage		$V_{PCOMPMIN}$	0.85	0.90	0.95	V
PFC Burst Mode	Trip Level for PFCDRIVER Stop*	$V_{PCOMPOFF}$	0.95	1.00	1.05	V
	Trip Level for PFCDRIVER Start*	$V_{PCOMPON}$	Threshold for PFCDRIVER stop + 50mV			V
PFC Maximum On-Time						
PFC Max. On-Time	VHV_{PEAK} = 150V	$T_{ONMAXPLV}$	22	25	28	μs
	VHV_{PEAK} = 250V	$T_{ONMAXPHV}$	7	8	9	μs
PFC Minimum Off-Time						
PFC Minimum Off-Time *		$T_{POFFMIN}$		1		μs
PFC Maximum Frequency						
PFC Maximum Frequency		F_{MAXPFC}	225	250	275	kHz
PFC Current Sensing (PFCSENSE Pin)						
Current Sense Input Threshold Voltage	VHV_{PEAK} = 150V	$V_{PFCCSLV}$	0.47	0.52	0.57	V
	VHV_{PEAK} = 250V	$V_{PFCCSHV}$		0.40		V
Leading Edge Blanking time		T_{LEBPFC}	180	250	320	ns
PFC Zero Current Detector (PFCAUX Pin)						
Upper Clamp Voltage	IPFCAUX = 3mA	$V_{PFCAUXUC}$	3.5	4.0	4.5	V
PFC ZCD Trip Level		$V_{PFCAUXH}$	0.15	0.20	0.25	V
Delay from PFCAUX to Output *		$T_{DPFCZCD}$		200		ns
PFC ZCD Time Out	After PFCDRIVER Turn-off	T_{TOPFC}	40	50	60	μs
PFC ON/OFF Control (PFCONOFF pin)						
Source Current for PFC OFF Threshold Setting		I_{PFCOFF}	24.10	25.00	25.90	μA
Source Current for PFC ON Threshold Setting		I_{PFCON}		25.75		μA

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
Flyback Comp Pin (FBCOMP Pin)							
Short Circuit Current	V_{COMP}=0V		$I_{FBCOMPSC}$	0.100	0.125	0.150	mA
Flyback Burst Mode	Trip Level for FBDRIVER Start	LD7791/A/C	$V_{BSTONQR}$	0.7	0.8	0.9	V
		LD7791B		1.0	1.1	1.2	
	Trip Level for FBDRIVER Stop	LD7791/A/C	$V_{BSTOFFQR}$	0.5	0.6	0.7	V
		LD7791B		0.8	0.9	1.0	
Heavy Load Trigger Level			$V_{IFBCSEN}$	2.8	2.9	3.0	V
Open Loop Voltage	FBCOMP pin open		V_{FBC}	5.2	5.4	5.6	V
Over Load Protection (FBCOMP Pin)							
OLP Trigger Level (VOLP)			V_{OLP}	4.1	4.2	4.3	V
Output Short Circuit Protection							
VCC OSCP Trigger Level *	VFBCOMP > VOLP		V_{CCOSCP}	UVLO (OFF) +2			V
Flyback OVP (FBAUX pin)							
OVP Trigger Current			$I_{FBAUXOVP}$	270	300	330	µA
Upper Clamp Voltage	IFBAUX = 0.3mA		V_{FBAUXH}	1.90	2.00	2.10	V
Debounce Cycle*			$T_{DFBAUXOVP}$		4		FB PWM cycle
FBAUX OVP Detection Blanking Time *	After FBDRIVER Turn-off		$T_{DFBOVPDET}$		3		µs
Zero Current Detection (FBAUX Pin)							
Lower Clamp Voltage	IFBAUX = -1mA		$V_{FBAUXLC}$	-0.3		0	V
Flyback ZCD Trip Level			V_{QRDLQR}		50		mV
Flyback ZCD Delay Time *			T_{DFBZCD}		200		ns
Flyback ZCD Time Out1	After Max. Frequency		T_{O1QR}	4	5	6	µs
Minimum Flyback ZCD Time Out2	After FBDRIVER Turn-off		T_{O2QR}	115	150	185	µs
ZCD Blanking Time	After FBDRIVER Turn-off		$T_{OFFMINQR}$		3		µs

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Flyback Max. Frequency		F_{MAXQR}	78	85	92	kHz
Flyback Max. Frequency Mode Threshold, V_{FBCOMP} *		$V_{FBCFMAX}$		2.2		V
Flyback Green Mode Frequency		$F_{GREENQR}$	27	30	33	kHz
Flyback Green Mode Threshold, V_{FBCOMP} *		$V_{FBCGREEN}$		1.0		V
Flyback Maximum On Time		$T_{ONMAXQR}$	40	45	50	μs
Flyback Current Sensing (FBSENSE Pin)						
Threshold for Cycle by Cycle Current Limit, Vcs(off)	(-20°C ~125°C)	V_{OCQR}	0.62	0.65	0.68	V
Leading Edge Blanking Time		T_{LEBQR}	250	350	450	ns
OCP Compensation Current	VHV_{PEAK} = 250Vdc FBCOMP = 3V	I_{FBCSHV}	180	200	220	μA
Delay to Output*		T_{DCS}		80		ns
PFC and Flyback Gate Drive Output (PFCDRIVER & FBDRIVER Pin)						
Output Low Level	VCC=15V, I_{SINK}=100mA	V_{OUTH1}	0		1.5	V
Output High Level	VCC=15V, I_{SOURCE} =100mA	V_{OUTL}	9.0		VCC	V
Output High Level	VCC=9V, I_{SOURCE} =2mA	V_{OUTH2}	8.5		VCC	V
Output High Clamp Level	VCC=17V	V_{OUTCL}		13		V
Rising Time *	VCC =15V, CL=2700pF	T_{OUTR}		130		ns
Falling Time *	VCC =15V, CL=2700pF	T_{OUTF}		45		ns

Notes:

*Guaranteed by design.

Typical Performance Characteristics

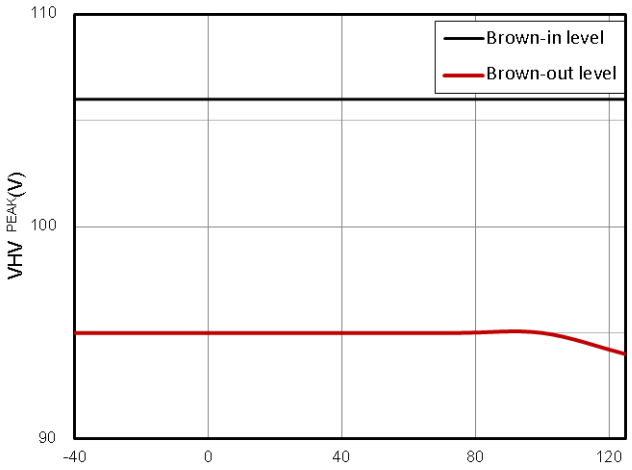


Fig1. BNO level vs.Temperature

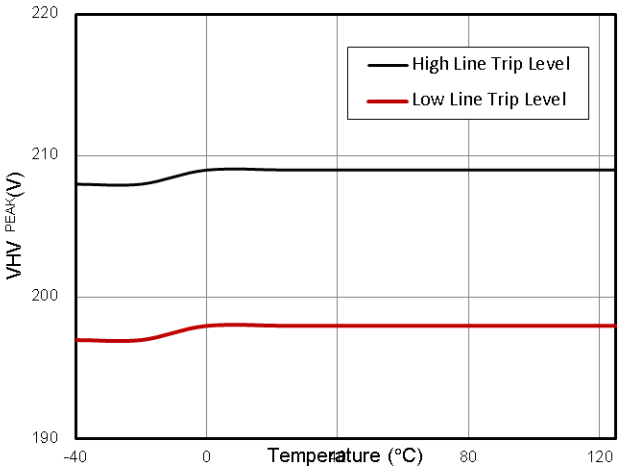


Fig2. High/Low Line Detection Trip Level vs.Temperature

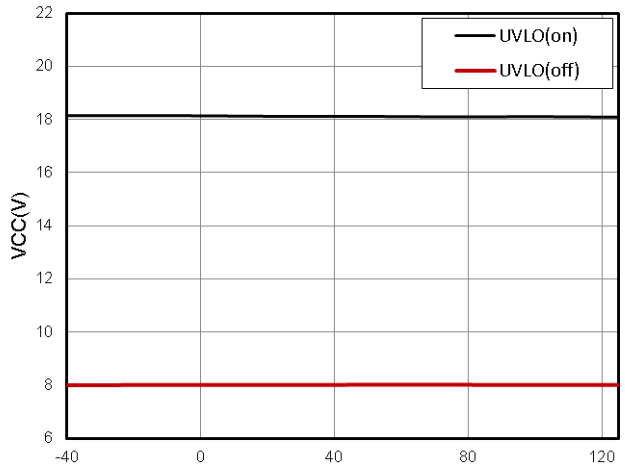


Fig3. UVLO level vs.Temperature

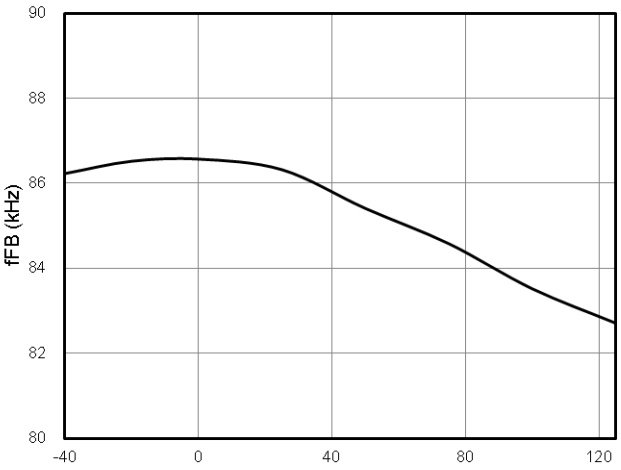


Fig4. QR Flyback Max. Frequency vs.Temperature

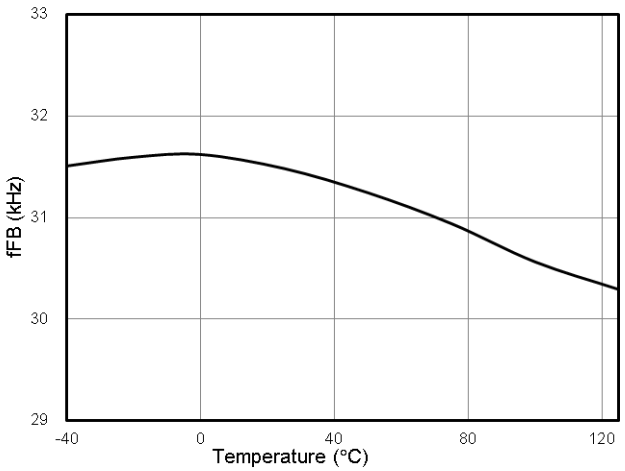


Fig5. QR Flyback Green Mode Frequency vs.Temperature

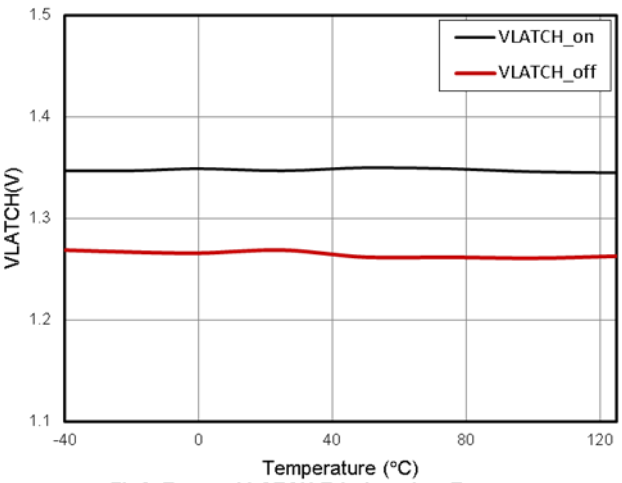


Fig6. External LATCH Trip Level vs.Temperature

Typical Performance Characteristics

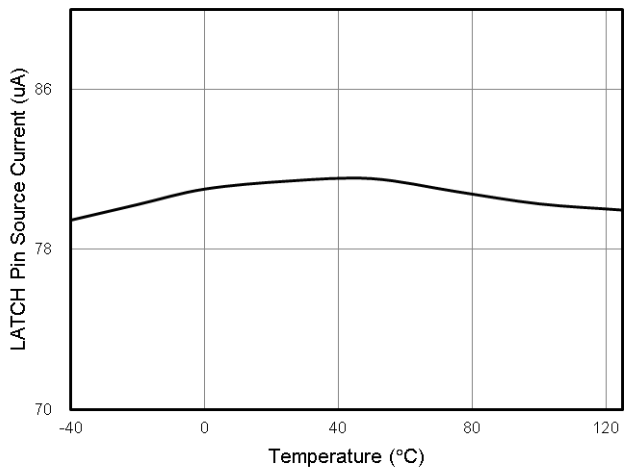


Fig7. LATCH Pin Source Current vs.Temperature

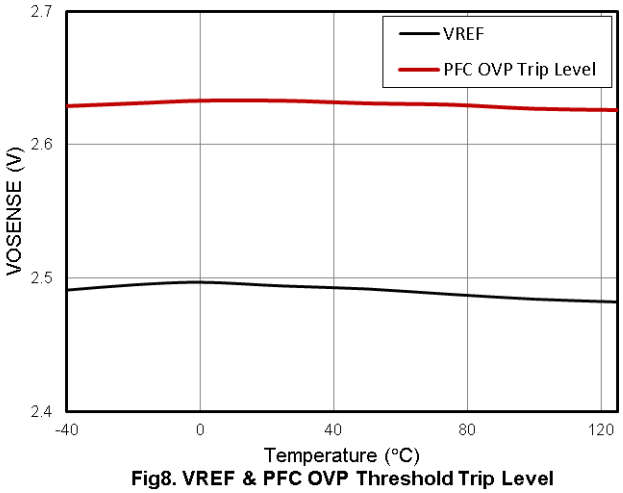


Fig8. VREF & PFC OVP Threshold Trip Level vs.Temperature

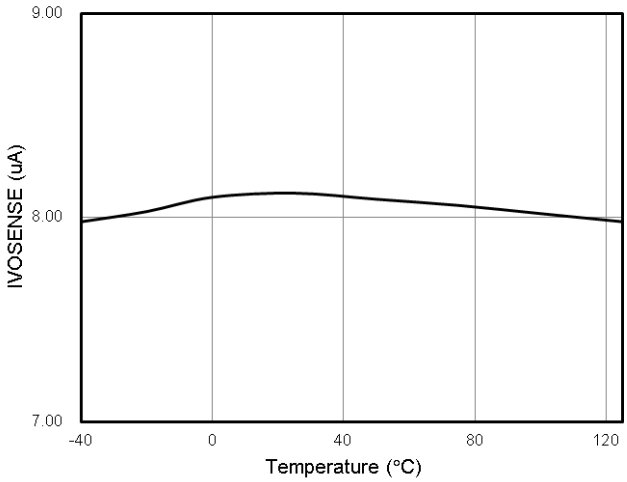


Fig9. Source Current of VOSENSE vs.Temperature

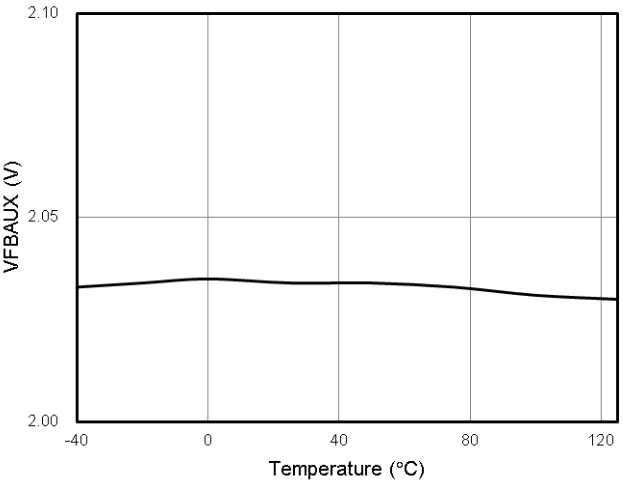


Fig10. FBAUX Upper Clamp Voltage vs.Temperature

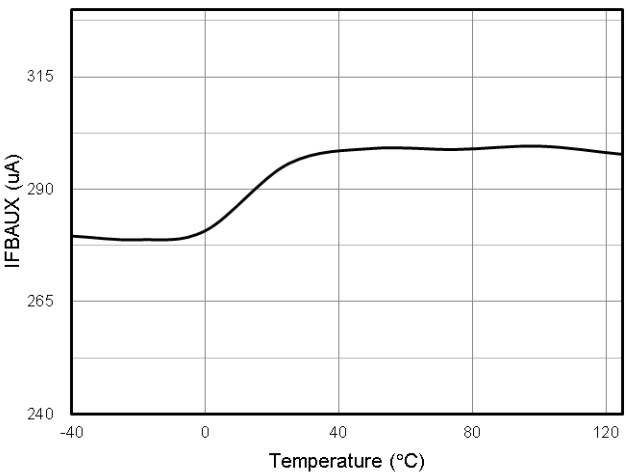


Fig11. FBAUX OVP Trip Current vs.Temperature

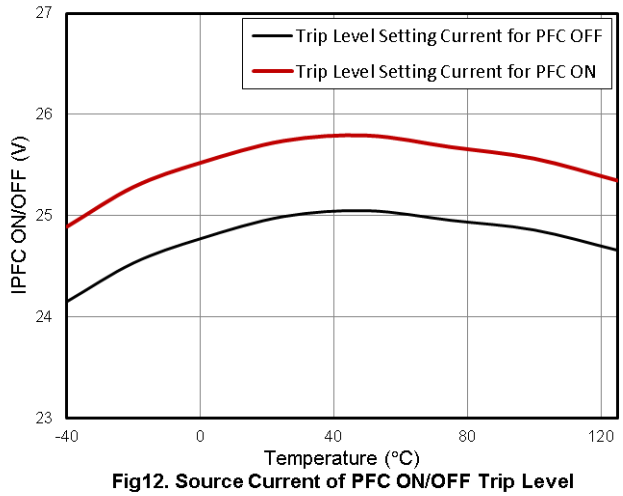


Fig12. Source Current of PFC ON/OFF Trip Level Setting vs.Temperature

Typical Performance Characteristics

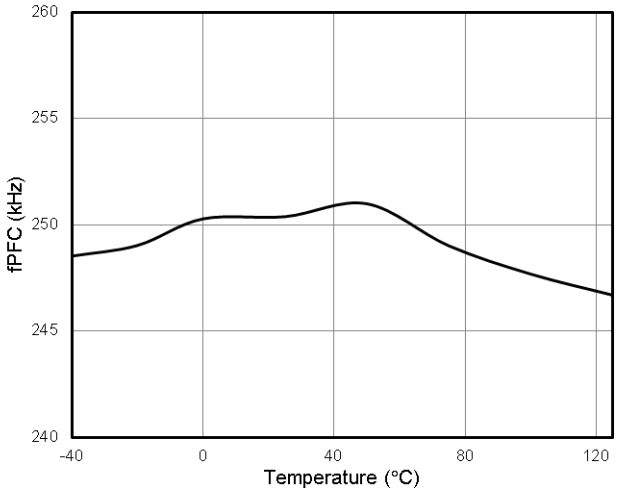


Fig13. PFC Max. Frequency vs.Temperature

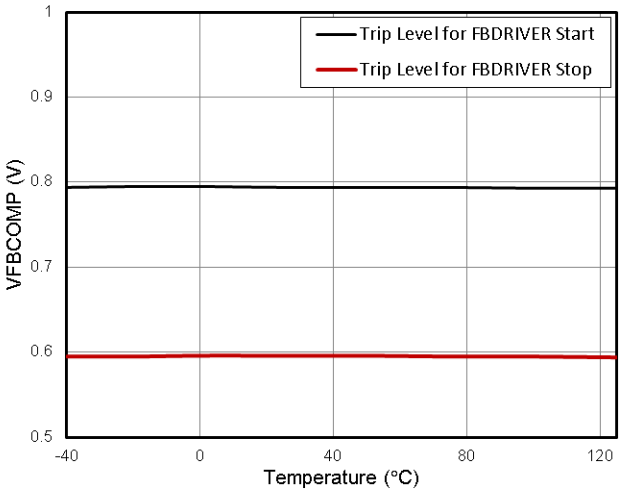


Fig14. Threshold for FB Burst Mode vs.Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers to integrate more functions and reduce the external part counts. The LD7791/A/B/C is ideal for these applications to provide an easy and cost effective solution. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes too much power to meet the power saving requirement. In most cases, startup resistors carry larger resistance and take much time to start up.

As shown in Fig 15, the LD7791/A/B/C is implemented with a high-voltage startup circuit to minimize power loss. During the startup phase, the high-voltage current source sinks current from AC Line or Neutral to provide the startup current and charge the VCC capacitor C1 at the same time.

Please refer to Fig 16. If VCC is below PDR, the charge current is only 1.5mA and the lower charge current can protect IC if the VCC Pin is short to the GND. Once VCC voltage rises up to the UVLO(ON) threshold, HV pin will no longer charge the capacitor. On the contrary, it sends a gate-drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across VCC pin and ensure the supply voltage is high enough to power on the LD7791/A/B/C in addition to driving the power MOSFET. As shown in Fig 16, the hysteresis is provided to prevent the LD7791/A/B/C from shutdown by the voltage dip during startup. The turn-on and turn-off threshold level are set at 18V and 8V respectively.

For better EMI performance, it's recommended to connect HV pin to the input terminals of bridge diode, as Fig 15.

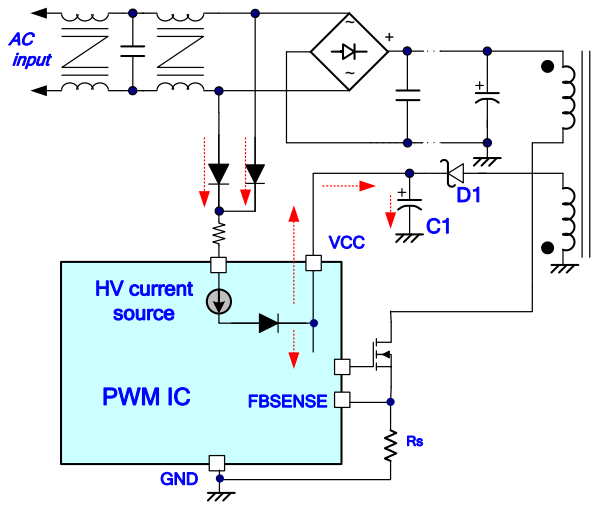


Fig 15.

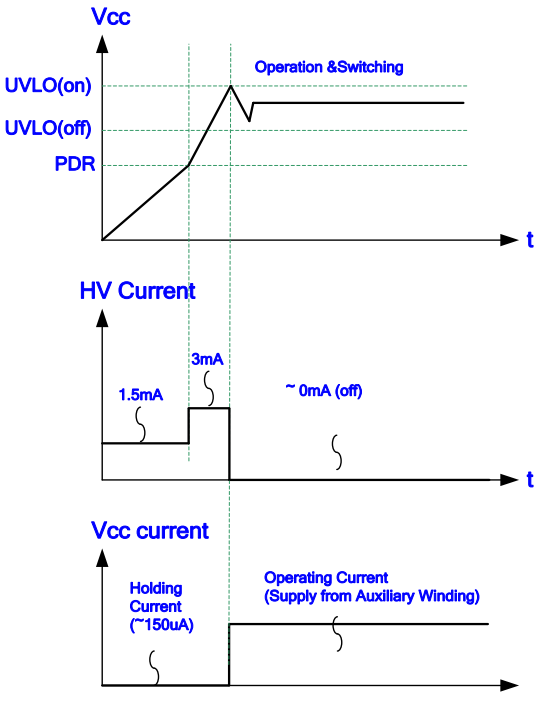


Fig 16.

Output Driver Stage

The device builds a CMOS buffer respectively in the stages of PFC and Flyback, with typical 500mA/-1200mA driving capability, to drive the power MOSFET directly. The output voltage is fixed at 13V to protect the MOSFET gate even when the VCC voltage is over 13V.

Brown In/ Out Protection

The LD7791/A/B/C features brown-in / brown-out protection on HV pin. As the built-in comparator detects line voltage, it will turn off the controller to prevent any damages. In case of VHV < Brown-out Level, the output driver will be disabled even when VCC already reaches UVLO (ON). It therefore forces VCC hiccup between ULVO (on) and UVLO (OFF). Unless the line voltage is large enough and over Brown-in Level, the output driver will not start switching even if the next ULVO (on) is tripped. A hysteresis is designed to prevent false-triggering and damage to the external components during turn-on and turn-off phase. See Fig 17 for the operation.

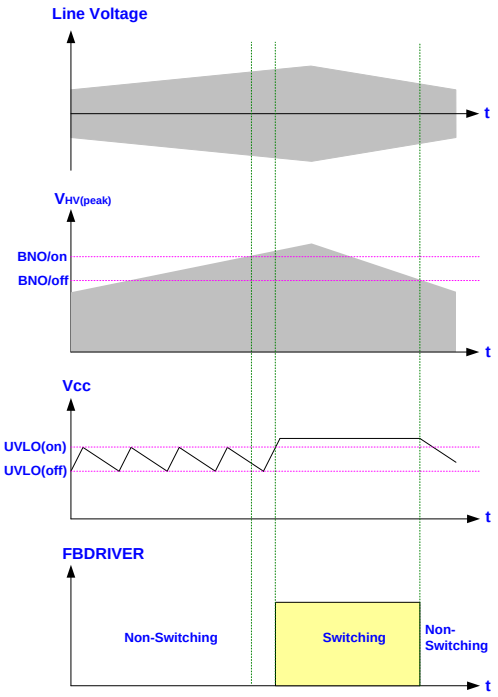


Fig 17.

High Line and Low Line Detection

The HV pin can detect AC input level to control source current of VOSENSE Pin and OCP compensation logic. During AC input variations, the source current of VOSENSE and OCP compensation logic is as follows:

VHV_{PEAK}	Source Current of VOSENSE	OCP Comp. Logic
> 220V	0A	Enable
< 184V	8μA	Disable

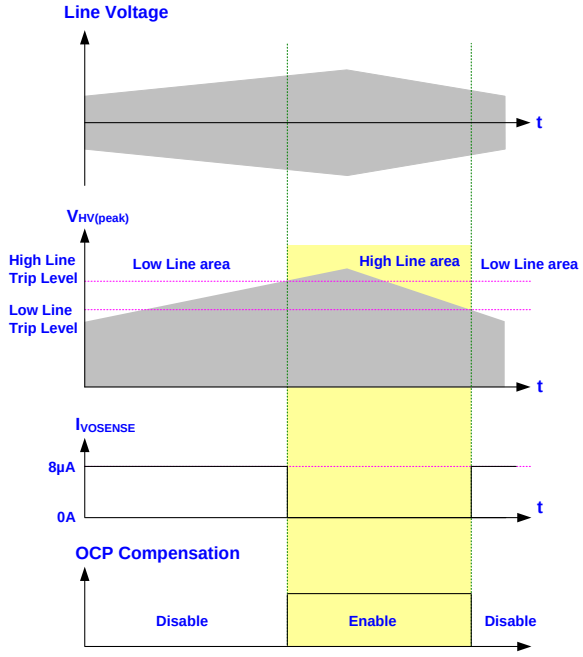


Fig 18.

X-CAP Discharge Function

In general, a discharging resistor is placed across X-capacitor. To meet safety requirement, this component requires to be discharged in less than 1sec, that is,

$$\tau_{Discharge} = C_{X-Cap} \times R_{Discharge} \leq 1sec$$

The power loss of this resistor is in direct proportion to the square of input voltage. For example, if the input voltage is 264Vac and the discharging resistance is around 2MΩ,

35mW, we can predict the power loss by the following equation.

$$P_{Loss} = \frac{V_{AC(RMS)}^{2}}{R_{Discharge}}$$

To eliminate the significant power loss from this discharging resistor, the LD7791/A/B/C applies the innovative patent technology to discharge X-CAP's energy through HV current source when AC line is disconnected. Fig 19 shows the operation.

By applying this technology, the system can easily pass the safety test without discharging resistor. It reduces power loss as well.

If it's unplugged, the AC voltage across X-CAP will still remain the same. The LD7791/A/B/C detects HV pin to monitor the AC voltage across X-CAP. If AC voltage across X-CAP rises or falls beyond the limit of the threshold, under any load conditions, the HV scheme will sink constant current to the GND to discharge it in around 75ms of debounce time.

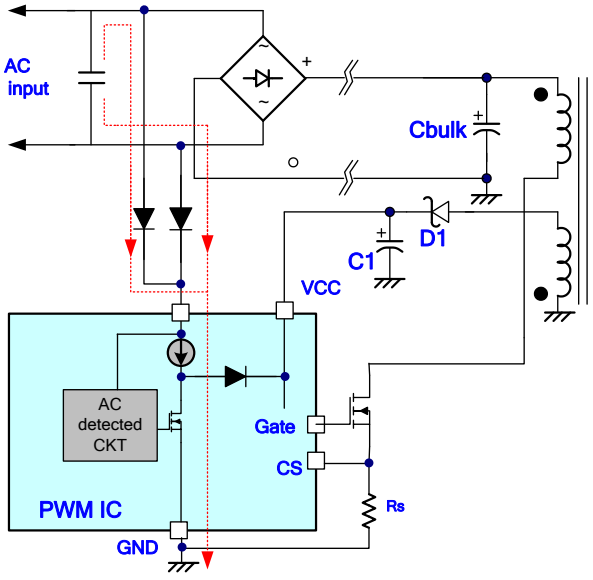


Fig 19.

Flyback Green Mode and PFC Turn-off Control

The LD7791/A/B/C uses maximum frequency limit scheme to control flyback switching frequency, and it depends on the level of FBCOMP voltage. When output loading is decreased, FBCOMP voltage becomes lower and the switch frequency can be reduced under the light load condition. This feature helps to enhance the efficiency in light load condition. The curve is shown as Fig 20.

To meet the requirement of European 'EMC-directive', it's necessary to adopt a solution with PFC control. In order to enhance efficiency under light load, the LD7791/A/B/C features PFC control and is able to shut down switching to reduce power consumption. As FBCOPM voltage falls below PFC ON/OFF voltage threshold, the PFC controller will stop PFCDRIVER switching until FBCOMP voltage resume its level. See Fig 21 for the block.

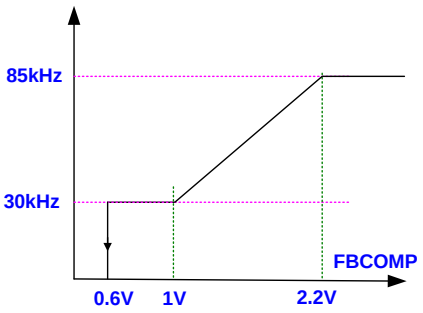


Fig 20. Max. Frequency Limit of Flyback

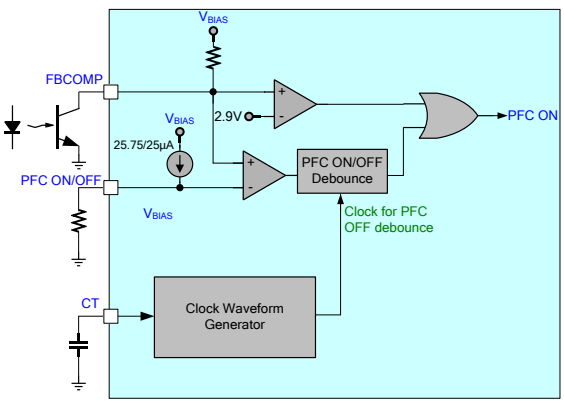


Fig 21.

PFC Output Voltage Setting

The LD7791/A/B/C monitors the output voltage signal from the VOSENSE pin through a resistor divider pair of RA and RB. A transconductance amplifier is used to replace the conventional voltage amplifier. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal. The current is flowed out of the VOSENSE Pin (8μA) during low line condition. The PFC output voltage is determined by the following relationship.

High Line:

$$\text{PFC } V_O = 2.5V \times (1 + \frac{RA}{RB // R_{VOSENSE}}) \quad \cdots\cdots\cdots\cdots\cdots (1)$$

Low Line:

$$\text{PFC } V_O = (2.5V - 8\mu A \times RB // R_{VOSENSE}) \times (\frac{RA}{RB // R_{VOSENSE}}) + 2.5V \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Please refer to the equation where RA and RB are values for top and bottom feedback resistor (as shown in the Fig 22).

Once the value of PFC V_O is determined, then substitutes the value of RA/RB obtaining from the formula (1) to (2) to get the RB value.

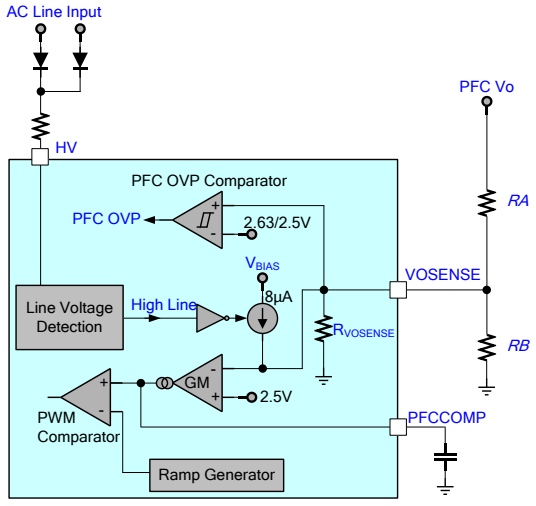


Fig 22.

PFC Over Voltage Protection

In order to prevent the bulk cap from being harmed due to overvoltage phenomenon during start-up, transient or fault conditions. The OVP is implemented on the VOSENSE pin. If the VOSENSE voltage rises over the OVP threshold of 2.63V, the output driver circuit will be shut down simultaneously to stop the switching of the power MOSFET until the VOSENSE voltage drops to 2.5V. Fig 15 shows its operation.

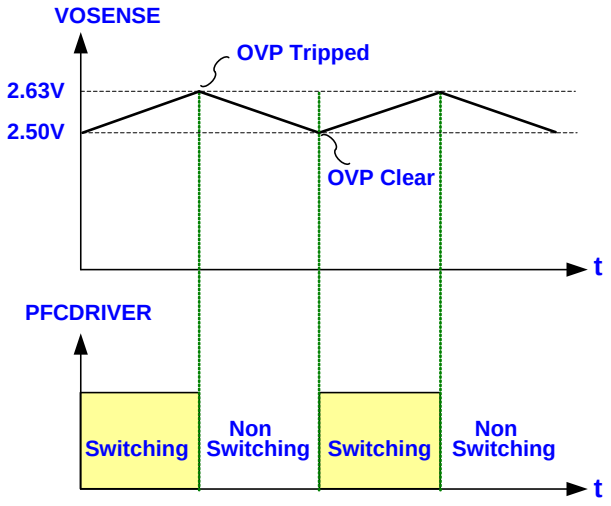


Fig 23.

PFC Zero Current Detection

Fig 24 shows PFC Zero Current Detection (ZCD) block. As the auxiliary winding coupling with the inductor detects that the current over the boost inductor drops to zero, the ZCD block will switch on the external MOSFET. This feature allows transition-mode to be operated. If the voltage of the PFCAUX pin rises above 0.2V, the ZCD comparator will turn on the MOSFET. The PFCAUX pin is protected internally by 4V-high clamp and 0V-low clamp. The 50μs timer will generate a MOSFET turn-on signal if the output driver has being at low level over 50μs.

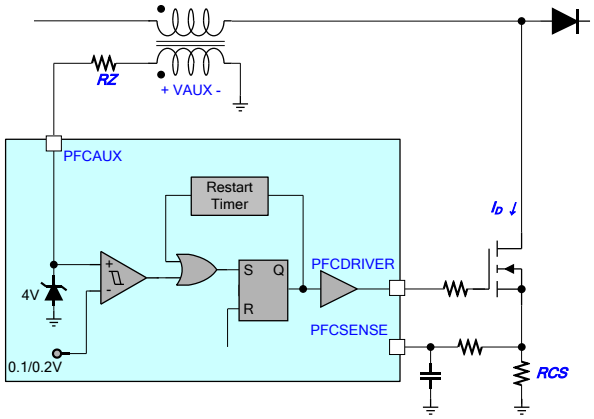


Fig 24.

Fig 25 shows typical ZCD-related waveforms. Rz will produce some delay because of the parasitic capacitance on the PFCAUX pin. Before the switch turns on with delay, the stored charge of the C_{OSS} (MOSFET output capacitor) will be discharged to a small filter capacitor C_{IN1} with a bridge diode through the path indicated in Fig 26. So the input current I_{IN1} drains to zero at the time. Here, it's recommended to set source current of the PFCAUX pin around 1mA. Rz can be obtained from the below formula and it is also adjustable to control the turn-on timing of the switch.

$$R_Z = PFC\ Vo^{MAX} \times \frac{N_{AUX,PFC}}{N_{P,PFC}} \div 1mA$$

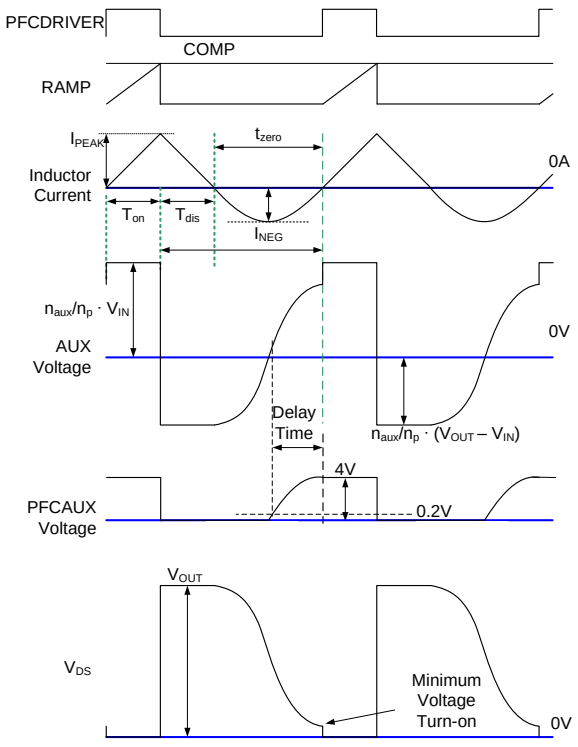


Fig 25.

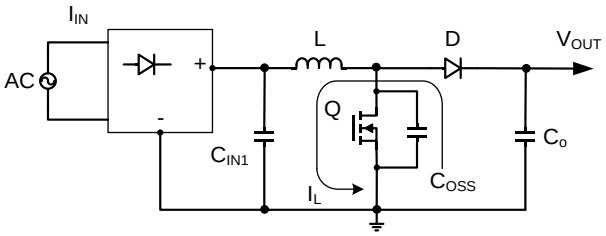


Fig 26.

PFC Current Sensing

The LD7791/A/B/C detects the PFC MOSFET current across the PFCSENSE pin to protect the MOSFET, by performing the cycle-by-cycle current limit. The maximum voltage threshold of the PFCSENSE pin is set at 0.52V. The MOSFET peak current can be obtained as below.

$$I_{PEAK(MAX)} = \frac{0.52V}{R_{PFCS}}$$

A 250ns leading-edge blanking (LEB) timer is built in the PFCSENSE pin to prevent the false-triggering caused by current spike.

However, the pulse width of the turn-on spike is determined according to the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for high power application to avoid the PFCSENSE pin being damaged by the negative turn-on spike.

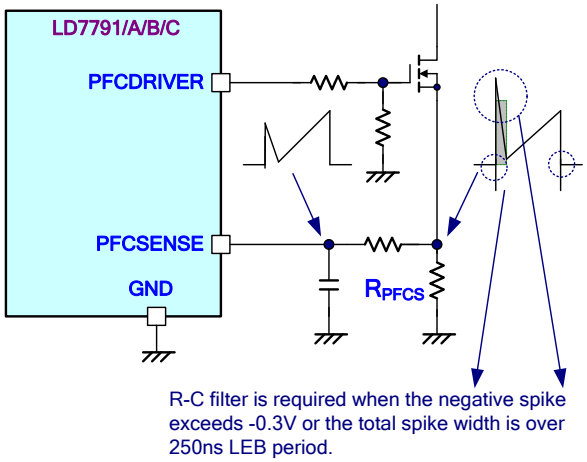


Fig 27.

Flyback Voltage Feedback Loop

The voltage feedback signal is provided by the TL431 at the secondary side through the photo-coupler to the FBCOMP pin of the LD7791/A/B/C and fed to the voltage divider with 1/5.5 ratio. That is,

$$V_{FBSENSE(PWM_{COMPARATOR})} = \frac{V_{FBCOMP}}{5.5}$$

A pull-high resistor is embedded internally to optimize the external circuit.

Flyback Burst Mode Control

The output driver of the LD7791/A/B/C can be disabled immediately by pulling FBCOMP pin voltage level below FBDRIVER Stop Trip Level. The disable-mode can be released when FBCOMP pin voltage level is pulled higher than FBDRIVER start trip level.

Flyback Current Sensing & OCP Compensation Design Tip

The LD7791/A/B/C features current mode of flyback control. It receives both current and voltage signal to form the control loop and achieve regulation. LD7791/A/B/C detects the primary MOSFET current across FBSENSE pin for peak current mode and also limits the current cycle-by-cycle. The maximum voltage threshold of FBSENSE pin is set at 0.65V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.65V}{R_{FBS}}$$

In general, the power converter provides various current signals to reflect the input voltage with propagation delay time. To compensate it, an offset voltage is added to the FBSENSE signal by an internal current source (200μA) and an external resistor (R_{OCP}) between the sense resistor (R_{FBS}) and FBSENSE pin, as shown in Fig 28. The compensation current is only enabled when FBCOMP voltage is above 2.9V at high line condition. ROCP: 220Ω~1kΩ; COPC: 47pF~470pF.

As PFC behaves in current sensing, a 350ns leading-edge blanking (LEB) timer is incorporated in the input of FBSENSE pin to prevent false-triggering caused by current spike.

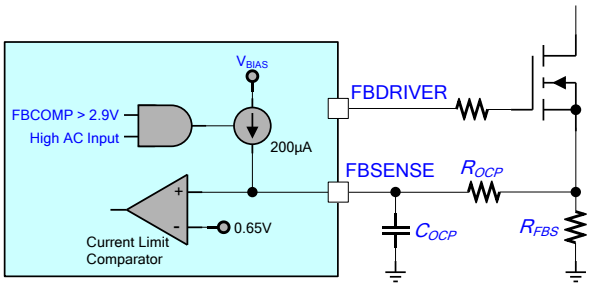


Fig 28.

Protection Mode

There are two kinds of protection modes in the LD7791/A/B/C.

Auto-Recovery Protection Mode

As Auto-Recovery protection circuit latches the operation, the gate output will switch for a short term as every time VCC rises back to UVLO(ON). It therefore forces the VCC hiccup between UVLO(ON) and UVLO(OFF). As soon

as the fault condition is removed, the system will resume it operation right away. Fig 29 shows the operation.

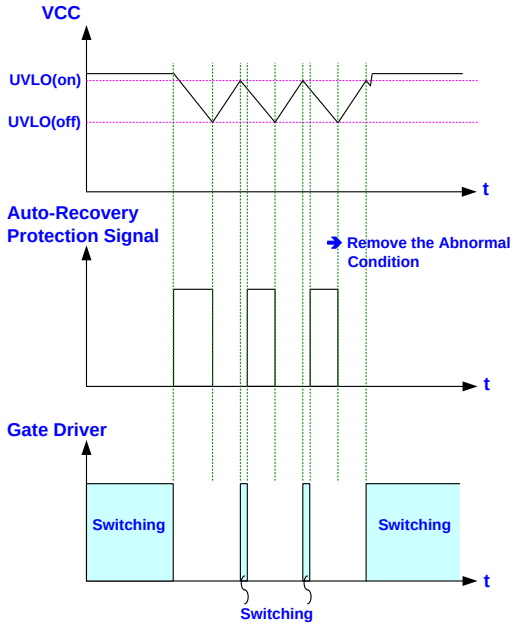


Fig 29.

Latch Protection Mode

As Latch type protection circuit latches the operation, the gate output will remain in off-state even when the VCC reaches UVLO(ON). The system is unable to recover unless it is repowered to let VCC drop below Power Down Reset (PDR) and then ramps over UVLO(ON). Fig 30 shows the operation.

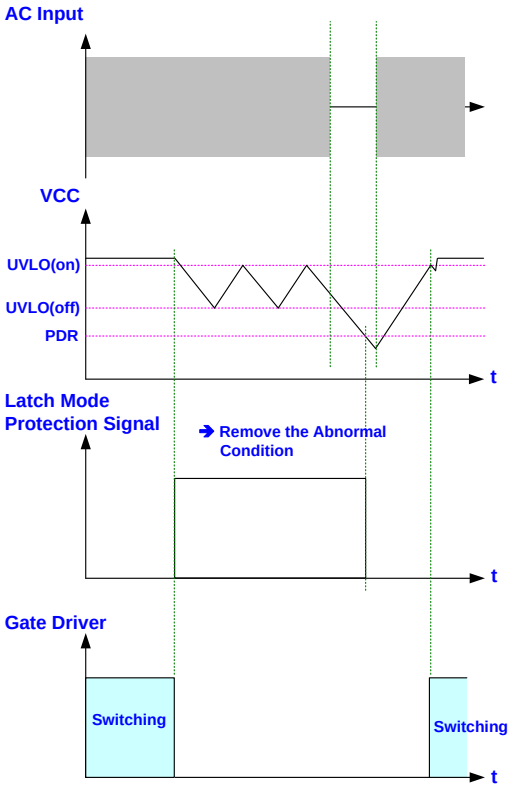


Fig 30.

Over Load Protection (OLP)– Auto Recovery or Latch

To protect the circuit from being damaged at over-load condition, short or open loop condition, the LD7791/A/B/C is implemented with smart OLP function. The LD7791/A/B/C features auto recovery function for LD7791/A/C, while LD7791B features latch function. See Fig 31 for the auto-recovery waveform. In such fault condition, the feedback system will force the voltage loop to enter saturation and then pull high the voltage over FBCOMP pin (VFBCOMP). When VFBCOMP ramps up to the OLP tripped level (4.2V) for longer than the OLP delay time, the protection will be activated to turn off the output driver and stop the switching of power circuit. The OLP delay time is set by CT pin. It is to prevent the false triggering during the transient condition of power-on and turn-off.

A divide-4 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-4 counter starts to count the number of UVLO(OFF). The protection mode will not be released and the output will not be resumed until the 4th UVLO(off) level is tripped. With the protection mechanism, the average input power will be reduced, so that the component temperature and stress can be controlled in the safe operating area.

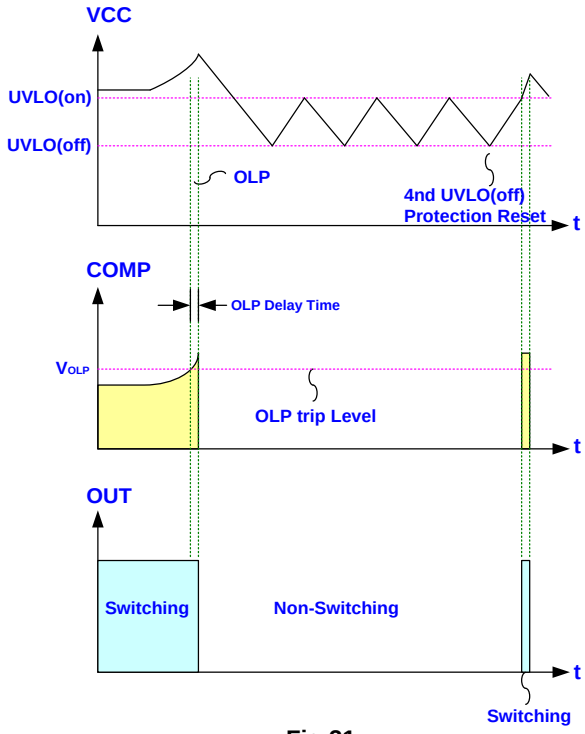


Fig 31.

Output Short Circuit Protection (OSCP)

If the output of the system is short-circuited, Vo and VCC will drop immediately. Due to the operating of the voltage loop, FBCOMP voltage will be pulled high at the same time. If the situation continues to pull FBCOMP high over 4.2V for over 16ms and VCC drops below 10V, it will activate OSCP protection against damage and turn off the gate driver.

OVP on VCC – Auto Recovery or Latch

The maximum VCC rating of the LD7791/A/B/C is about 32.5V. To protect the LD7791/A/B/C in over-voltage condition, it is implemented with OVP function on VCC. Once VCC voltage rises over the OVP threshold, it will turn off the output driver right away and be disable the power MOSFET until the UVLO(ON) is tripped.

The LD7791/A/B/C offers both auto-recovery mode protection (LD7791/C) and latch mode protection(LD7791B/C) for the users to choose. Fig 32 shows auto-recovery mode operation.

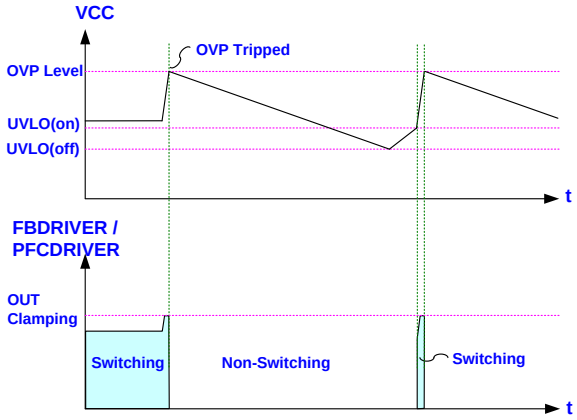


Fig 32.

Flyback Zero Current Detection

Fig 33 shows Flyback Zero Current Detection (ZCD) block. As PFC behaves in ZCD, as soon as the auxiliary winding coupled with the inductor detects that the current over the flyback transformer drops to zero, the ZCD block will switch on the external MOSFET. This feature enables Quasi-Resonant operation. The FBAUX uses falling edge to trigger ZCD to turn on FBDRIVER and the trigger level is 0.05V as shown in Fig 34. FBAUX pin is built-in with 2V-high and 0V-low clamp.

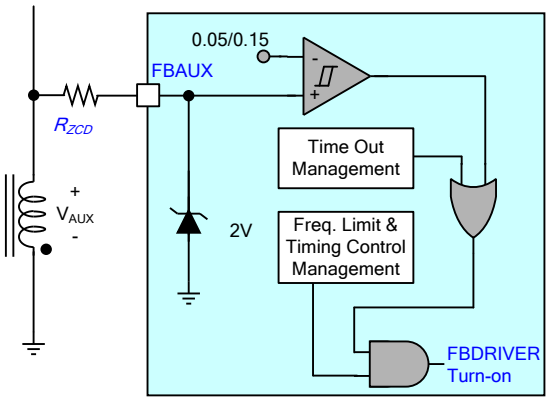


Fig 33.

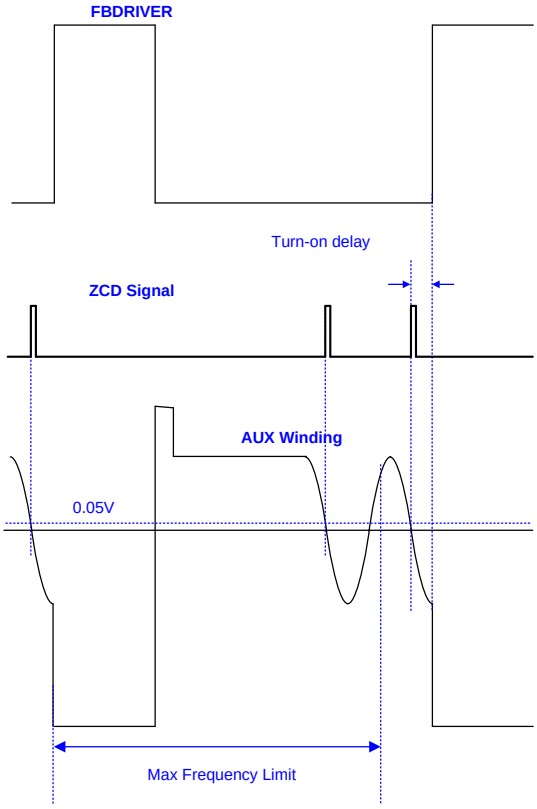


Fig 34.

OVP on FBAUX – Auto Recovery or Latch

FBAUX also provides over voltage protection (OVP). An output overvoltage protection is implemented in the LD7791/A/B/C, as shown in Fig 35 and Fig 36. It senses the auxiliary winding voltage by the resistor, R_{ZCD}. The auxiliary winding voltage is reflected on the secondary winding and therefore the flat voltage on FBAUX pin is in proportion to the output voltage. The flat voltage can be transformed into a current signal. The sinking current of FBAUX is,

$$I_{FBAUX} = [(V_O + V_D) \times \frac{N_{AUX}}{N_S} - 2V] / R_{ZCD}$$

The LD7791/A/B/C samples the signal after FBDRIVER turns off with 3μs delay to perform output over voltage protection. This 3μs delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampled current level is compared with internal threshold current 300μA. If the sampled current exceeds the OVP trip level, an internal counter will start to count the subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If 4 flyback PWM cycles of the subsequent OVP events are detected, the OVP circuit will switch the power MOSFET off.

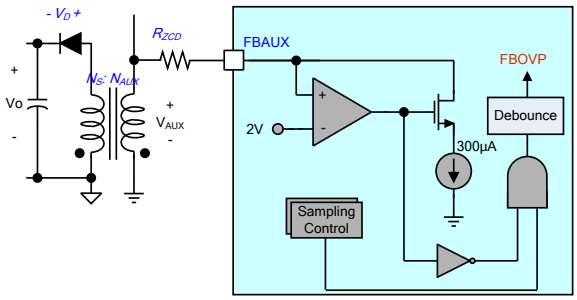


Fig 35.

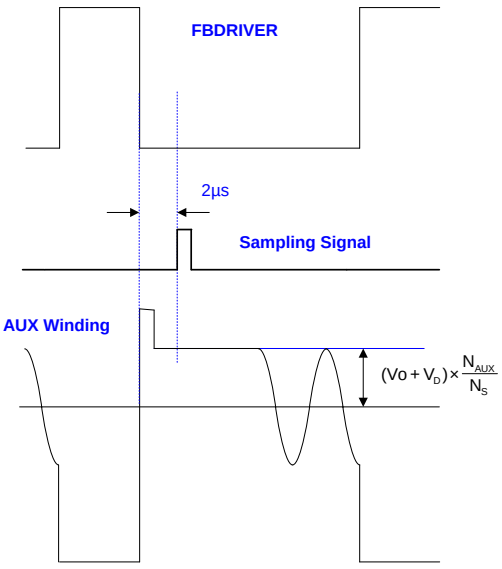


Fig 36.

On-Chip OTP – Auto Recovery

An internal OTP circuit is embedded in the LD7791/A/B/C to provide the worst-case protection. When the chip temperature rises over the trip OTP level, the output driver will be disabled until the chip is cooled down below the hysteresis temperature.

External Latch –Latch

The External Latch function is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Once an over-temperature condition is detected, the OTP will be activated to shut down the LD7791/A/B/C.

Typically, the NTC is recommended to connect to LATCH pin. The NTC resistance will decrease as the device or surroundings stays in high temperature. The relationship is shown as below.

$$V_{LATCH} = 80\mu A \times R_{NTC}$$

When the formula, V_{LATCH} < Turn-off Trip (typ. 1.25V), is established, it will trigger the protection to shut down the output driver and latch off the power supply. The LD7791/A/B/C will remain latched unless the VCC drops below PDR (power down reset) and rise over UVLO(ON). It requires two conditions to restart the LD7791/A/B/C successfully. Cool down the circuit so that the NTC resistance will increase and raise V_{LATCH} above 1.35V, then to plug in AC power again. The detailed operation is shown in Fig 37.

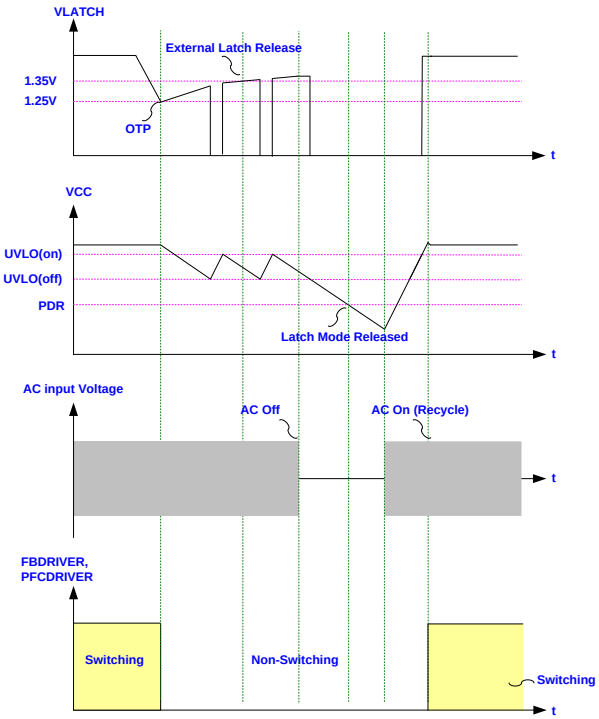


Fig 37.

Adjustable Timer on CT Pin

Connect CT pin with an external capacitance to generate clock for timer. The OLP debounce, PFC Turn-off debounce and flyback Soft-start period are set according to the below table.

C_{CT}	FB Soft-start period	OLP Debounce Time	PFC Turn-off Debounce	
22nF	4.6ms	30ms	LD7791, LD7791A LD7791C	0.47s
			LD7791B	3.76s
47nF	10.0ms	64ms	LD7791, LD7791A LD7791C	1.00s
			LD7791B	8.00s
68nF	14.0ms	93ms	LD7791, LD7791A LD7791C	1.45s
			LD7791B	11.6s
100nF	21.2ms	136ms	LD7791, LD7791A LD7791C	2.13s
			LD7791B	17.0s

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7791/A/B/C consists of an anti-floating resistor at PFCDRIVER and FBDRIVER pin to prevent the output driver in any abnormal condition which may false triggering MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig 38, the resistor R8 can provide a discharge path to prevent the MOSFET from being false-triggering by the current through the gate-to-drain capacitor C_{GD}. Therefore, the gate of MOSFET should be always pulled low and kept in the off-state as the gate resistor is disconnected or opened in any case.

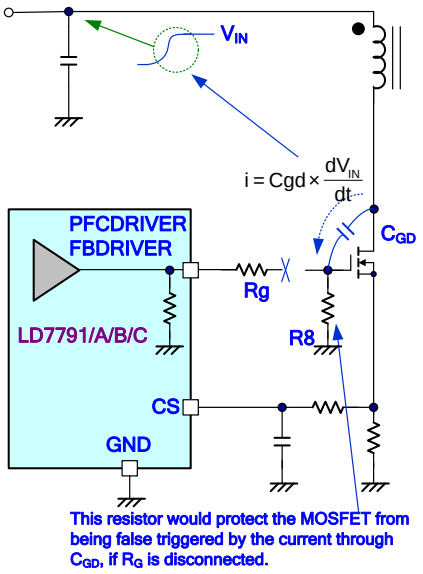


Fig 38.

Protection Resistor on the HV Path

In some other Hi-V process and design, there may be a parasitic SCR to be formed between HV pins, VCC and GND. As shown in Fig 39, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in the LD7791/A/B/C. Fig 40 shows the equivalent Hi-V structure circuit of the LD7791/A/B/C. The LD7791/A/B/C is more capable to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to be added in the Hi-V path to regard as a current limit resistor whenever a negative voltage is applied.

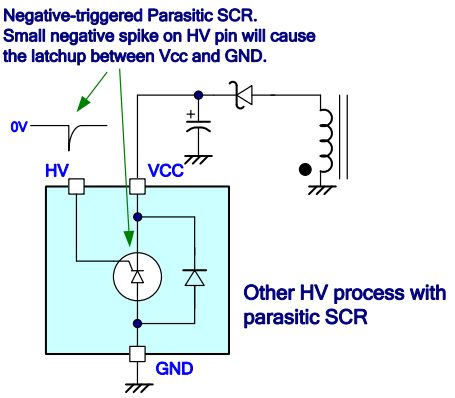


Fig 39.

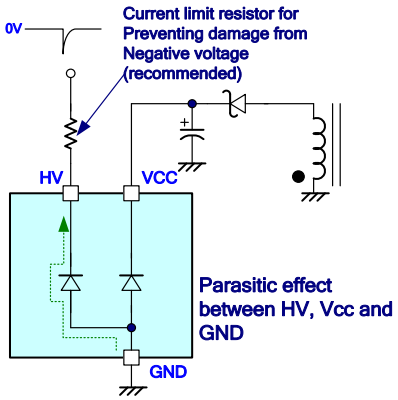


Fig 40.

PCB Layout Guideline

The LD7791/A/B/C consists of a pair of gate drivers. Here are some guide lines to layout the PCB for suppressing the noises caused from the effects between PFC and flyback. The PCB layout diagram is shown as Fig 41.

1. Separate small signal current loop from gate driver or VCC current loop.
2. Separate VCC current loop from PFC gate driver to minimize the effect from flyback ZCD.
3. Minimize the trace length between the GND pin and the current sense resistor.
4. Be aware of routing the HV pin AWAY from the other traces so that it possesses high voltage.

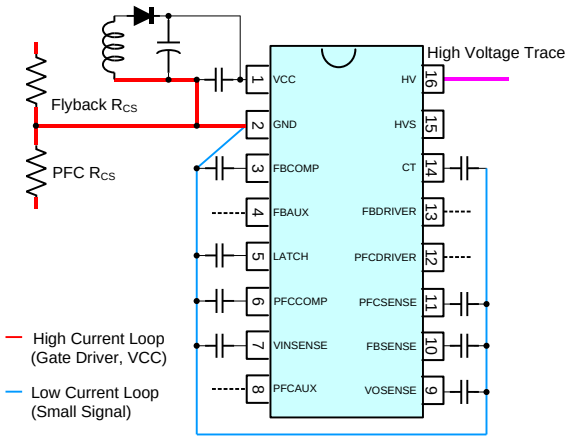


Fig 41.

Inrush Current of PFC

During the period that AC power goes on/off fast, inrush current will flow through PFC choke if bulk capacitor voltage is lower than AC line voltage. Once PFC controller remains operation in such condition, large current will flow in PFC MOSFET during gate turn-on phase, shown as Fig 42. So, it's necessary to select a MOSFET of proper current stress to avoid damage.

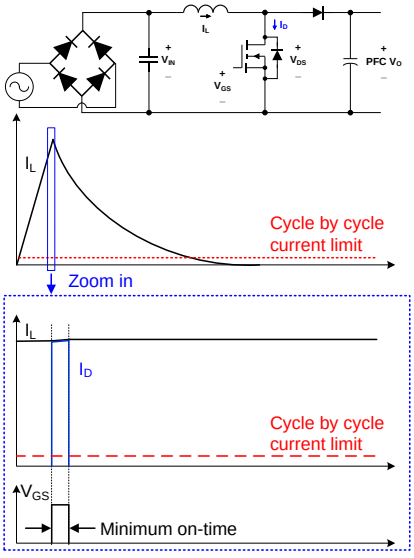


Fig 42.

Under this condition, during MOSFET gate turn-on and turn-off period, some MOSFET will couple with the high frequency energy, generated from parasitic element as inrush current resonates into the controller. See Fig 43 for it. The gate driver of controller can be damaged by the

external energy. A bead core is added in the gate driver current loop to filter the high frequency voltage from damage, shown as Fig 44. Placing an extra by-pass diode here to limit inrush current of PFC choke helps to minimize the risk, shown as Fig 45.

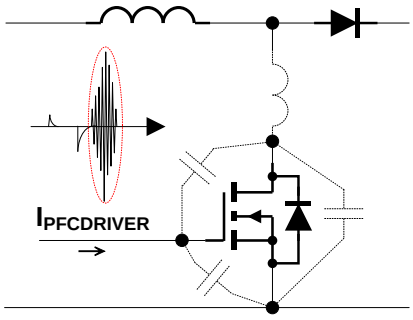


Fig 43.

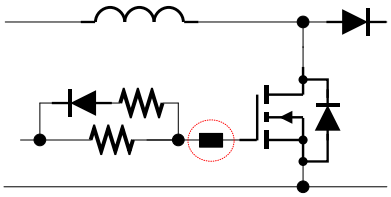


Fig 44.

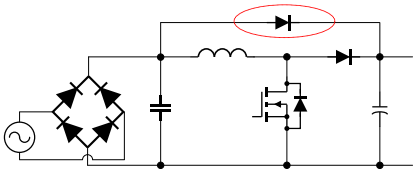
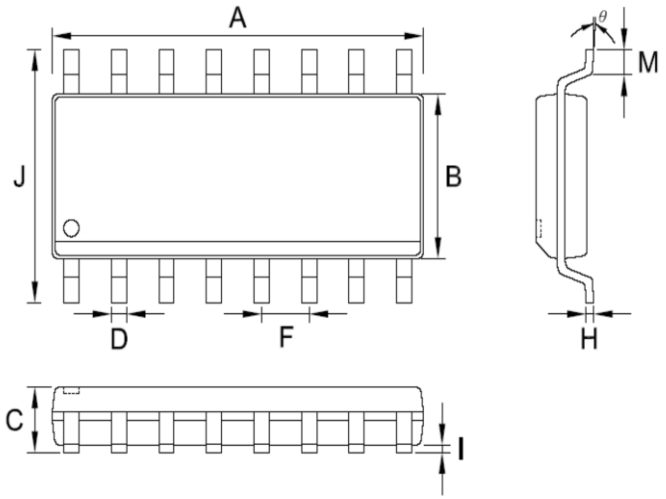


Fig 45.

Package Information

SOP-16



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	9.800	10.010	0.386	0.394
B	3.800	4.000	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.510	0.013	0.020
F	1.27 TYP.		0.05 TYP.	
H	0.178	0.254	0.007	0.010
I	0.100	0.254	0.004	0.010
J	5.790	6.200	0.228	0.244
M	0.380	1.270	0.015	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Date	Change Notice
00	09/03/2014	Original Specification.
01	03/03/2015	Add LD7791B information.
02	04/24/2015	Spec θ_{JC} is added. Spec items are changed: 1. The max power dissipation and junction temperature are changed. 2. The typical value of t_{FBSS} is changed. 3. The C_{CT} Pin timer table is modified.
03	05/26/2016	The block diagram is corrected.
04	06/14/2019	Add LD7791C information.

Important Notice

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