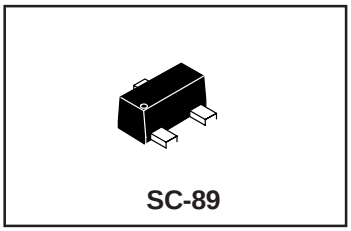
Bias Resistor Transistors

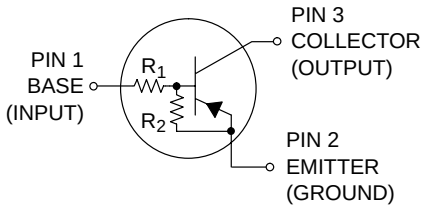
LDTA114EET1G Series

PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network



This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC-89 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- We declare that the material of product compliance with RoHS requirements.



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Total Device Dissipation, FR−4 Board (Note 1) @ T_A = 25°C Derate above 25°C	P_D	200 1.6	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR−4 Board (Note 2) @ T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 × 1.0 Inch Pad.

LDTA114EET1G Series

ORDERING INFORMATION AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping†
LDTA114EET1G	6A	10	10	SC−89	3000 Tape & Reel
LDTA124EET1G	6B	22	22	SC−89	3000 Tape & Reel
LDTA144EET1G	6C	47	47	SC−89	3000 Tape & Reel
LDTA114YET1G	6D	10	47	SC−89	3000 Tape & Reel
LDTA114TET1G	6E	10	∞	SC−89	3000 Tape & Reel
LDTA143TET1G	6F	4.7	∞	SC−89	3000 Tape & Reel
LDTA123EET1G	6H	2.2	2.2	SC−89	3000 Tape & Reel
LDTA143EET1G	43	4.7	4.7	SC−89	3000 Tape & Reel
LDTA143ZET1G	6K	4.7	47	SC−89	3000 Tape & Reel
LDTA124XET1G	6L	22	47	SC−89	3000 Tape & Reel
LDTA123JET1G	6M	2.2	47	SC−89	3000 Tape & Reel
LDTA115EET1G	6N	100	100	SC−89	3000 Tape & Reel
LDTA144WET1G	6P	47	22	SC−89	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	LDTA114EET1G	I_{EBO}	−	−	0.5	mAdc
	LDTA124EET1G		−	−	0.2	
	LDTA144EET1G		−	−	0.1	
	LDTA114YET1G		−	−	0.2	
	LDTA114TET1G		−	−	0.9	
	LDTA143TET1G		−	−	1.9	
	LDTA123EET1G		−	−	2.3	
	LDTA143EET1G		−	−	1.5	
	LDTA143ZET1G		−	−	0.18	
	LDTA124XET1G		−	−	0.13	
	LDTA123JET1G		−	−	0.2	
	LDTA115EET1G		−	−	0.05	
	LDTA144WET1G		−	−	0.13	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

LDTA114EET1G Series

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)						
DC Current Gain	LDTA114EET1G	h_{FE}	35	60	–	–
(V_{CE} = 10 V, I_C = 5.0 mA)	LDTA124EET1G		60	100	–	
	LDTA144EET1G		80	140	–	
	LDTA114YET1G		80	140	–	
	LDTA114TET1G		160	250	–	
	LDTA143TET1G		160	250	–	
	LDTA123EET1G		8.0	15	–	
	LDTA143EET1G		15	27	–	
	LDTA143ZET1G		80	140	–	
	LDTA124XET1G		80	130	–	
	LDTA123JET1G		80	140	–	
	LDTA115EET1G		80	150	–	
	LDTA144WET1G		80	140	–	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_E = 0.3 mA)		$V_{CE(sat)}$	–	–	0.25	Vdc
(I_C = 10 mA, I_B = 5 mA)	LDTA123EET1G					
(I_C = 10 mA, I_B = 1 mA)	LDTA114TET1G/LDTA143TET1G					
	LDTA143ZET1G/LDTA124XET1G					
	LDTA143EET1G					
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	LDTA114EET1G		–	–	0.2	
	LDTA124EET1G		–	–	0.2	
	LDTA114YET1G		–	–	0.2	
	LDTA114TET1G		–	–	0.2	
	LDTA143TET1G		–	–	0.2	
	LDTA123EET1G		–	–	0.2	
	LDTA143EET1G		–	–	0.2	
	LDTA143ZET1G		–	–	0.2	
	LDTA124XET1G		–	–	0.2	
	LDTA123JET1G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	LDTA144EET1G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	LDTA115EET1G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	LDTA144WET1G		–	–	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	–	–	Vdc
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	LDTA114TET1G					
	LDTA143TET1G					
	LDTA123EET1G					
	LDTA143EET1G					
Input Resistor	LDTA114EET1G	R1	7.0	10	13	kΩ
	LDTA124EET1G		15.4	22	28.6	
	LDTA144EET1G		32.9	47	61.1	
	LDTA114YET1G		7.0	10	13	
	LDTA114TET1G		7.0	10	13	
	LDTA143TET1G		3.3	4.7	6.1	
	LDTA123EET1G		1.5	2.2	2.9	
	LDTA143EET1G		3.3	4.7	6.1	
	LDTA143ZET1G		3.3	4.7	6.1	
	LDTA124XET1G		15.4	22	28.6	
	LDTA123JET1G		1.54	2.2	2.86	
	LDTA115EET1G		70	100	130	
	LDTA144WET1G		32.9	47	61.1	
Resistor Ratio		R_1/R_2				–
	LDTA114EET1G/LDTA124EET1G					
	LDTA144EET1G/LDTA115EET1G		0.8	1.0	1.2	
	LDTA114YET1G		0.17	0.21	0.25	
	LDTA114TET1G/LDTA143TET1G		–	–	–	
	LDTA123EET1G/LDTA143EET1G		0.8	1.0	1.2	
	LDTA143ZET1G		0.055	0.1	0.185	
	LDTA124XET1G		0.38	0.47	0.56	
	LDTA123JET1G		0.038	0.047	0.056	
	LDTA144WET1G		1.7	2.1	2.6	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

LDTA114EET1G Series

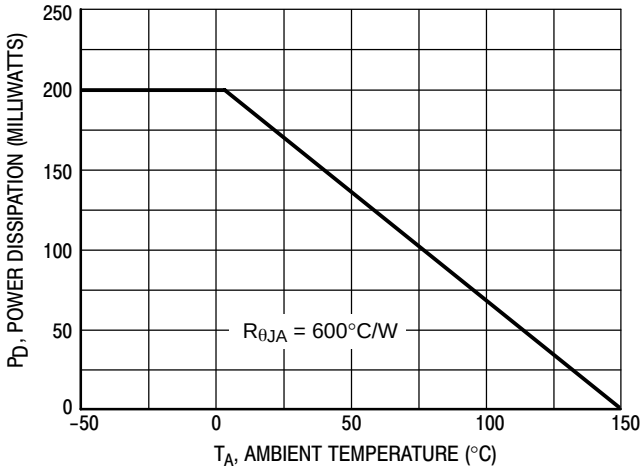


Figure 1. Derating Curve

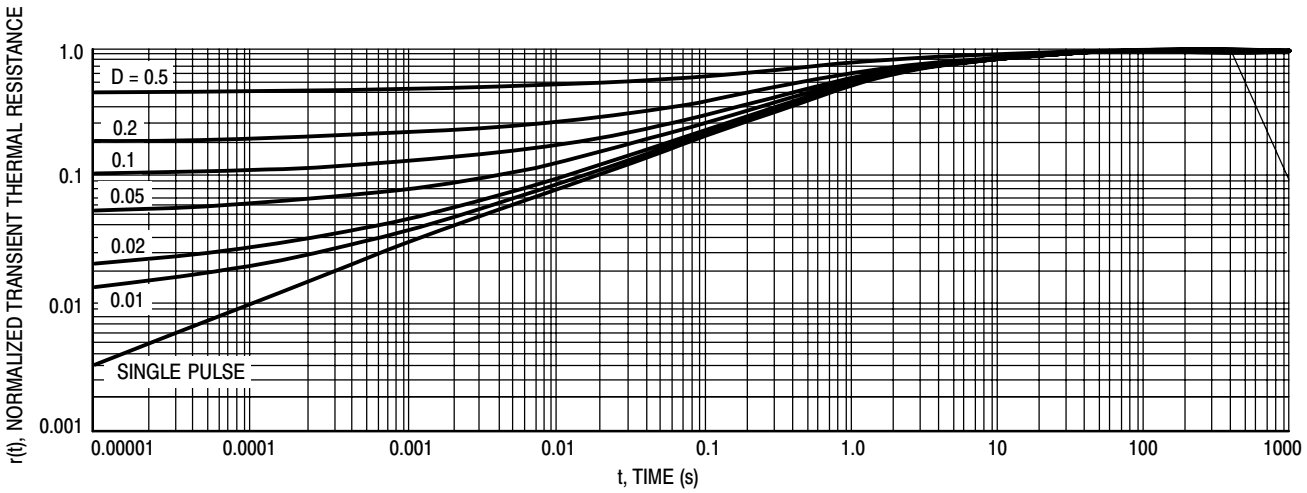


Figure 2. Normalized Thermal Response

LDTA114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTA114EET1G

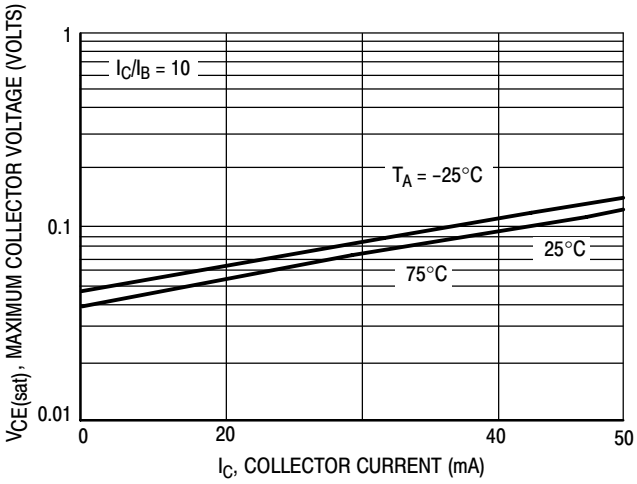


Figure 3. $V_{CE(sat)}$ versus I_C

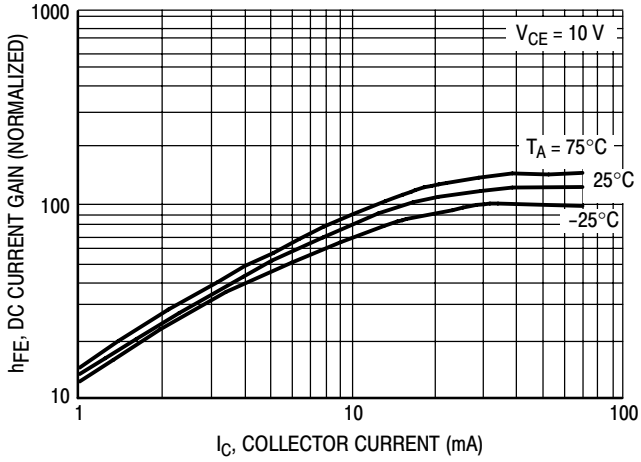


Figure 4. DC Current Gain

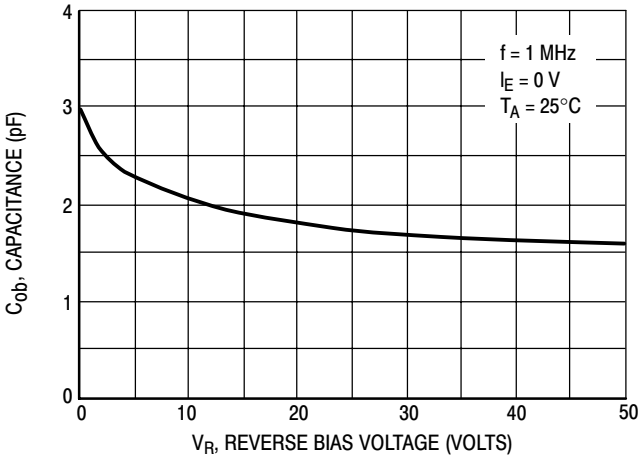


Figure 5. Output Capacitance

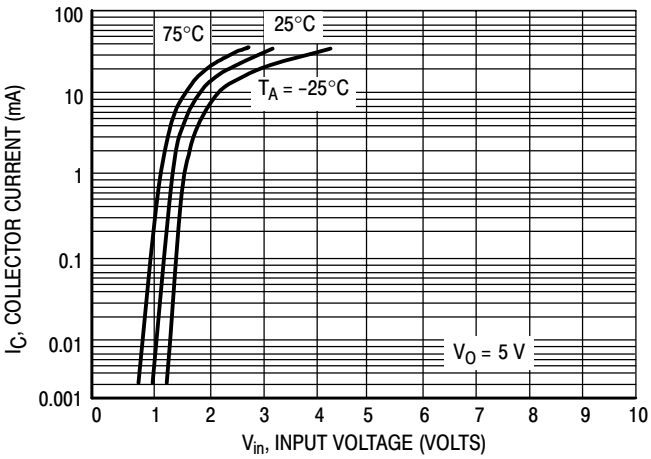


Figure 6. Output Current versus Input Voltage

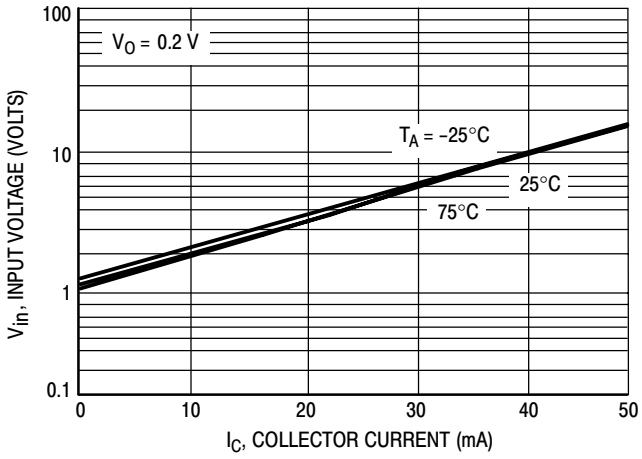


Figure 7. Input Voltage versus Output Current

LDTA114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTA123EET1G

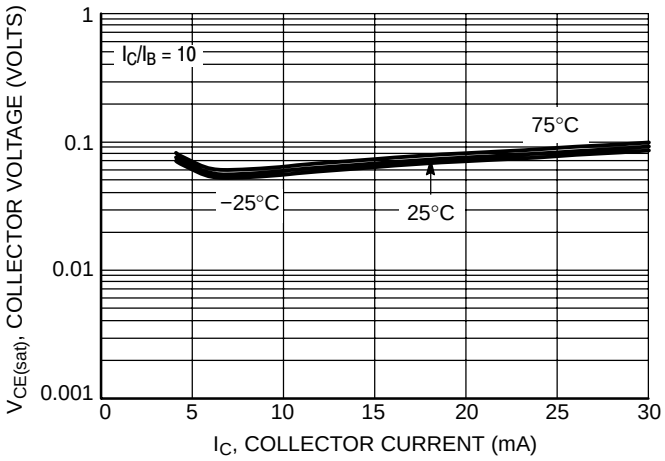


Figure 8. $V_{CE(sat)}$ versus I_C

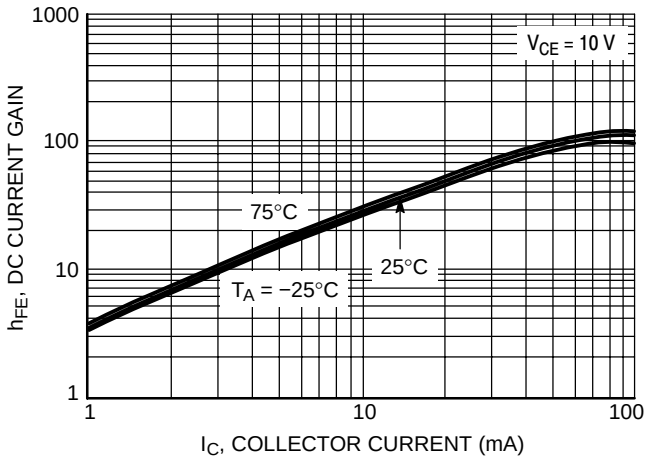


Figure 9. DC Current Gain

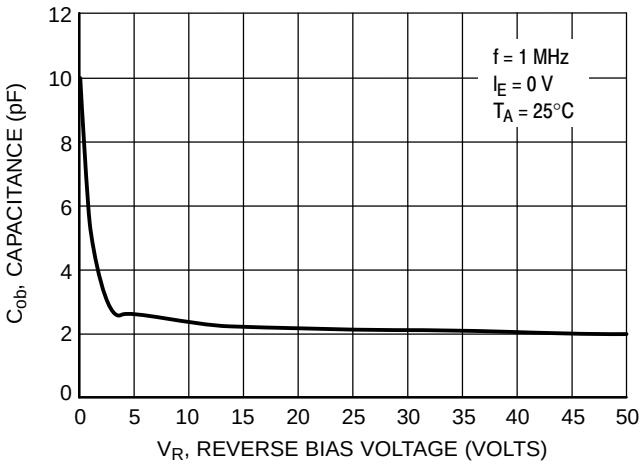


Figure 10. Output Capacitance

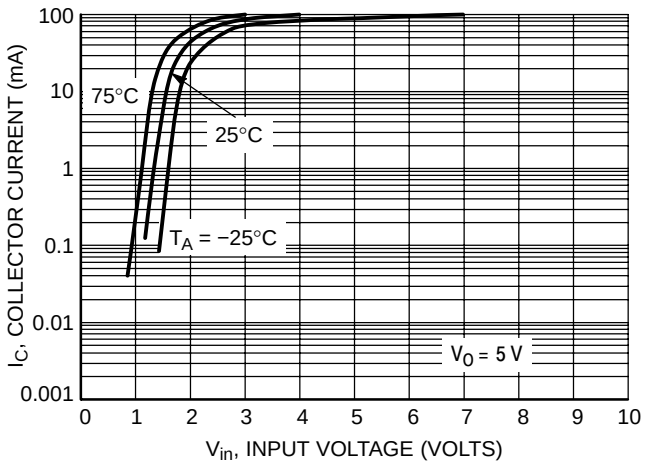


Figure 11. Output Current versus Input Voltage

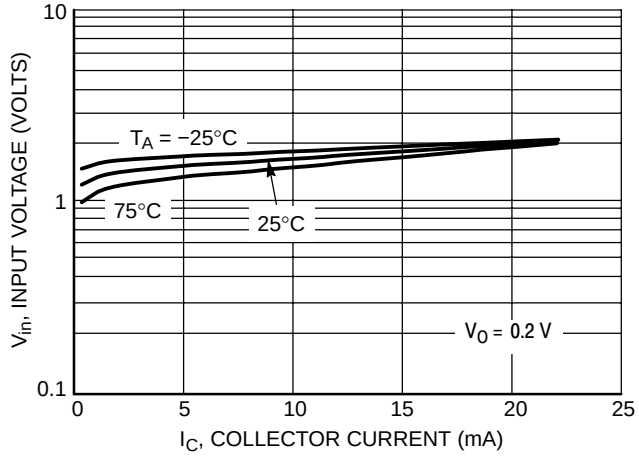


Figure 12. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − LDTA124EET1G

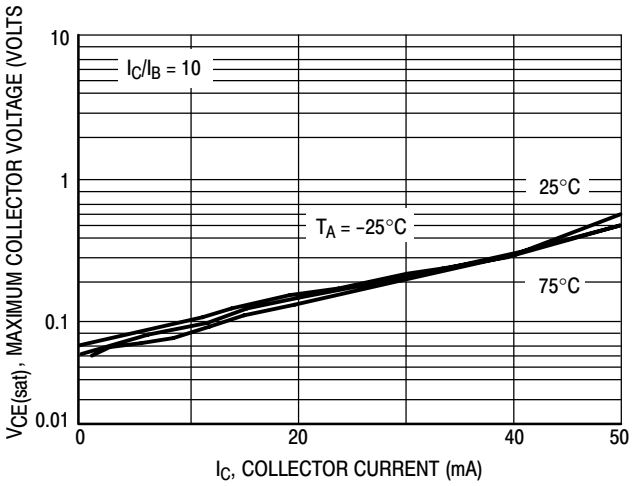


Figure 13. $V_{CE(sat)}$ versus I_C

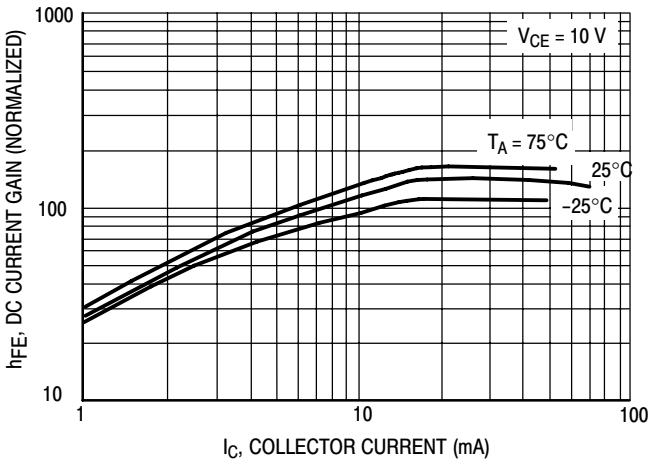


Figure 14. DC Current Gain

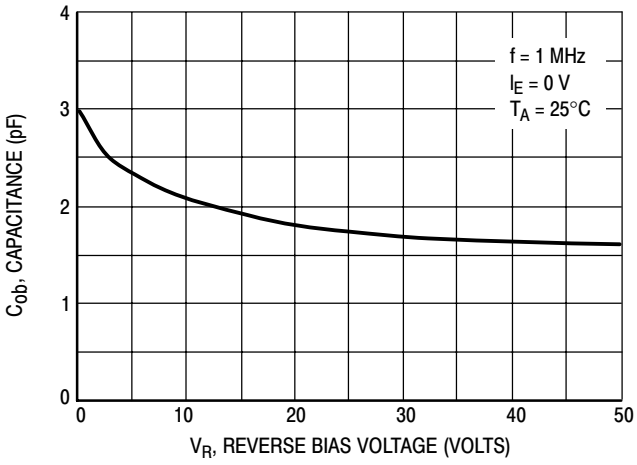


Figure 15. Output Capacitance

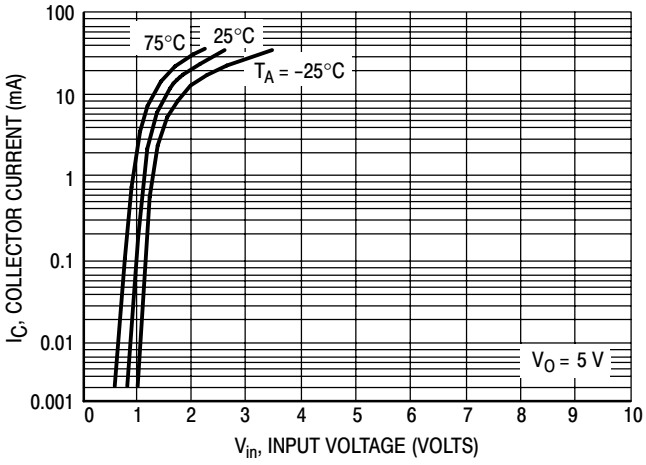


Figure 16. Output Current versus Input Voltage

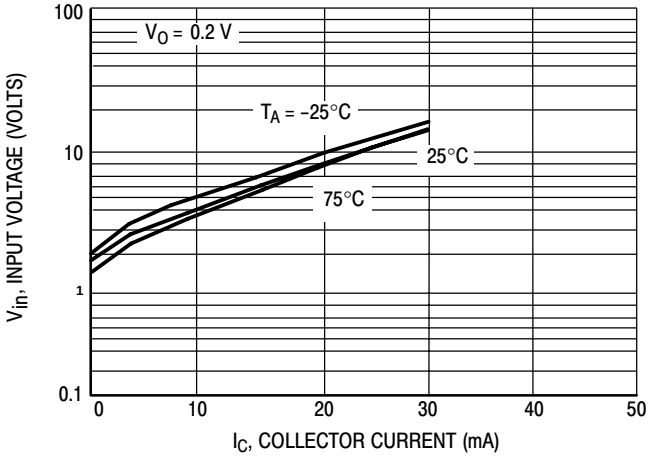


Figure 17. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − LDTA144EET1G

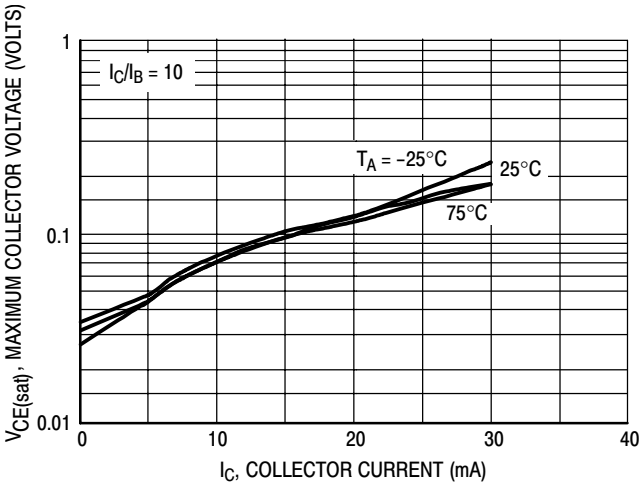


Figure 18. $V_{CE(sat)}$ versus I_C

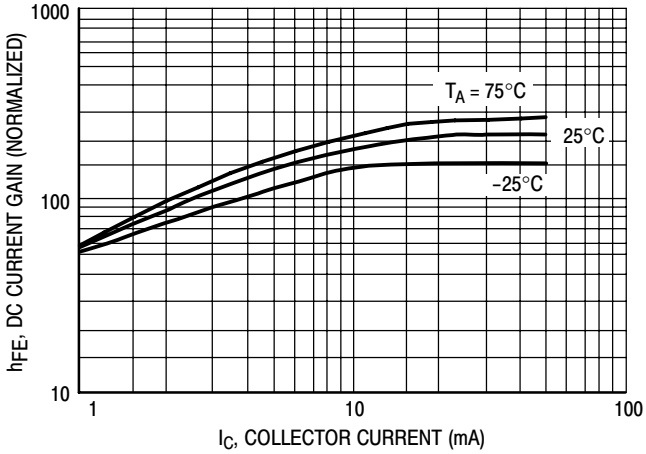


Figure 19. DC Current Gain

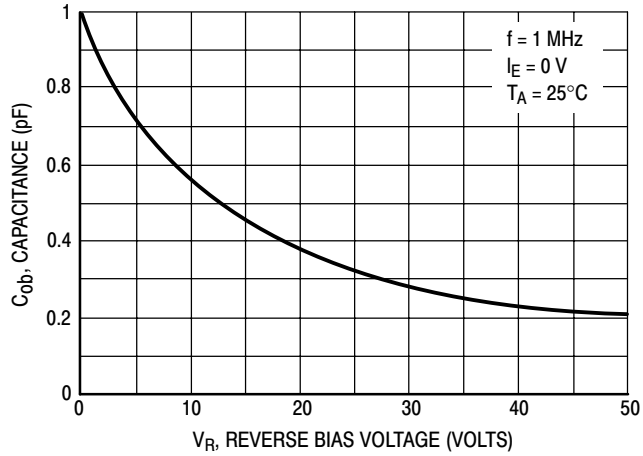


Figure 20. Output Capacitance

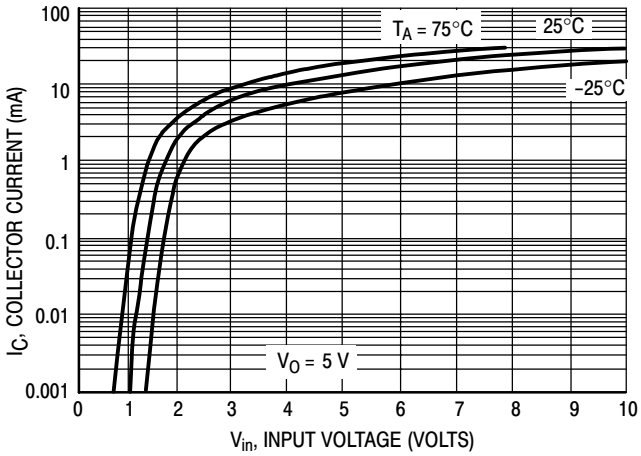


Figure 21. Output Current versus Input Voltage

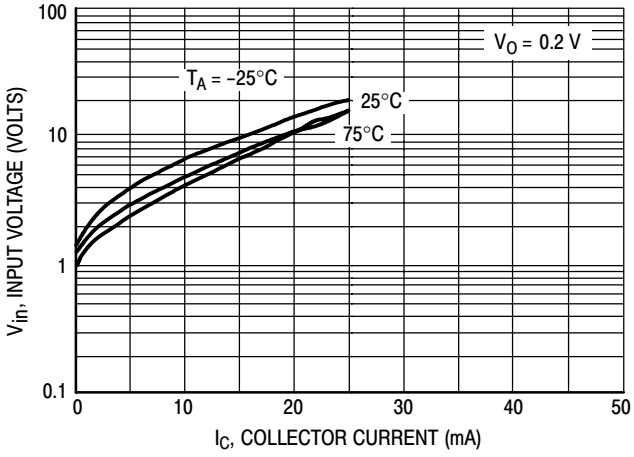


Figure 22. Input Voltage versus Output Current

LDTA114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTA114YET1G

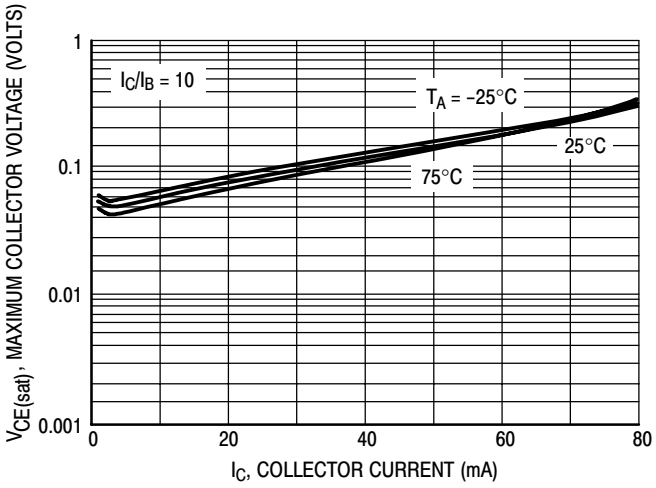


Figure 23. $V_{CE(sat)}$ versus I_C

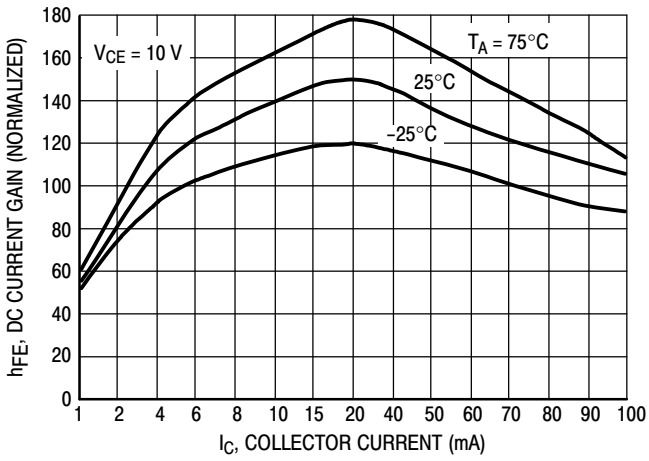


Figure 24. DC Current Gain

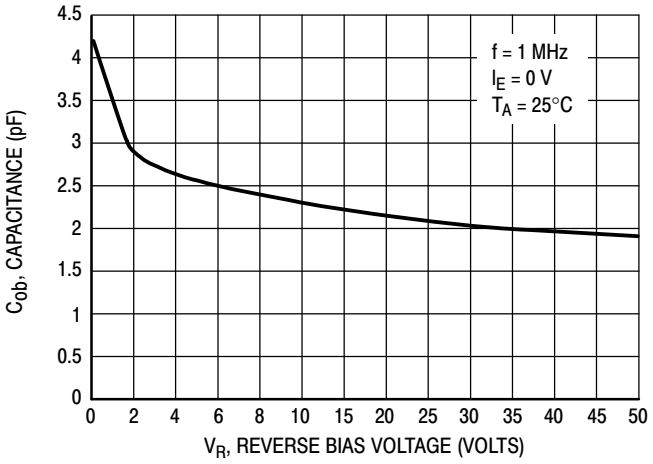


Figure 25. Output Capacitance

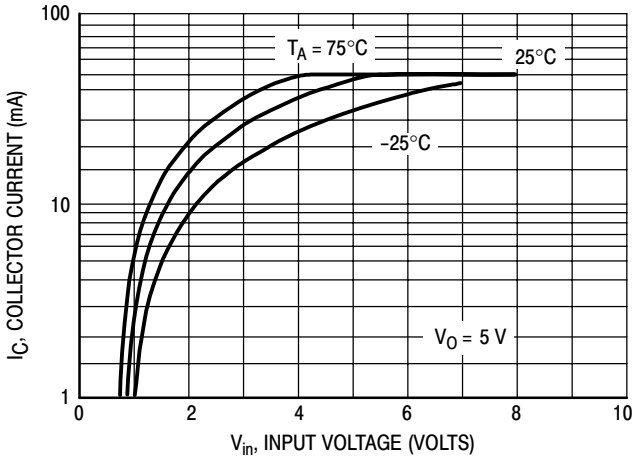


Figure 26. Output Current versus Input Voltage

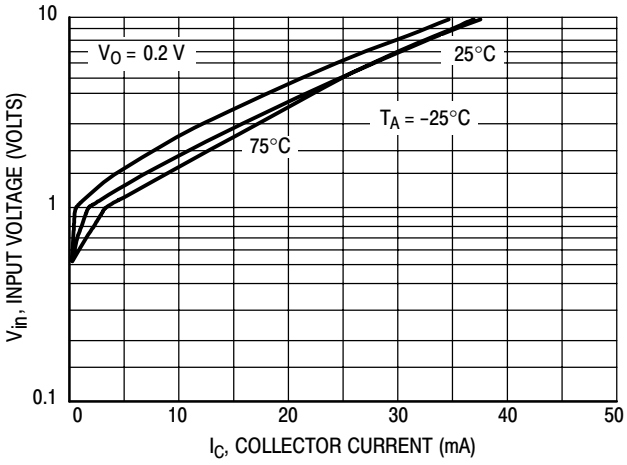


Figure 27. Input Voltage versus Output Current

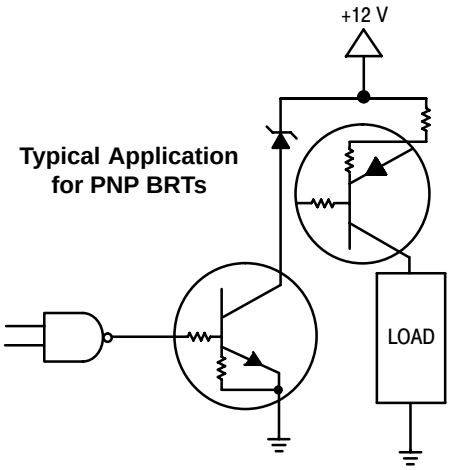


Figure 28. Inexpensive, Unregulated Current Source

LDTA114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LDTA115EET1G

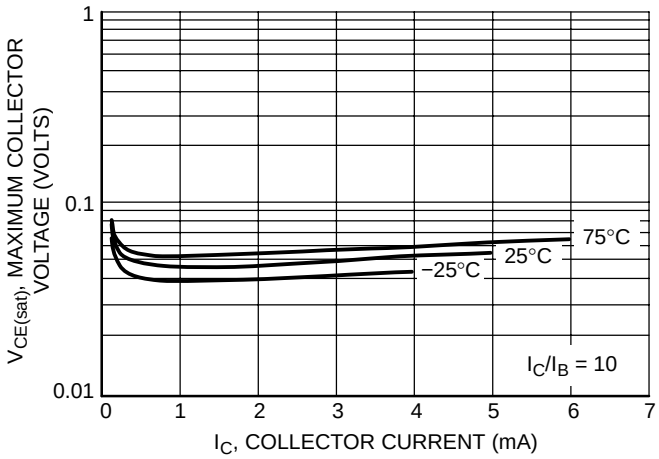


Figure 29. Maximum Collector Voltage versus Collector Current

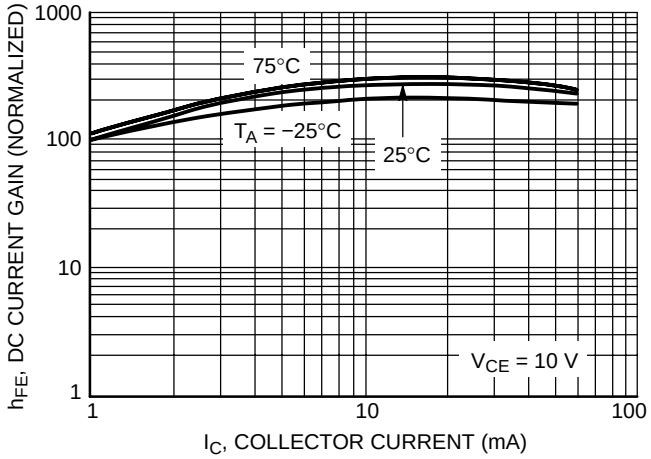


Figure 30. DC Current Gain

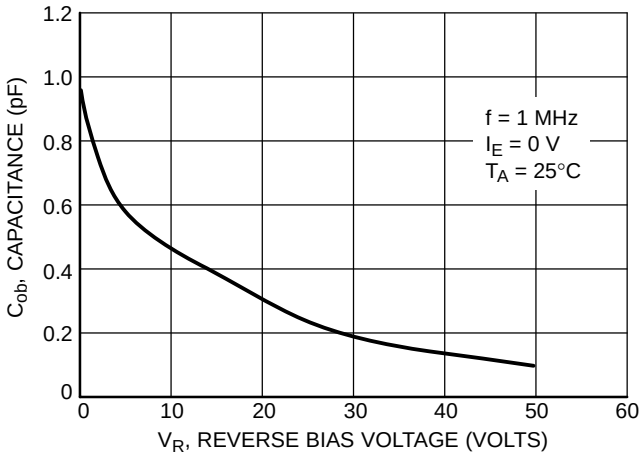


Figure 31. Output Capacitance

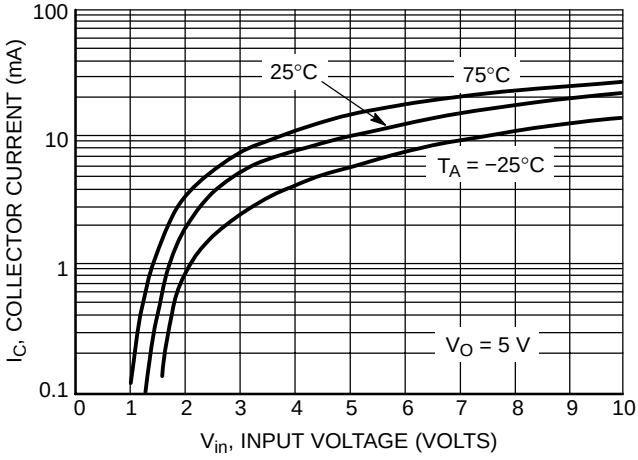


Figure 32. Output Current versus Input Voltage

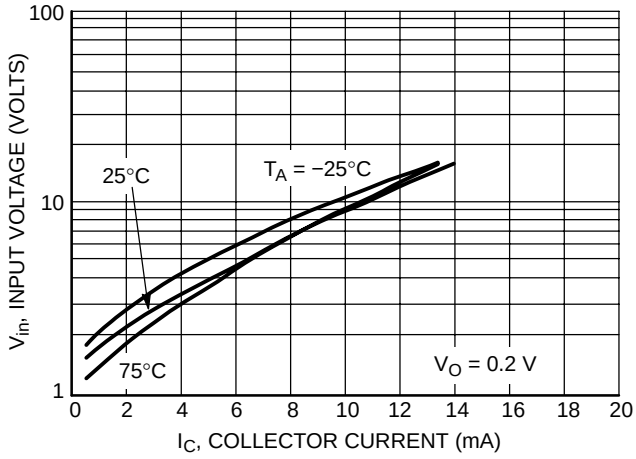


Figure 33. Input Voltage versus Output Current

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TYPICAL ELECTRICAL CHARACTERISTICS — LDTA144WET1G

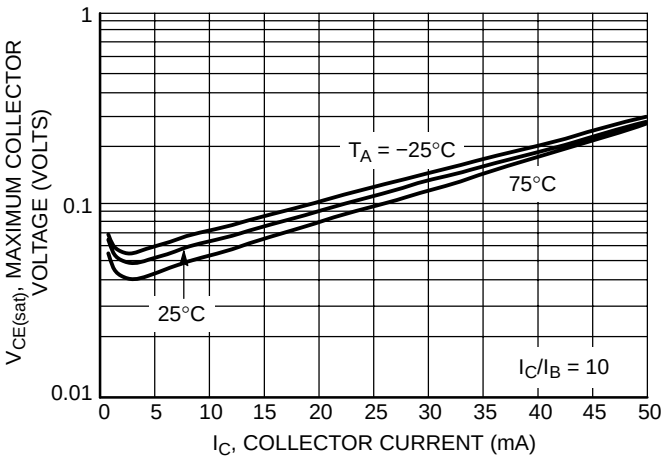

Figure 34. Maximum Collector Voltage versus Collector Current

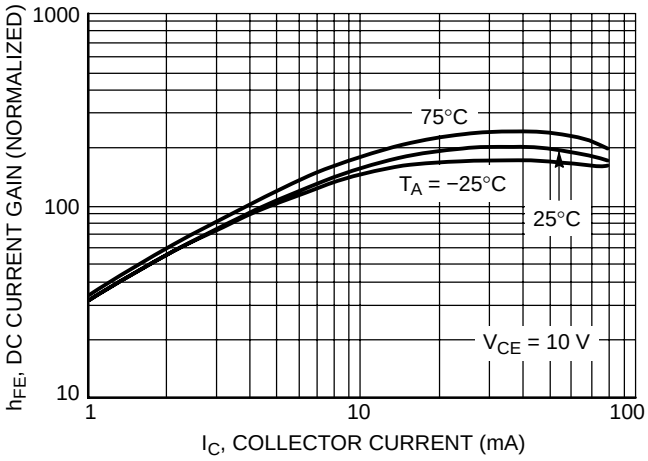

Figure 35. DC Current Gain

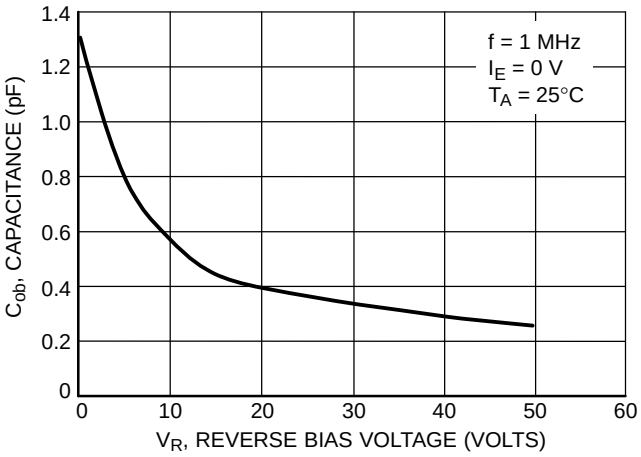

Figure 36. Output Capacitance

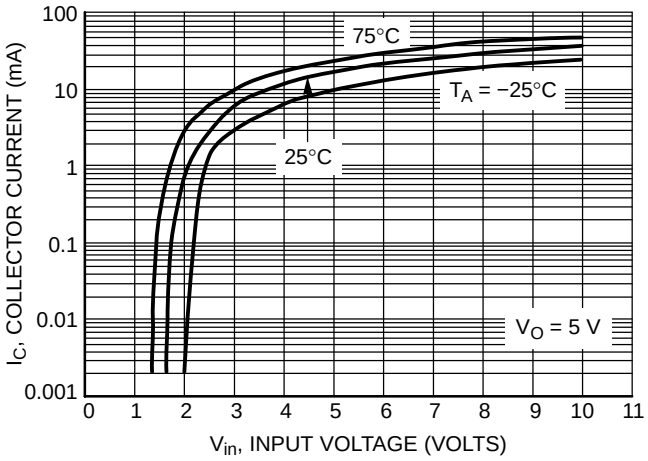

Figure 37. Output Current versus Input Voltage

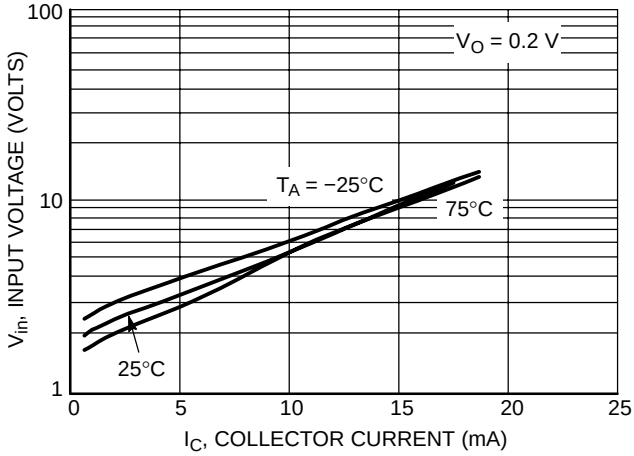

Figure 38. Input Voltage versus Output Current

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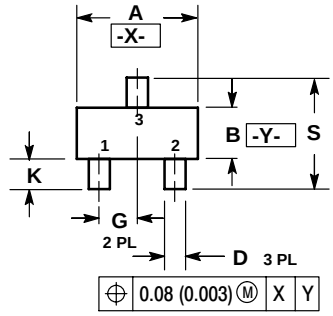
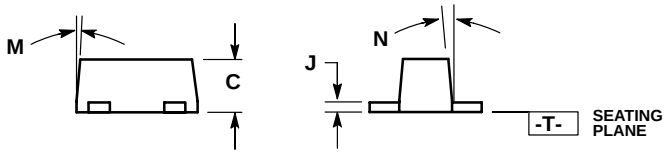
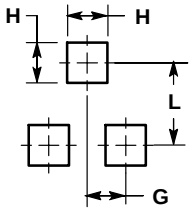




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G		0.50 BSC			0.020 BSC	
H		0.53 REF			0.021 REF	
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L		1.10 REF			0.043 REF	
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS