Build in EQ Function 25W Class-D Audio Amplifier With AGC function

General Description

The LPA2100 is a mono efficient, digital amplifier power stage for driving speakers up to 25W/4Ω. The LPA2100 integrates AGC(automatic gain control)circuit for a NCN(Non-Crack Noise) technical in application without damaging speaker when a high power signal occurs. When function failed happened to input capacitor, the chip will cut off the output circuit through detecting the input signal to protect speaker. The LPA2100 device is fully protected against faults with short-circuit protection and thermal protection as well as over-voltage and DC protection. Faults are reported back to the processor to prevent devices form being damaged during overload conditions.

Features

- 15W Output at 0.1% THD with a 4Ω Load and12.0V PVCC for amplifier
- Wide voltage range: 4.5V~15V
- Integrated 2 degree AGC circuit
- Integrated Self-Protection Circuits Including Over-Voltage, Under-Voltage, Over-Temperature, DC-Detect, and Short Circuit
- Multiple Switching Frequencies
  - AM Avoidance
  - Master/Slave Synchronization
  - Up to 450KHz Switching Frequency
- High Efficient Class-D Operation: >90%
- Indication for NCN(Non-Crack Noise)
- Pb-Free Package

Order Information

LPA2100 □ □ □ □

- F: Pb-Free
- Package Type
  - TS : ETSSOP-24
  - SP : ESOP16
- Mute type :
  - A : Active Low
  - Default : Active High

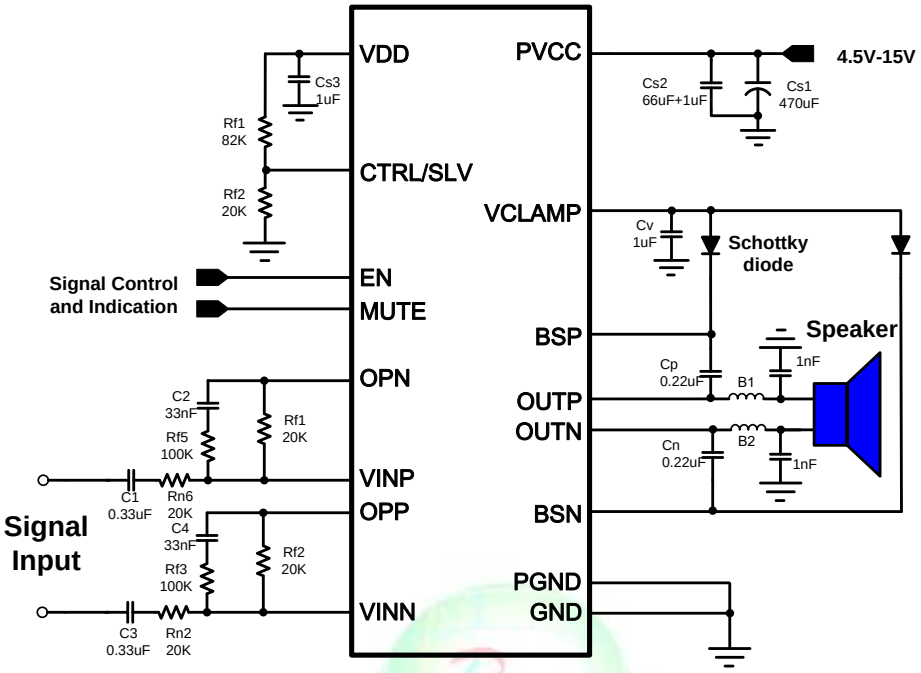
Marking Information

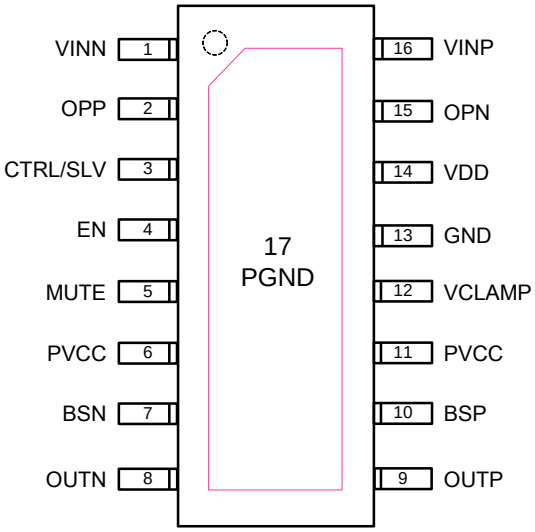
Device	Marking	Package	Shipping
LPA2100A	LPS LPA2100A YWX	ETSSOP-24 ESOP16	xxxK/REEL
LPA2100	LPS LPA2100 YWX	ETSSOP-24 ESOP16	xxxK/REEL
Y: Y is year code. W: W is week code. X: X is series number.			

Applications

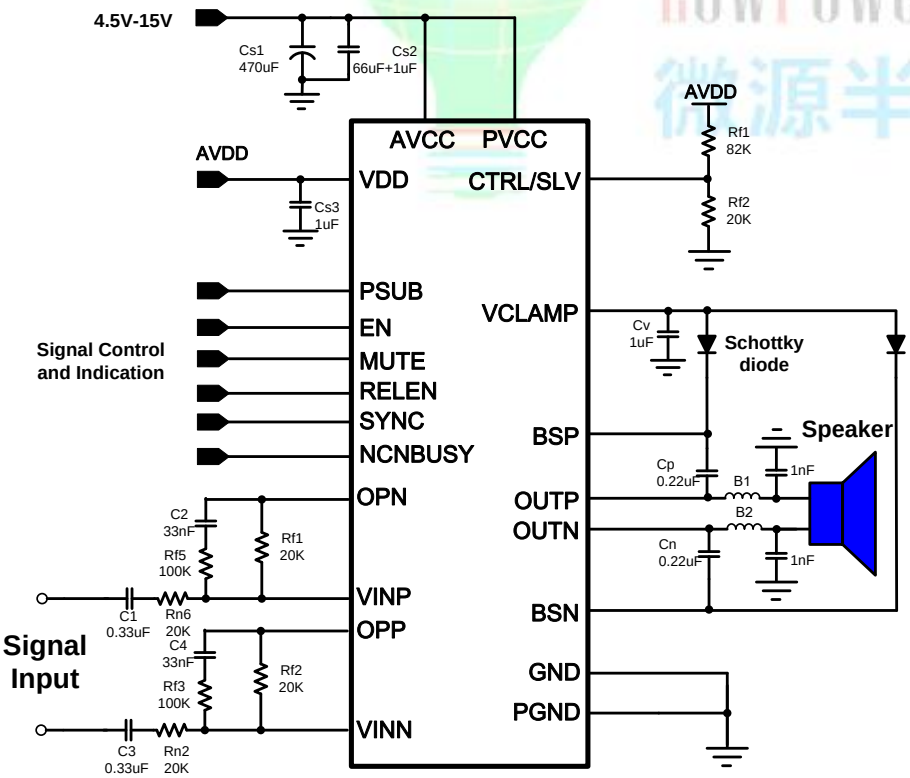
- Mini-Micro Component, Speaker Bar, Docks
- After-Market Automotive
- Consumer Audio Applications, CRT TV
- Portable Bluetooth Speaker
- Cellular and Smart mobile phone
- Square Speaker

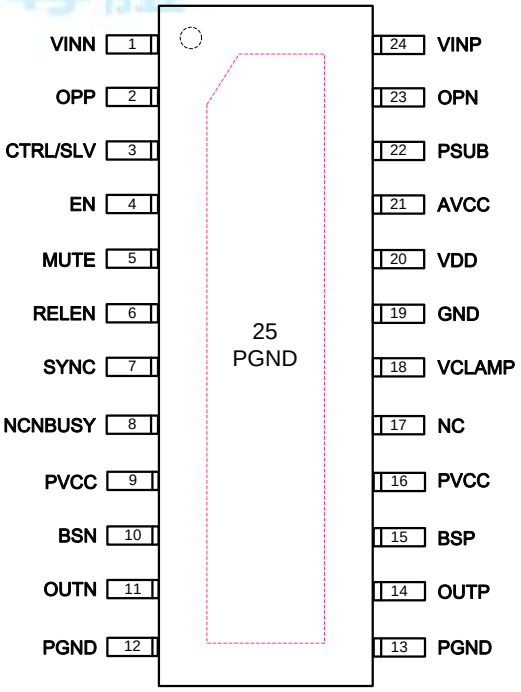
Typical Application Circuit





ESOP16



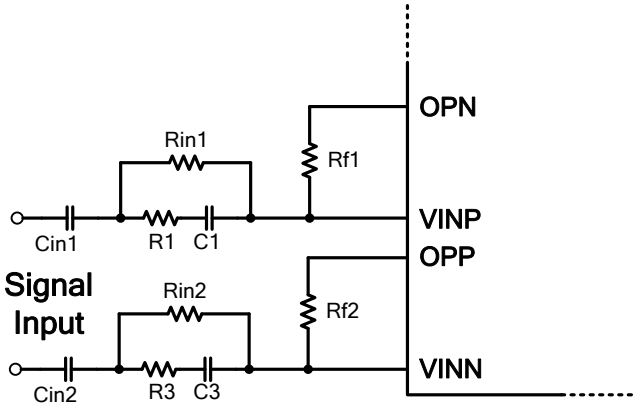


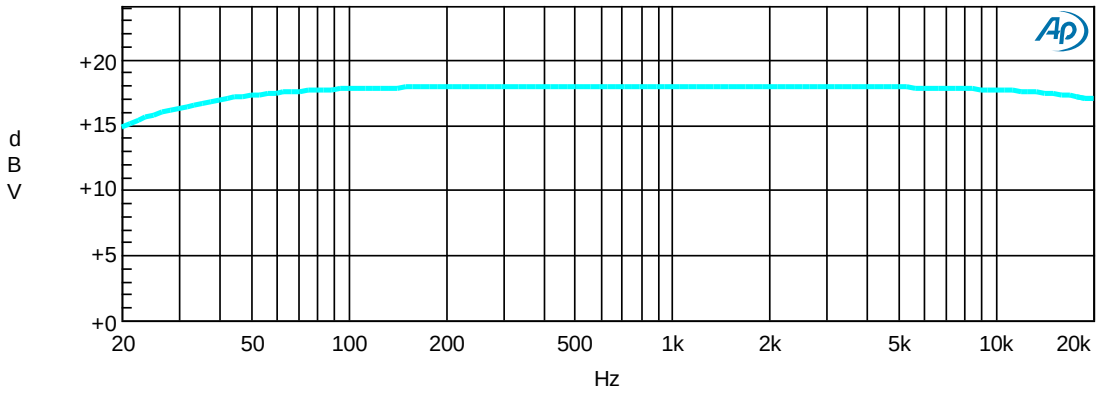
TSSOP-24

Functional Pin Description

TSSOP-24 Pin Num	ESOP16 Pin Num	Pin Name	Description
1	1	VINN	Negative signal input.
2	2	OPP	Positive signal output.
3	3	CTRL/SLV	AGC control and selects between Master and Slave mode depending on pin voltage divider. Show detail in sheet 1.
4	4	EN	Chip enable pin. Active high.
5	5	MUTE	Mute control. LPA2100A active high，LPA2100 active low.
6		RELEN	Crack Noise release pin. Active low.
7		SYNC	Clock input/output for synchronizing multiple class-D devices. Determined by CTRL/SLV pin. Show detail in sheet 1.
8		NCNBUSY	Indication of Crack Noise. Chip keeps output pulse through this pin when Crack occurs. Show detail in sheet 1.
9	6	PVCC	Power supply for chip.
10	7	BSN	Negative self boost output pin. There is a 220nF capacitor between this pin and OUTN.
11	8	OUTN	Negative output.
12,13,25	17	PGND	Power ground.
14	9	OUTP	Positive output.
15	10	BSP	Negative self boost output pin. There is a 220nF capacitor between this pin and OUTN.
16	11	PVCC	Power supply for chip.
17		NC	Floating pin.
18	12	VCLAMP	Supply for internal Power MOS. There should be a 1uF capacitor between this pin and GND.
19	13	GND	Analog ground.
20	14	VDD	Internal power supply. There should be a 1uF capacitor between this pin and GND.
21		AVCC	Analog power supply.
22		PSUB	Substrate voltage.
23	15	OPN	Negative signal output.
24	16	VINP	Positive signal input.

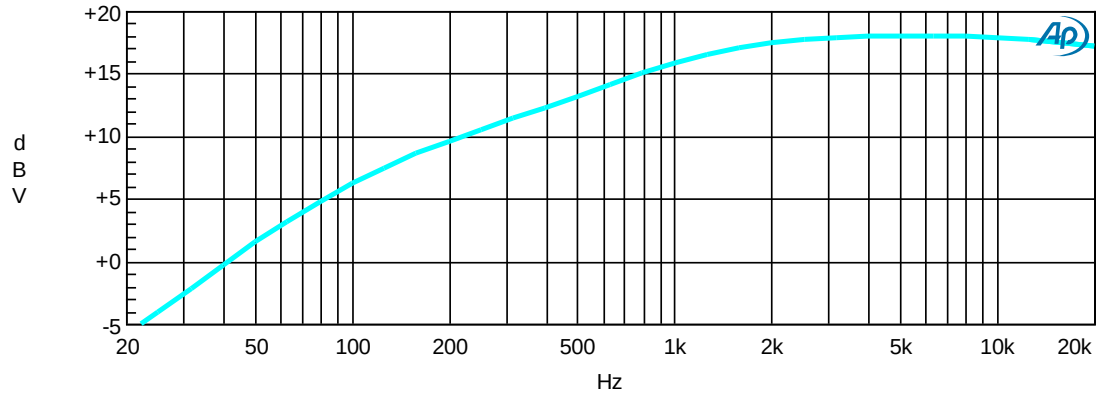
Classical Application 1: Low Restraint





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

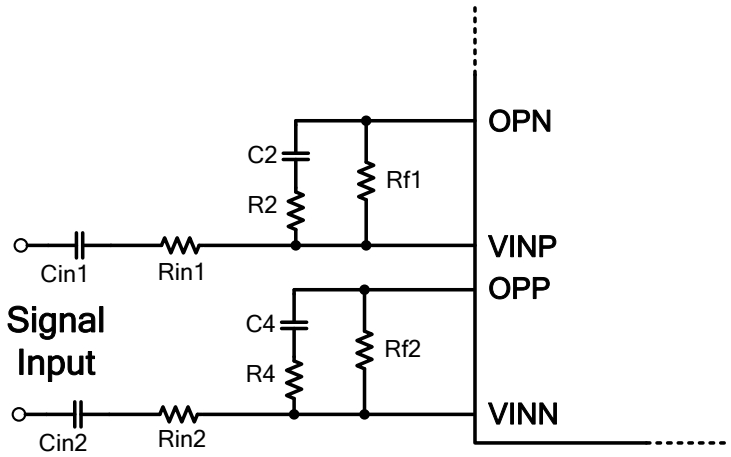
Cin1/2=1uF; Rin1/2=20K; R1/3=NC; C1/3=NC; Rf1/2=47K

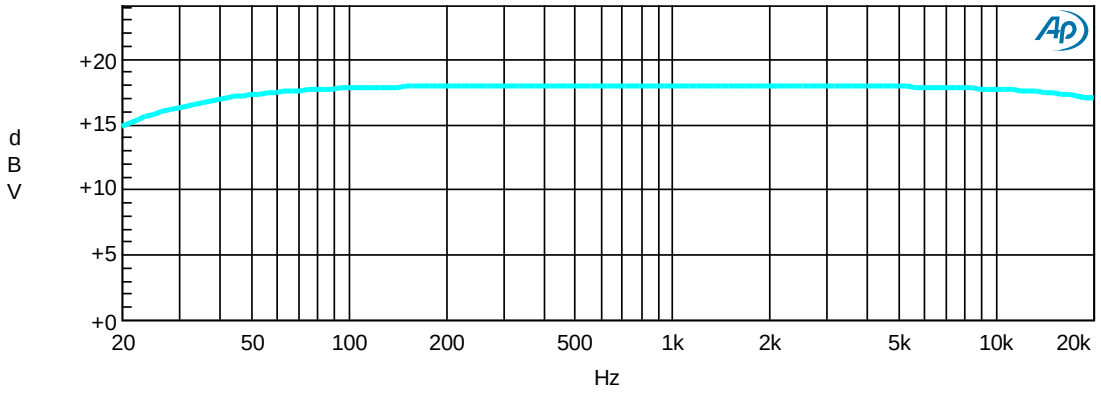


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=47nF; Rin1/2=20K; R1/3=20K;C1/3=10nF; Rf1/2=47K

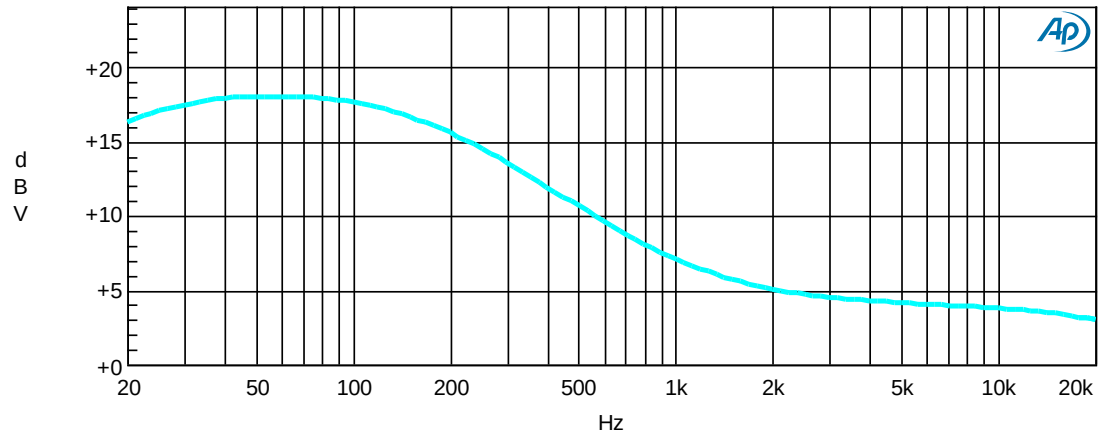
Classical Application 2: High Restraint





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

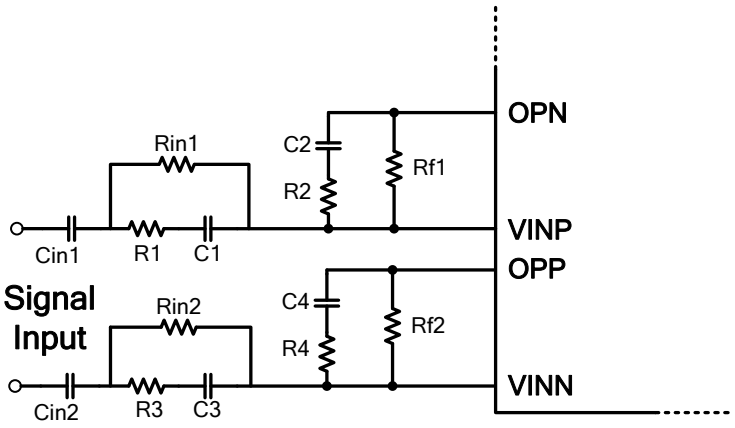
Cin1/2=1uF; Rin1/2=20K; C2/4=NC; R2/4=NC; Rf1/2=47K

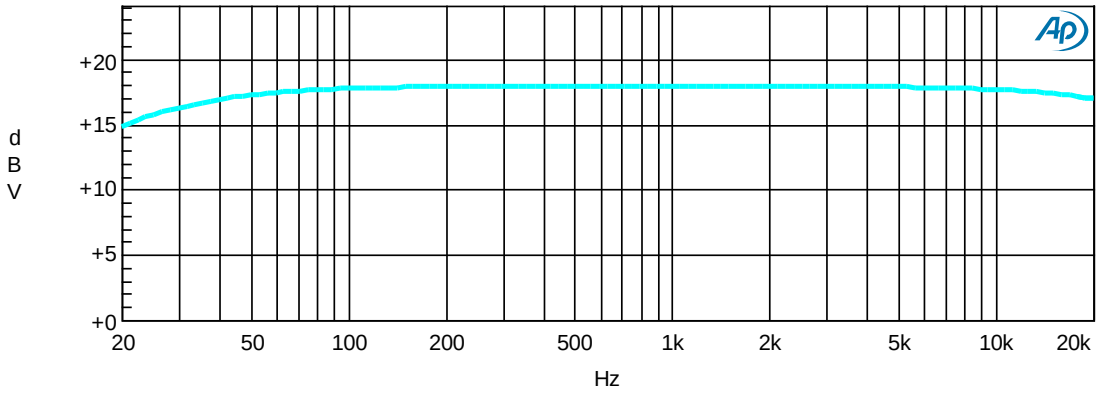


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=0.47uF; Rin1/2=20K; C2/4=15nF; R2/4=10K; Rf1/2=47K

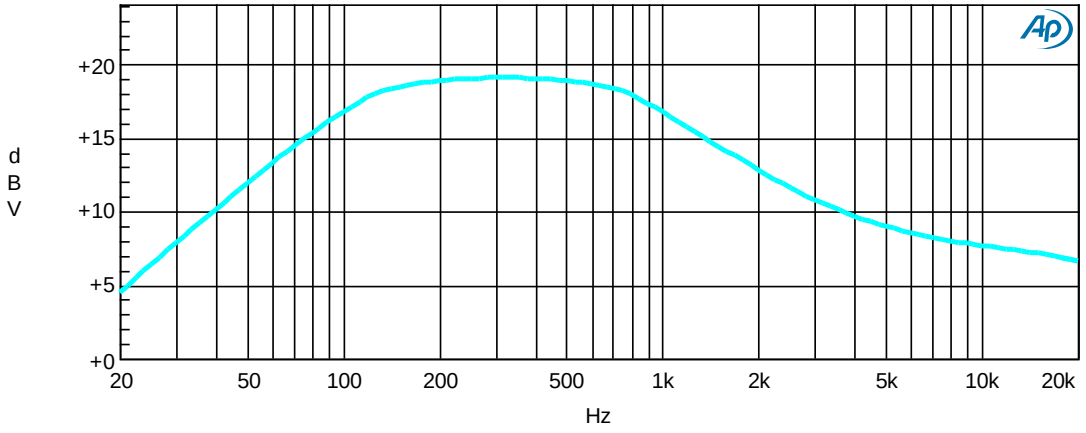
Classical Application 3: High and Low Restraint (Band Pass)





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=1uF; Rin1/2=20K;R1/3=NC; C1/3=NC; C2/4=NC; R2/4=NC; Rf1/2=47K



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=0.47uF; Rin1/2=20K; R1/3=20K; C2/4=10nF; R2/4=10K; Rf1/2=47K

Absolute Maximum Ratings Note 1

- ✧ Supply Voltage to GND ---------- -0.3V to 18V
- ✧ Other Pin to GND ---------- -0.3V to 6V
- ✧ Maximum Junction Temperature ---------- 150°C
- ✧ Operating Ambient Temperature Range (Ta) ---------- -40℃ to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (TSSOP-24, PD,TA=25°C) ---------- 3.4W
- ✧ Thermal Resistance (TSSOP-24, JA) ---------- 36℃/W
- ✧ Maximum Power Dissipation (ESOP-16, PD,TA=25°C) ---------- 1.9W
- ✧ Thermal Resistance (ESOP-16, JA) ---------- 65℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) Note 2 ---------- 2KV
- ✧ MM(Machine Mode) Note 3 ---------- 200V

Note 2. The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDEC.

Note 3. Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDEC.

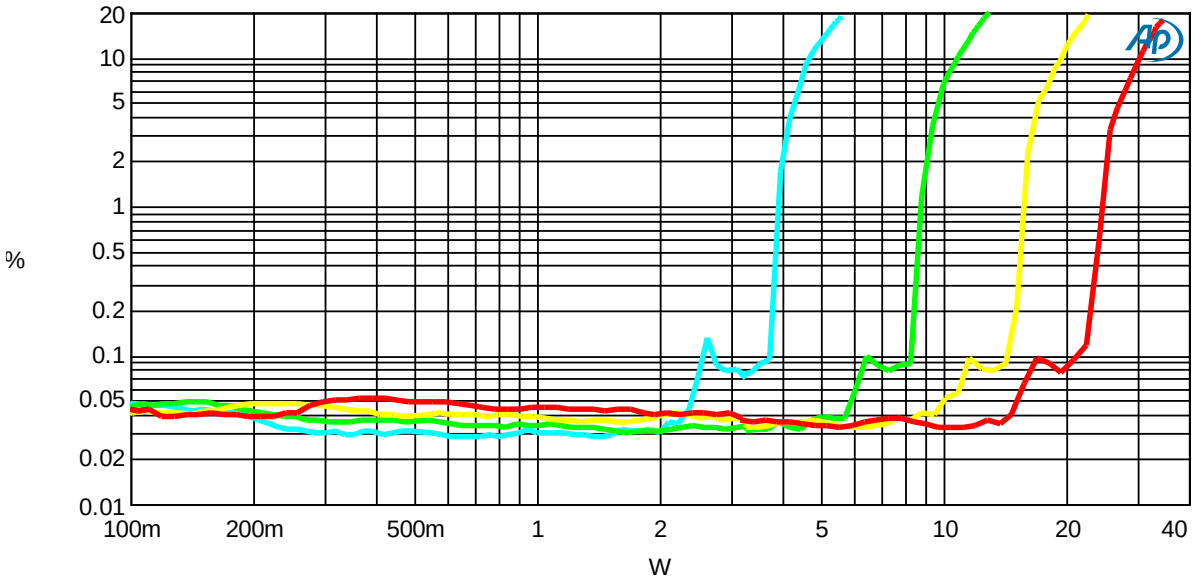
Electrical Characteristics

(T_A = 25°C, AV_{CC} = PV_{CC} = 12 V, R_L = 4 Ω, unless otherwise noted)

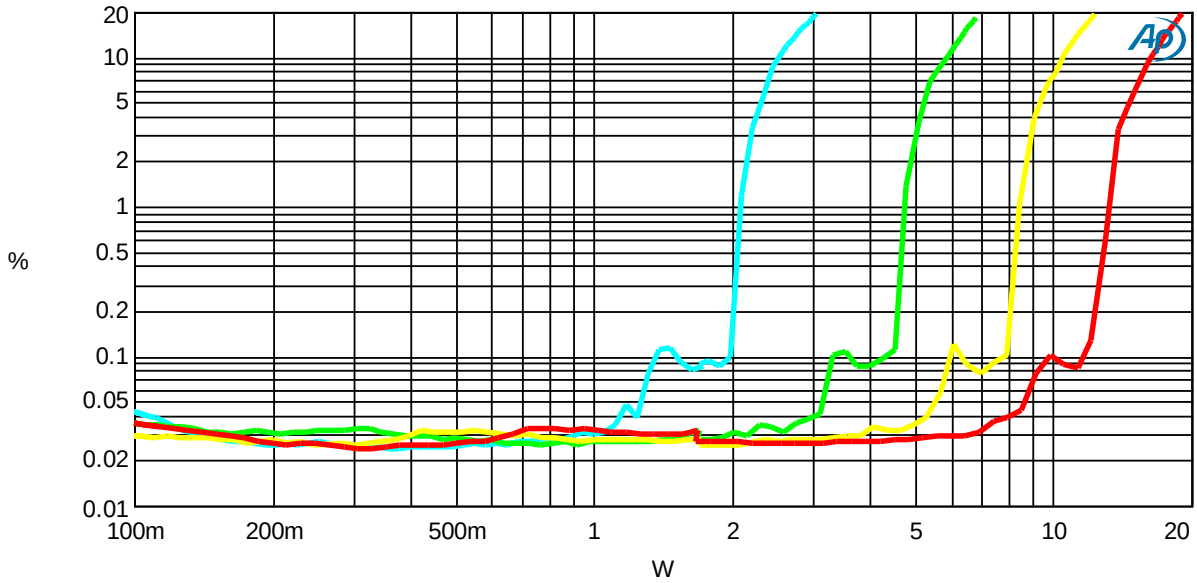
Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Supply power	PVCC			4.5		15	V
Output power	P_O	THD+N=10%, f=1KHz,RL=4Ω	PVCC=12V		18		W
			PVCC=14V		25		
		THD+N=10%, f=1KHz,RL=8Ω	PVCC=12V		10.5		
			PVCC=14V		14.3		
		THD+N=1%, f=1KHz,RL=4Ω	PVCC=12V		16		
			PVCC=14V		20		
		THD+N=1%, f=1KHz,RL=8Ω	PVCC=12V		8.5		
			PVCC=14V		11.6		
Power supply ripple rejection	PSRR	INPUT ac-grounded with CIN=0.47uF, PVCC=12V	f=100HZ		70		dB
			f=1KHz		73		
Signal-to-noise ratio	SNR	PVCC=12V,P_{OUT}=12W,R_L =4Ω	f=1KHz		95		dB
Efficiency	η	R_L=4Ω,P_O=12W	f=1KHz		91		%
Output integrated noise	Vn	22 Hz to 20kHz, A-weighted filter, Gain = 26dB			130		uV
Quiescent current	I_Q	PVCC=12V，No load			12		mA
Shutdown current	I_{SD}	PVCC=12V			2		uA
Internal power supply	VDD	PVCC=12V			5.1		V
Supply for internal Power MOS	VCLAMP	PVCC=12V			6.09		V
EN supply voltage(min)		PVCC=12V			>2.1		V
Shutdown supply current (min)		PVCC=12V			2		uA
MUTE supply voltage(min)		PVCC=12V，LPA2100L			1<		V
MUTE supply voltage(max)		PVCC=12V，LPA2100H			>1.9		V
MUTE supply Current		PVCC=12V			60		uA
Offset output voltage	V_{OS}	PVCC=12V, V_{SD} =0V			5		mV
fOSC Oscillator frequency	fsw	PVCC=5~12V	LPA2100A		350		KHz
			LPA2100		450		

Typical Operating Characteristic For Amplifier

PO VS THD

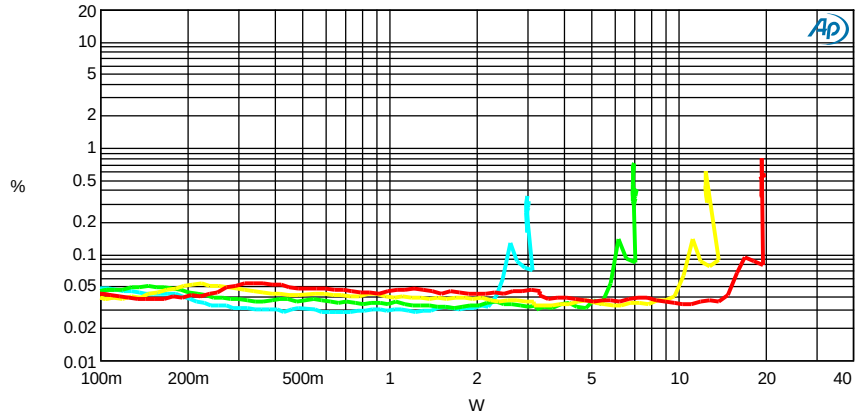


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	6V,4ohm,No NCN
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	9V,4ohm,No NCN
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	12V,4ohm,No NCN
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	15V,4ohm,No NCN

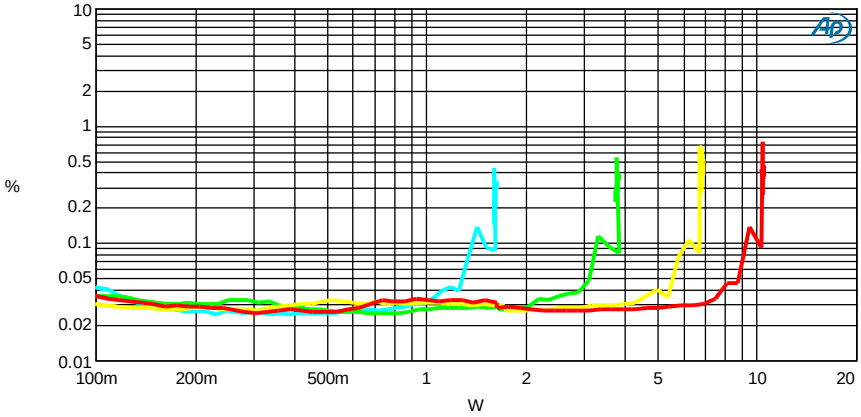


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	6V,8ohm,No NCN
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	9V,8ohm,No NCN
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	12V,8ohm,No NCN
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	15V,8ohm,No NCN

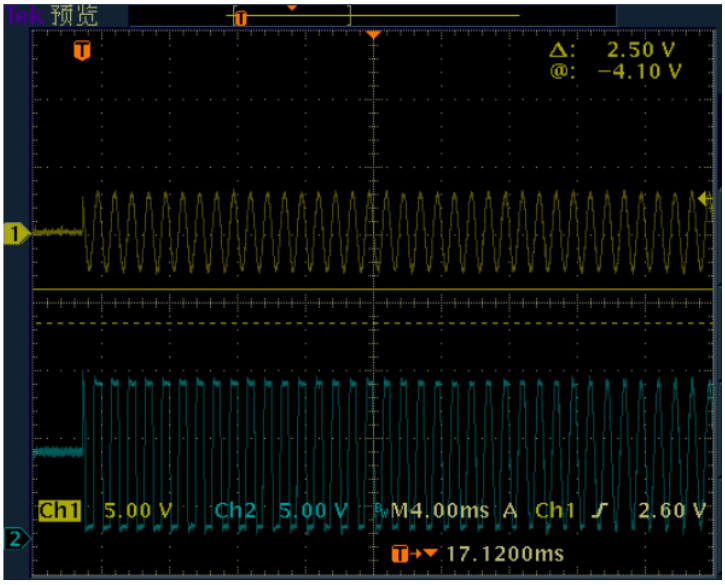
First degree NCN waveform：



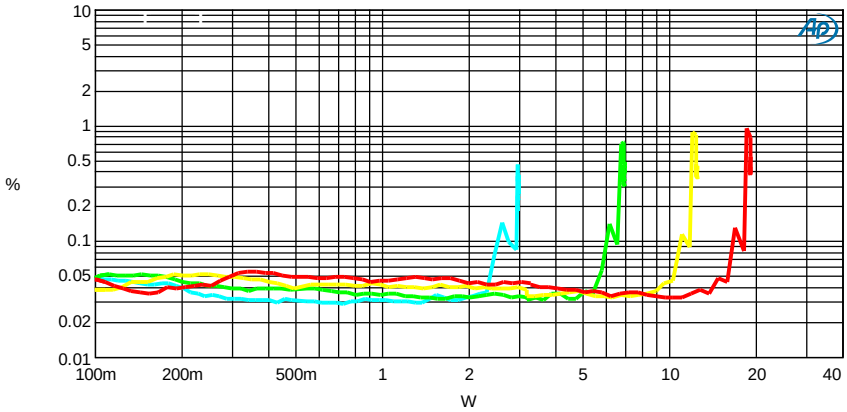
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	6V,4ohm,NCN1
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	9V,4ohm,NCN1
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	12V,4ohm,NCN1
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	15V,4ohm,NCN1



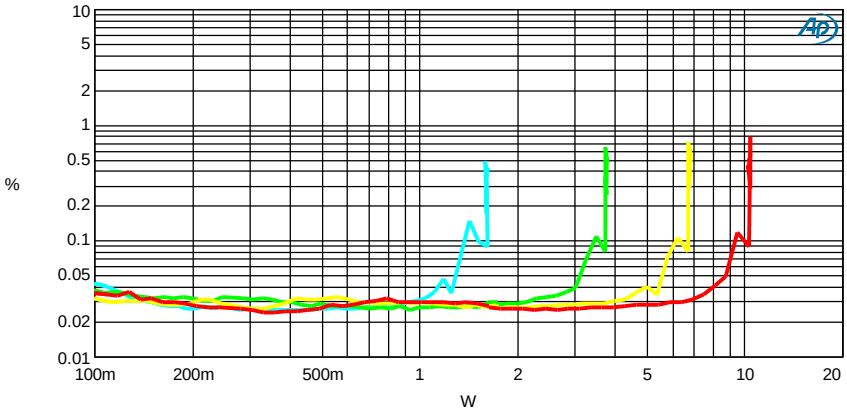
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	6V,8ohm,NCN1
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	9V,8ohm,NCN1
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	12V,8ohm,NCN1
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	15V,8ohm,NCN1



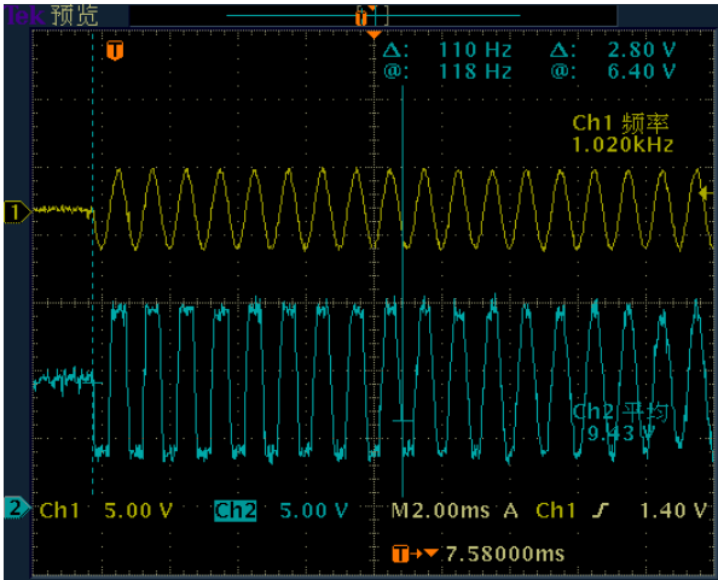
Second degree NCN waveform：



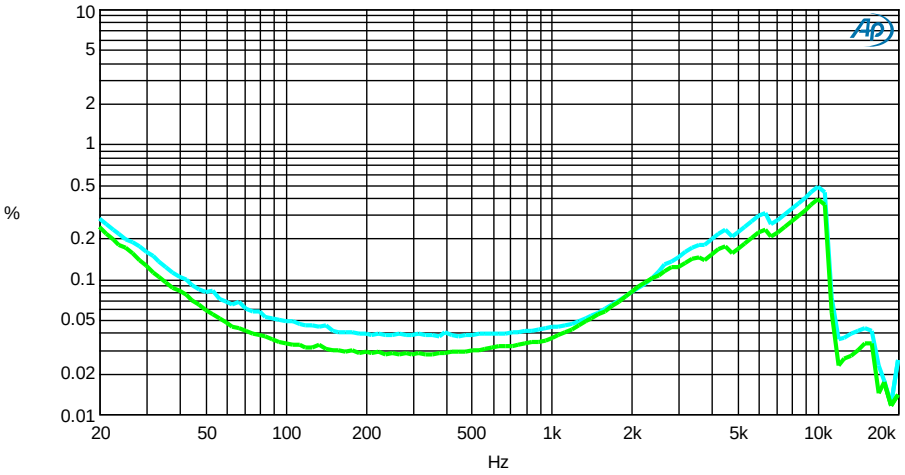
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	6V,4ohm,NCN2
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	9V,4ohm,NCN2
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	12V,4ohm,NCN2
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	15V,4ohm,NCN2



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	6V,8ohm,NCN2
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	9V,8ohm,NCN2
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	12V,8ohm,NCN2
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	15V,8ohm,NCN2

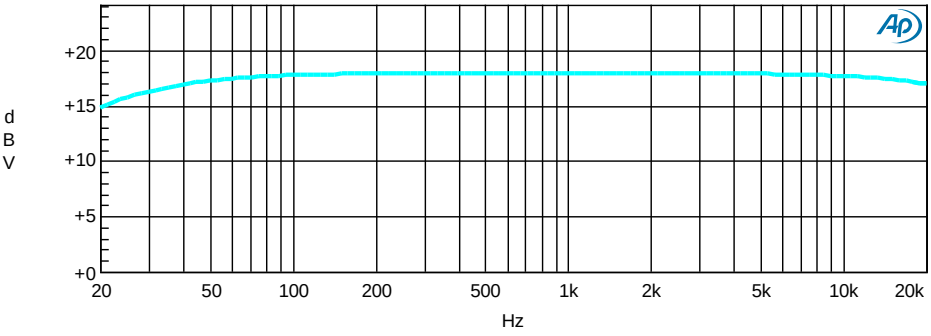


FRQ VS THD



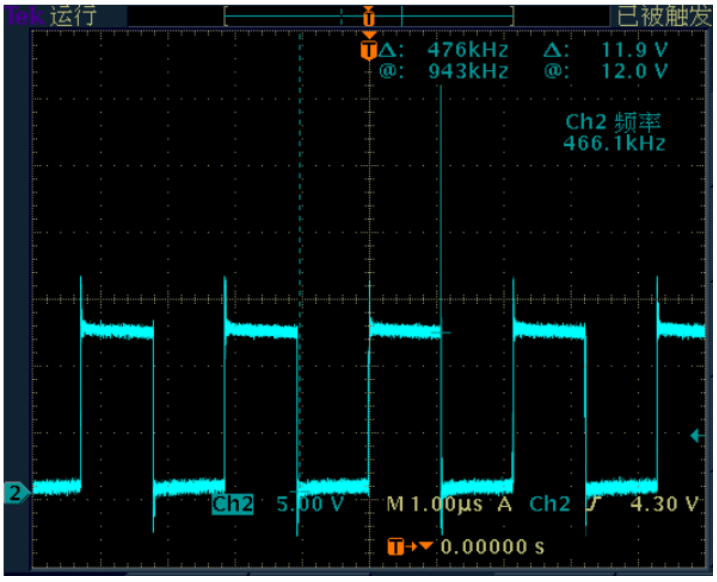
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	VDD=12V,RL=4ohm,Po=1W
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	VDD=9V,RL=4ohm,Po=1W

Frequency response：

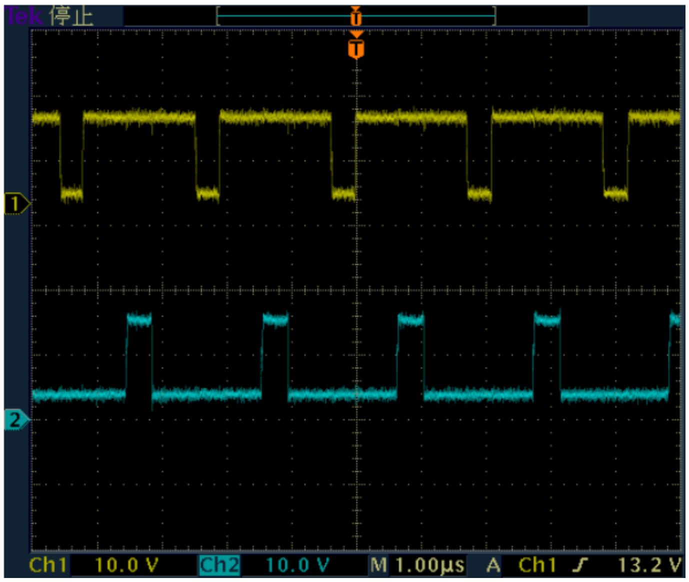


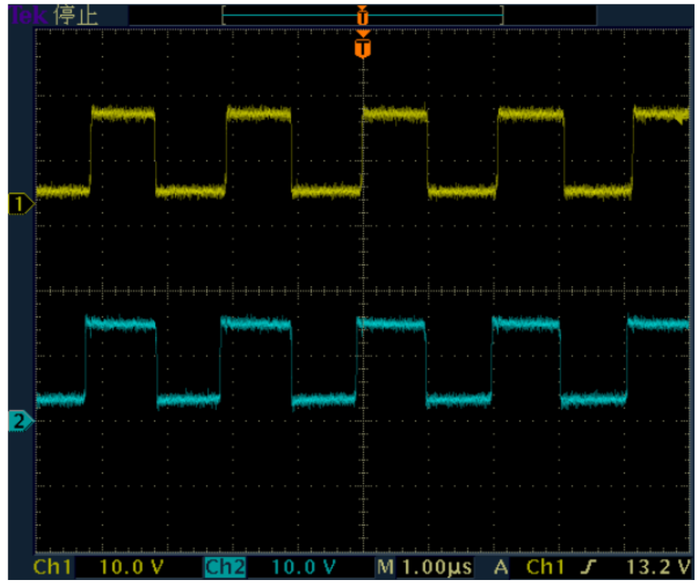
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

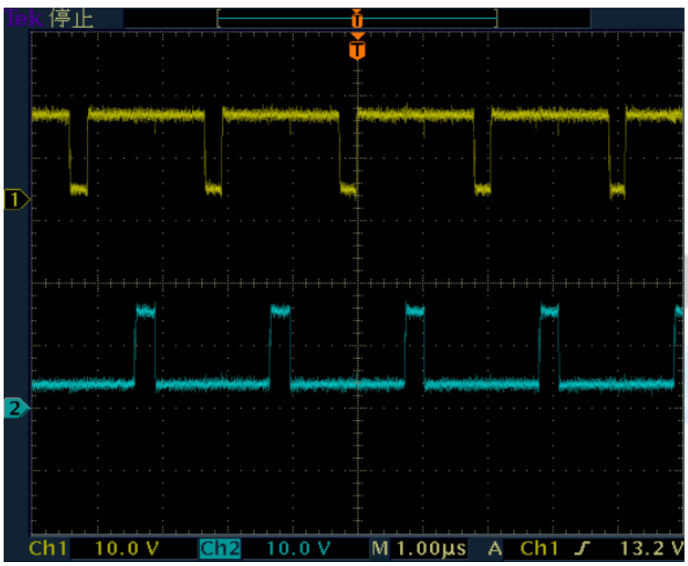
Output waveform：

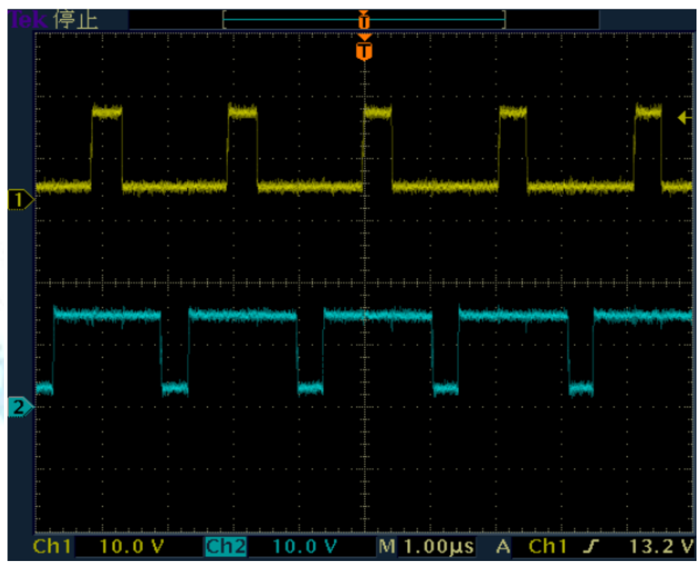


Output waveform：









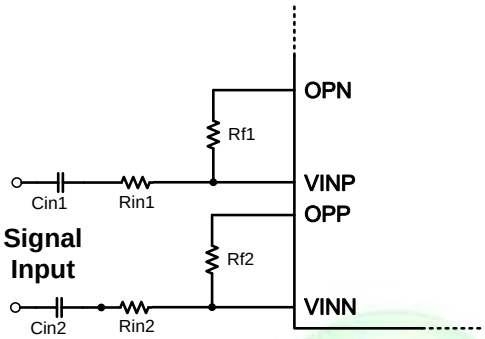
Applications Information(for Amplifier)

Gain

The gain of the LPA2100 is set by an external two resistor and multiplied by an internal 10 fold amplification.

AV= (Rf1/Rin1) *10=(Rf2/Rin2)*10

Gain=20lgAV



AGC For NCN

The LPA2100 integrates an automatic gain control technology to achieve NCN(Non-Crack Noise). The circuit could set different NCN degree by different resistance divider applying to CTRL/SLV to protect speaker as showed below.R1+R2 should less than 100K. Also, the voltage on CTRL/SLV set the Master/Slave synchronization mode. When circuit set master synchronization mode, chip will output a 500KHz frequency pulse signal through SYNC pin. If circuit used as Slave mode, chip can receive a pulse signal from 300KHz to 700KHz.

The function of NCN(Non-Crack Noise) needs two key processes: Detection of Crack and Suppression gain. When an overload signal applied to speaker, chip will suppress the gain of circuit through real-time detection output signal in a certain time. The suppression will be stronger until the output signal fall to the available range with a stable balance between the signal and suppression. In the same way, the suppression will be weaker when the input signal amplitude decreases.

Sheet.1 NCN function and Master/Slave synchronization

Voltage on CTRL/SLV	NCN	Master/Slave
CTRL/SLV < 1/6 VDD	Disabled	Master
1/6 VDD < CTRL/SLV < 2/6 VDD	2degree	Master
2/6 VDD < CTRL/SLV < 3/6 VDD	1degree	Master
3/6 VDD < CTRL/SLV < 4/6 VDD	Disabled	Slave
4/6 VDD < CTRL/SLV < 5/6 VDD	2degree	Slave
CTRL/SLV > 5/6 VDD	1degree	Slave

Note： 1degree：Detection delay time: 45ms，release of suppression: 2.6s；

2degree: Detection delay time: 10ms，release of suppression: 1.2s；

Shutdown operation

In order to reduce power consumption while not in use, the LPA2100 contains shutdown circuitry to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is applied to the EN pin. By switching the EN pin connected to GND, the LPA2100 supply current draw will be minimized in idle mode.

Power supply decoupling

The LPA2100 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR a low as possible. Power supply decoupling affects low frequency response. Optimum decoupling is achieved by using two capacitors of different types targeting to different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0μF, works best, placing it as close as possible to the device VDD terminal. For filtering lower- frequency noise signals, a large capacitor of 20μF (ceramic) and a capacitor of

220uF(electrolytic) are recommended, placing them near the audio power amplifier.

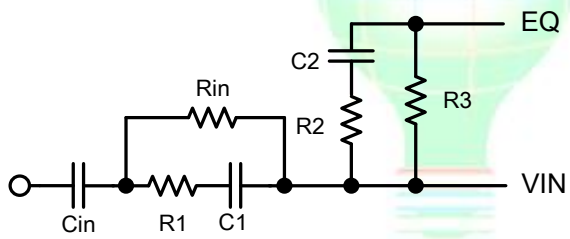
Short Circuit Protection (SCP)

The LPA2100 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output or output-to-GND short occurs. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

Signal Frequency suppress

The LPA2100 has an OPP/N pin which is the negative output of amplifier as show below. With R2 and C2, we can suppress high frequency part of signal. And the low frequency part of signal could be attenuated by R1 and C1.

$$f_H = \frac{1}{2\pi R_1 C_1} \quad ; \quad f_L = \frac{1}{2\pi R_2 C_2}$$



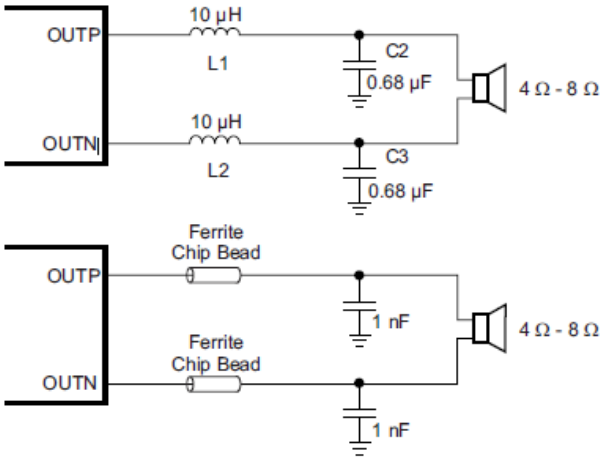
Over Temperature Protection

Thermal protection on the LPA2100 prevents the device from damage when the internal die temperature exceeds 150℃. There is a 15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30℃. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point without external system intervention.

How to reduce EMI

A simple solution is to put an additional capacitor at power supply terminal for power line. The traces from amplifier to speakers should design as short as we can. The LPA2100 has been tested with a simple ferrite bead filter for a variety of applications. The LPA2100 EVM passes FCC class-B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency. There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.



PCB Layout notices

1, In the path of the power supply, plus a 1uF and a 10uF to ground high-frequency filter capacitor. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor may achieve better sound effects.

2, Large (470 μF or greater) bulk power supply decoupling capacitors should be placed near the LPA2100 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible.

3, The power line, ground line and filter capacitor and bypass capacitors as close to the chip's pins, remember not to put the capacitor on the back of the board, through tiny holes through the jumper even over. Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.

4, Power, ground, and a large current line must try to be wide enough, if you want to add vias, the number of through-holes must be at least 6. The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability.

5, GND and VDD should be put independently, high-power signals to avoid interference.

6, If you want to pursue as large as the effect of power, a large selection of speakers or sound chamber with low resistance (such as 3.6Ω) speakers, or added to improve the supply voltage.

7, Including the line between large current cell and chip, the inductor should be as close and short as possible to chip for a high performance. Adding a coil to this pin would be helpful for EMI certification. If there is a high standards needed in LPA2100 application, we could add a coil and capacitor between chip and speaker constituting a LC filter which coil would be 100MHz, 600Ω and its DCI beyond 4A placing as close as possible to chip, the capacitor should be 1nF connecting the PGND.

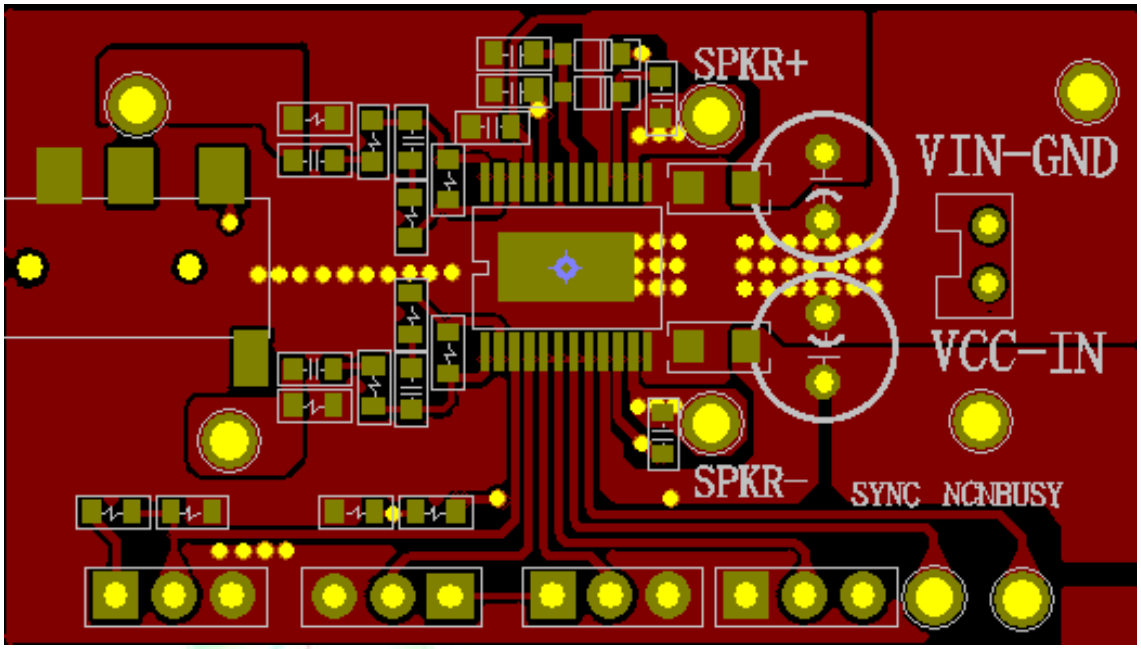
8, The position under the amplifier chip on the board must be added vents and large areas of exposed copper and tin to enhance heat dissipation.

9, In case of fixed gain and meeting demand, it should make C_{IN} small as possible as we can because it constitute a high through filter with Rin which cutoff frequency is 1/2*3.414*Cin*Rin. A high capacitance cap could make POP worse.

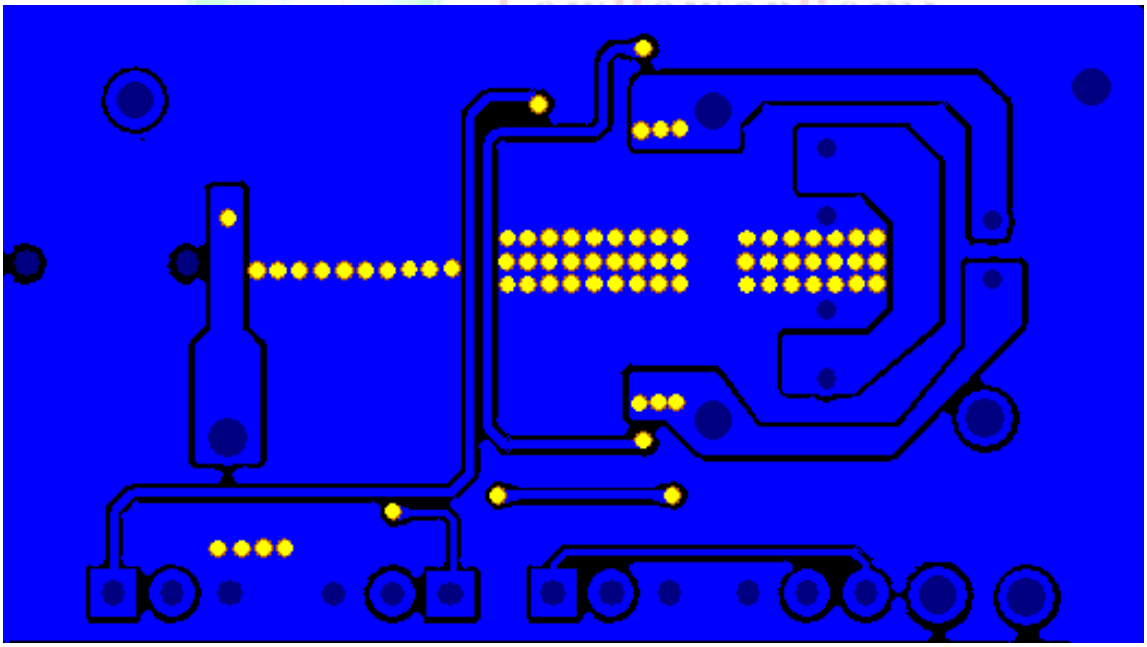
PCB LAYOUT

TSSOP24

TOP VIEW:

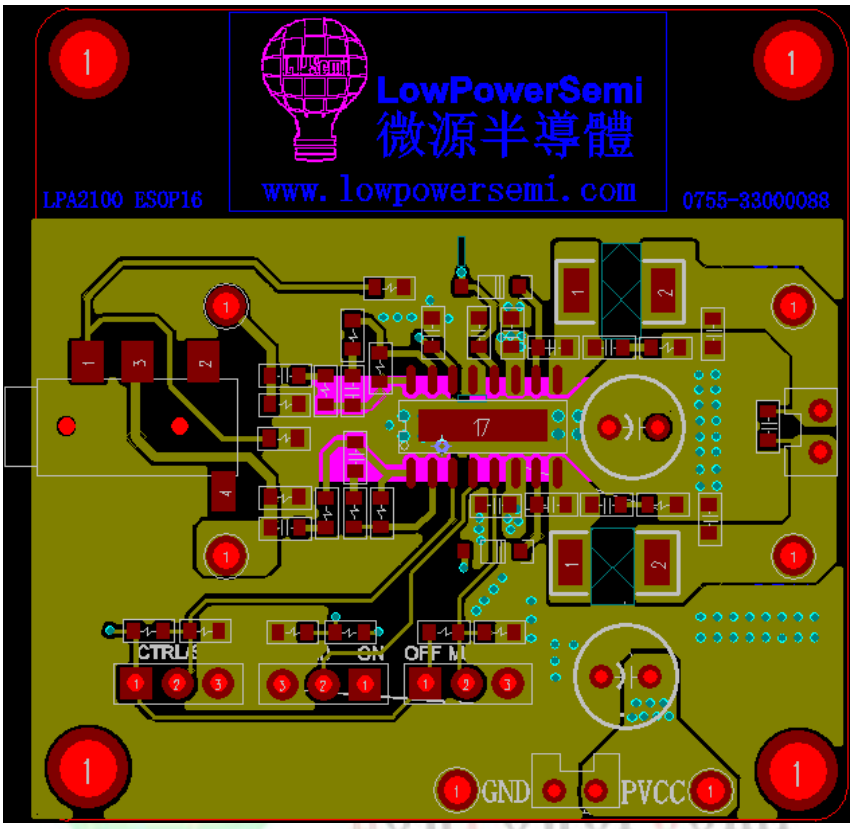


BOTTOM VIEW:

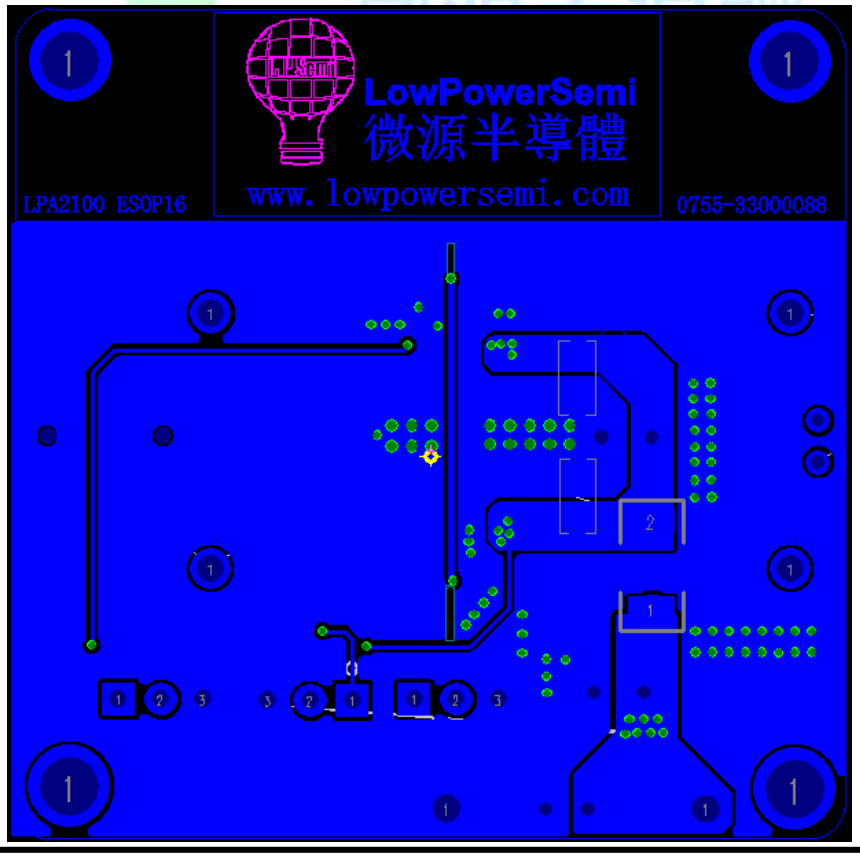


ESOP16

TOP VIEW:

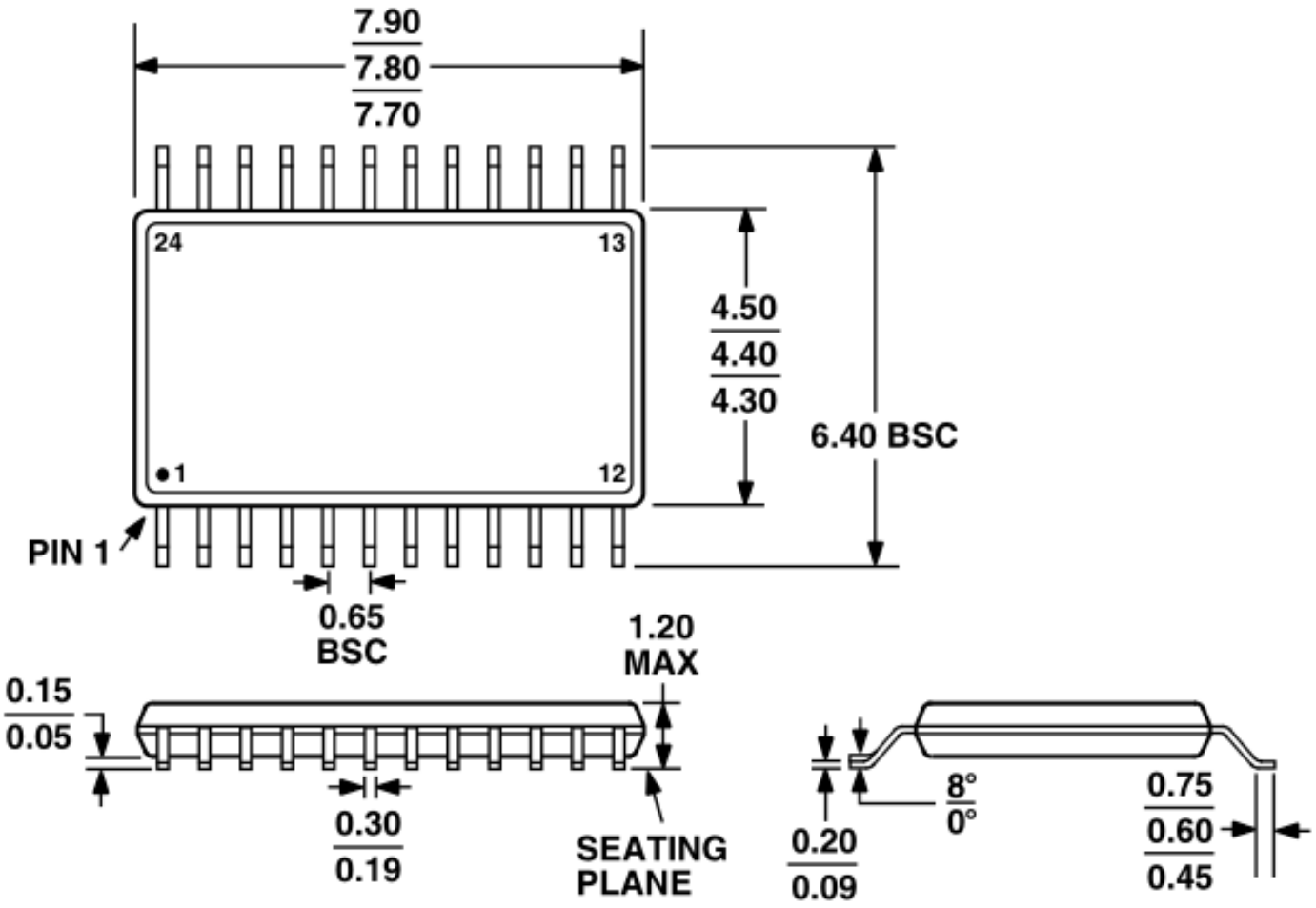


BOTTOM VIEW:

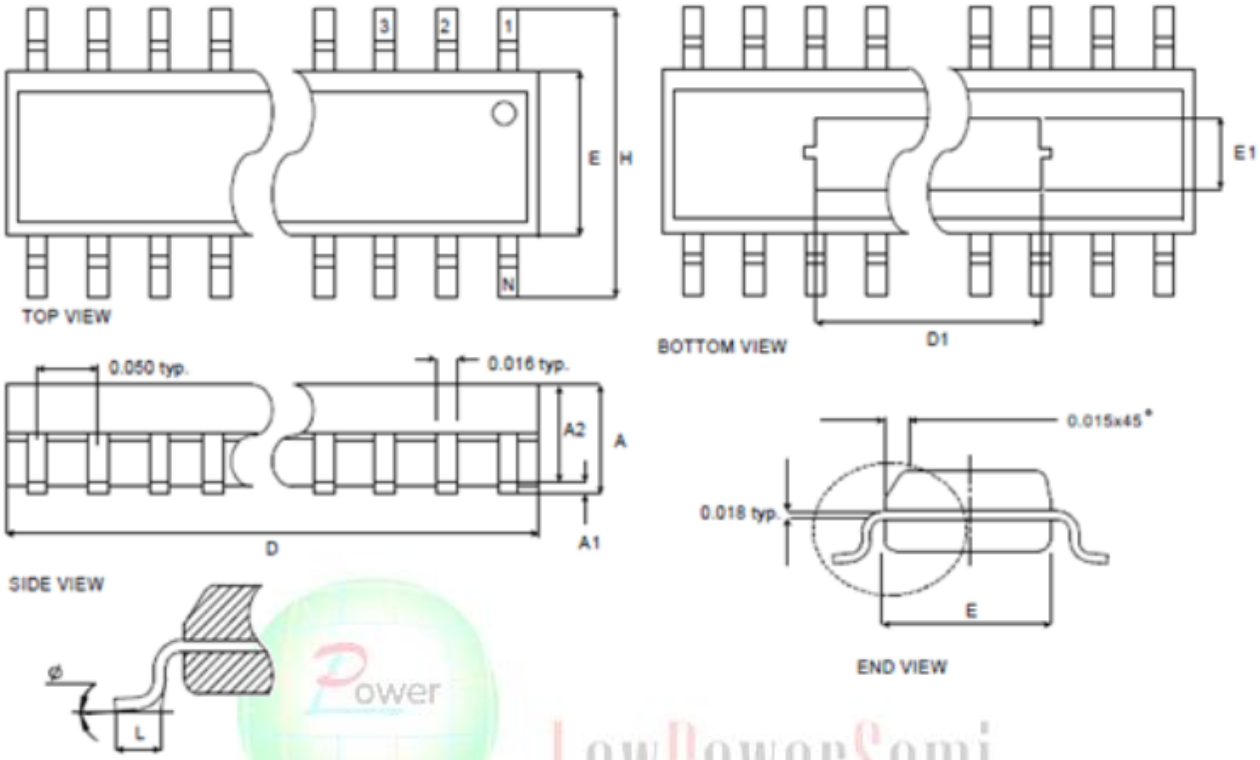


Packaging Information

TSSOP-24



ESOP-16



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.0	0.386	0.394
D1	4.115 REF		0.162 REF	
E	3.81	3.99	0.150	0.157
E1	2.184 REF		0.086 REF	
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
ϕ	0°	8°	0°	8°