LITE-ON SEMICONDUCTOR

L13ESD5V0CE2

BIDIRECTIONAL ESD PROTECTION DIODE

STAND-OFF VOLTAGE - 5.0 Volts POWER DISSIPATION - 130 Watts

GENERAL DESCRIPTION

The L13ESD5V0CE2 is designed to protect sensitive electronics from damage or latch up due to ESD, lightning, and other voltage induced transient events. The device will protect one line operating at 5.0 volts.

FEATURES

- Bi-directional ESD protection of one line.
- Max. peak pulse power: Ppp=130w at tp = 8/20 us.
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), >30KV(air) ; >30KV(contact)
- IEC 61000-4-5, level 1 (surge) ; Ipp=12A at tp = 8/20us.
- Qualified to AEC-Q101 Rev_C

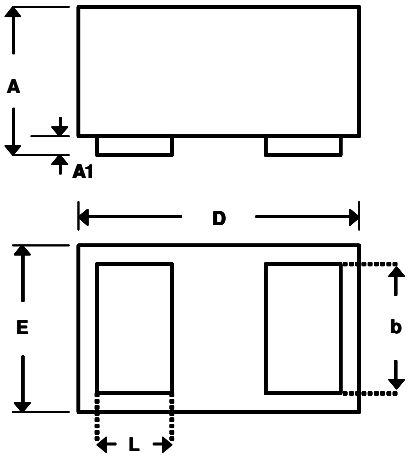
APPLICATION

- Computers and peripherals
- Communication system
- Audio & video equipment
- Portable instrumentation

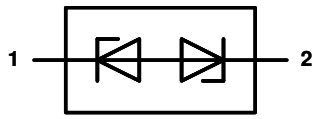
MECHANICAL DATA

- Case material: “Green” molding compound UL flammability classification 94V-0 (No Br, Sb, Cl),
- Component in accordance to RoHs 2011/65/EU
- Dimension = DFN, 1.00 mm (L)* 0.6 mm (W)

SOD-882



SOD-882		
DIM.	MIN.	MAX.
A	0.47	0.53
A1	0.00	0.05
b	0.25	0.55
D	0.95	1.075
E	0.55	0.675
L	0.20	0.45
All dimension in millimeter		



PIN ASSIGNMENT	
1	Cathode
2	Cathode

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25℃ ambient temperature unless otherwise specified.

ABSOLUTE RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power (8/20us waveform)	P_{PPM}	130	W
Peak pulse current (8/20us waveform)	I_{pp}	12	A
Operating junction temperature range	T_J	-55 to +150	℃
Storage temperature range	T_{STG}	-55 to +150	℃
Soldering temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
Reverse standoff voltage	--	V_{DRM}	--	5.0	V
Reverse leakage current	V_{DRM} = 5V	I_{RM}	--	100	nA
Breakdown voltage	I_R = 1 mA	V_{BR}	5.5	9.5	V
Junction capacitance (each I/O pin and ground)	V_R = 0V, f = 1MHz,	C_J	--	45	pF
Clamping voltage	I_{PP} = 1A (8/20 us)	V_{CL}	--	10	V
	I_{PP} = 12A (8/20 us)		--	14	

RATING AND CHARACTERISTIC CURVES
L13ESD5V0CE2

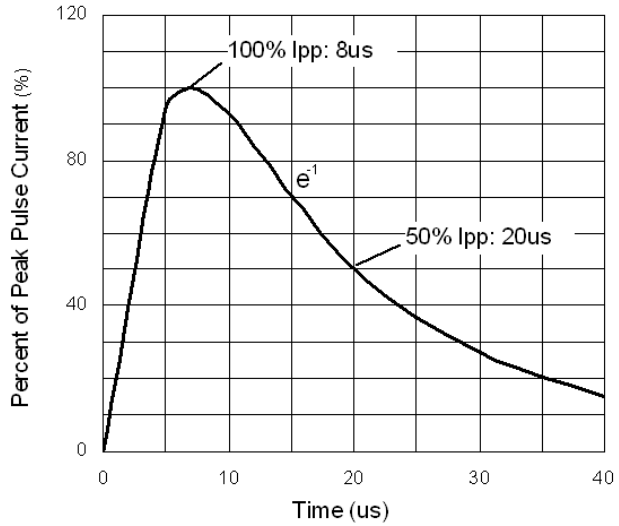


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

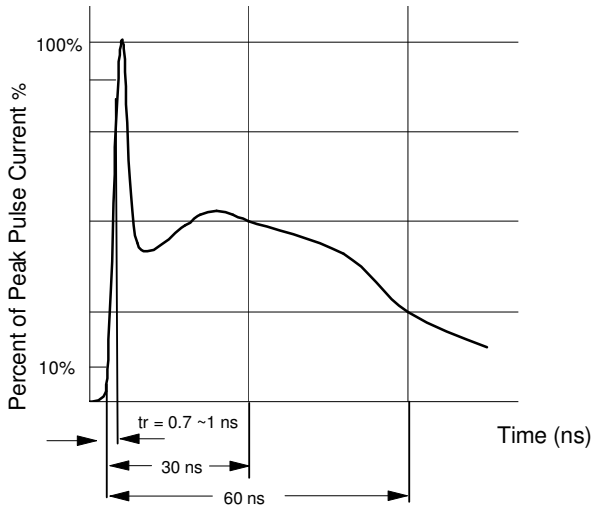


Figure 2. ESD pulse waveform according to IEC 61000-4-2

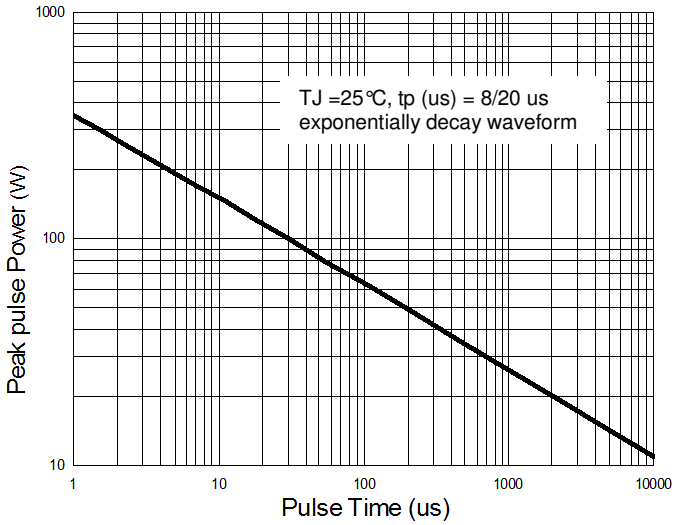


Figure 3. Power Dissipation versus Pulse Time

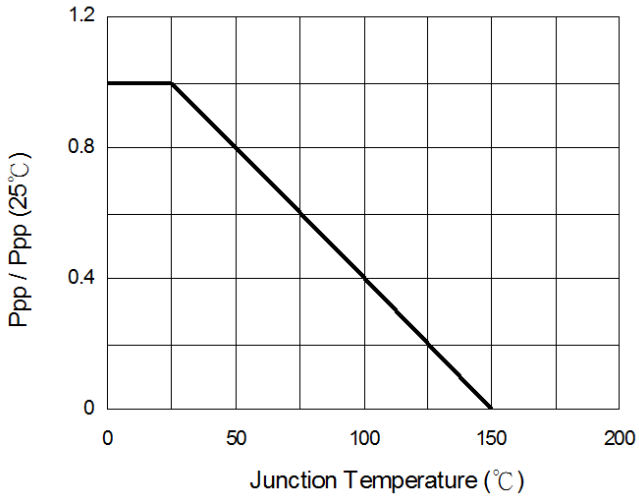


Figure 4. Peak pulse power versus TJ

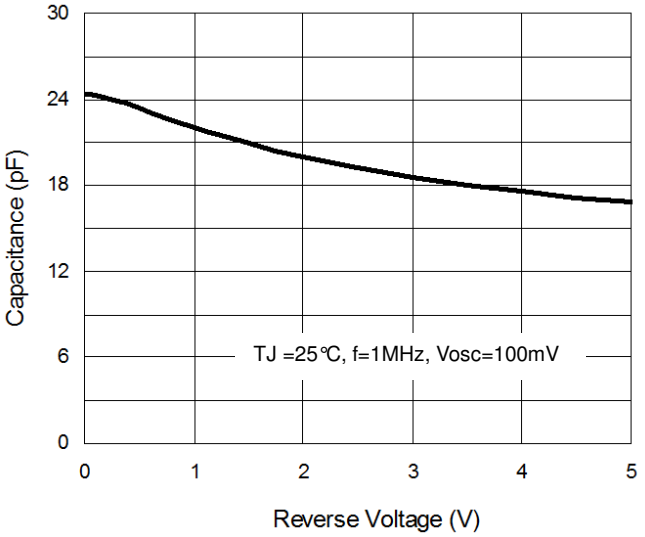


Figure 5. Typical Junction Capacitance

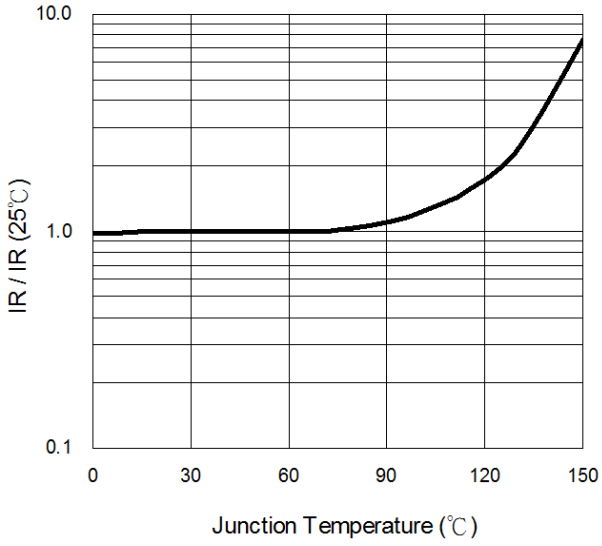


Figure 6. Reverse Leakage Current versus TJ

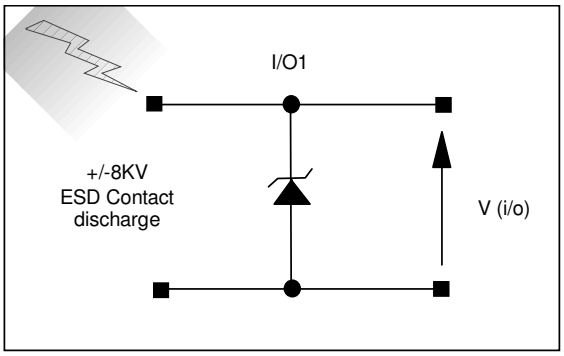


Figure 7. ESD Test Configuration

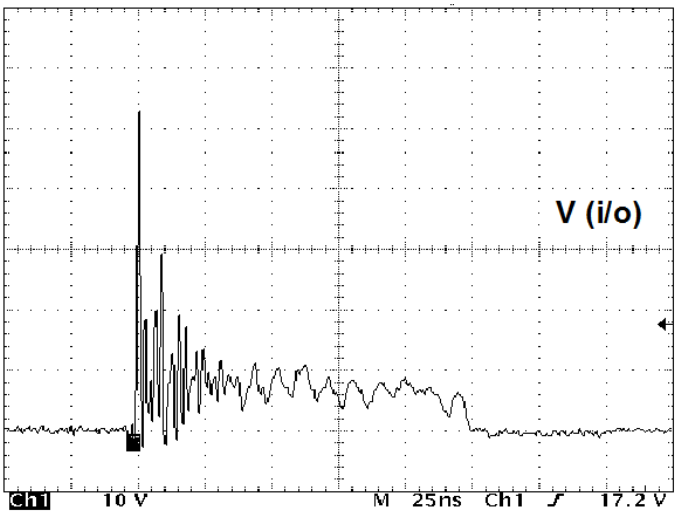


Figure 8. Clamped +8 kV ESD voltage waveform

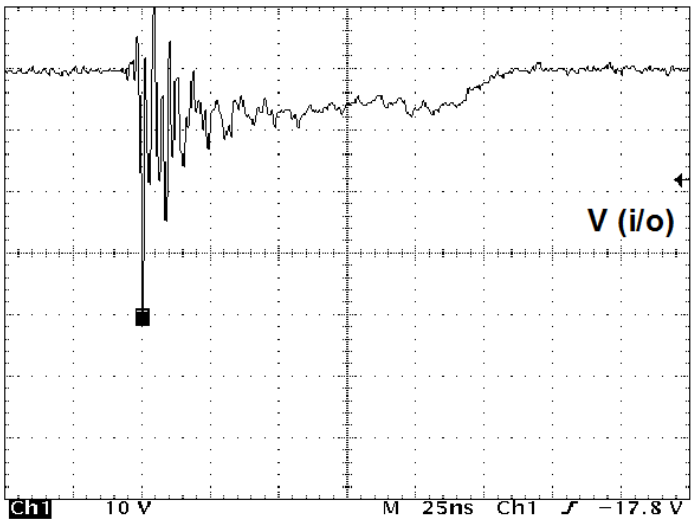
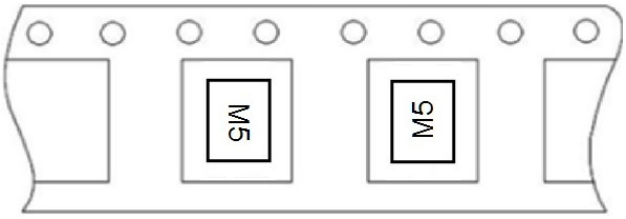


Figure 9. Clamped -8 kV ESD voltage waveform

MARKING AND PACKAGING INFORMATION
L13ESD5V0CE2

Marking and Orientation :

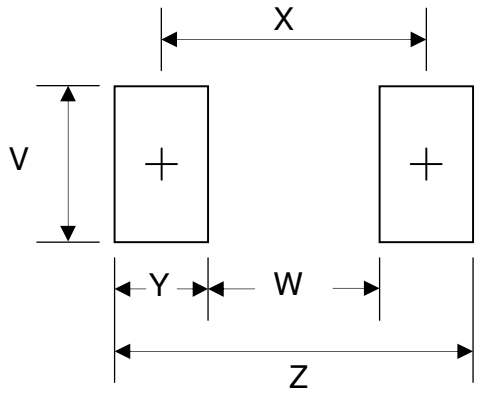


Note: Marking is none direction

Packaging Information :

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L13ESD5V0CE2	10K	7	150K	300K

SOD-882 Soldering Pad Layout :



Dim.	Millimeters	Inches
Z	1.30	0.051
X	0.75	0.029
W	0.20	0.007
Y	0.55	0.021
V	0.80	0.031

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