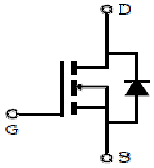
CRTD055N03L

Features

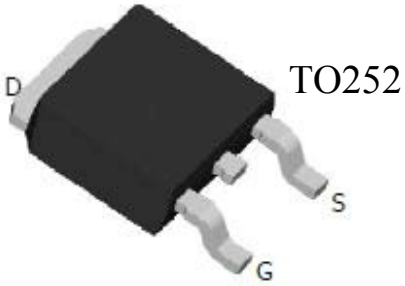
- Lead free and Green Device Available
- Low Rds-on to Minimize Conductive Loss
- High avalanche Current



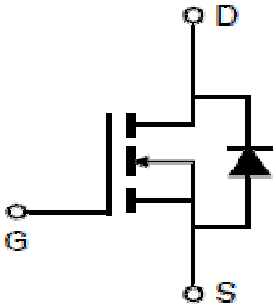
V_{DSS}	30V
$R_{DS(on)}$ Vgs=10V typ.	4.3mΩ
max.	5.5mΩ
$R_{DS(on)}$ Vgs=4.5V typ.	5.4mΩ
max.	7mΩ
I_D @ Vgs=10V (Silicon limited)	86A
I_D @ Vgs=10V (Package limited)	50A

Application

- Load Switch
- SPMS



TO252



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Param		Maximum	Unit
V_{DSS}	Drain-to-Source Voltage		30	V
V_{GSS}	Gate-to-Source Voltage		±20	V
I_D Vgs=10V	Continuous Drain Current	T_C=25°C (Silicon limited)	86	A
		T_C=100°C (Silicon limited)	61	
		T_C=25°C (Package limited)	50	
I_D Vgs=4.5V		T_C=25°C (Silicon limited)	76	
		T_C=100°C (Silicon limited)	54	
		T_C=25°C (Package limited)	50	
I_{DP}	Pulsed Drain Current	T_C=25°C	-	A
I_{AS}	Avalanche Current (L=0.1mH)		23	A
E_{AS}	Avalanche Energy (L=0.1mH)		26	mJ
P_D	Maximum Power Dissipation	T_C=25°C	71	W
		T_C=100°C	35	
T_J, T_{STG}	Junction & Storage Temperature Range		-55~175	°C

Thermal Characteristics

Symbol	Parameter	Max.	Unit
R_{thJC}	Thermal resistance, junction to case	2.1	℃/W
R_{thJA}	Thermal resistance, junction to ambient	106	℃/W

Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	30	—	—	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V,V_{GS}=0V	—	—	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	0.8	—	1.8	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	—	—	±100	nA
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=25A	—	4.3	5.5	mΩ
		V_{GS}=4.5V, I_D=20A	—	5.4	7	
G_{fs}	Forward Transconductance	VDS=5V, ID=90A	—	72	—	S
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=25A,V_{GS}=0V	—	0.8	1.3	V
I_S	Diode Continuous Forward Current		—	—	50	A
t_{rr}	Reverse Recovery Time	IS=20A, di/dt=100A/us	—	14	—	nS
Q_{rr}	Reverse Recovery Charge		—	2.8	—	nC
Dynamic Characteristics						
R_G	Gate Resistance	V_{GS}=0V, V_{DS}=0V, Frequency=1MHz	—	1.9	—	Ω
C_{iss}	Input Capacitance	VGS=0V, VDS=15V, F=1MHz	—	2999	—	pF
C_{oss}	Output Capacitance		—	335	—	
C_{rss}	Reverse Transfer Capacitance		—	290	—	
$t_{d(on)}$	Turn-On Delay Time	VDS=15V, ID=1A, Rg=3 Ω, VGS=4.5V	—	21	—	nS
t_r	Rise Time		—	32	—	
$t_{d(off)}$	Turn-Off Delay Time		—	59	—	
t_f	Fall Time		—	34	—	
Gate Charge Characteristics						
Q_g	Total Gate Charge	VDS=25V，VGS=4.5V，ID=14A	—	26	—	nC
Q_{gs}	Gate-to-Source Charge		—	3.5	—	
Q_{gd}	Gate-to-Drain Charge		—	14	—	

Typical Operating Characteristics

Figure 1. Typ. Output Characteristics

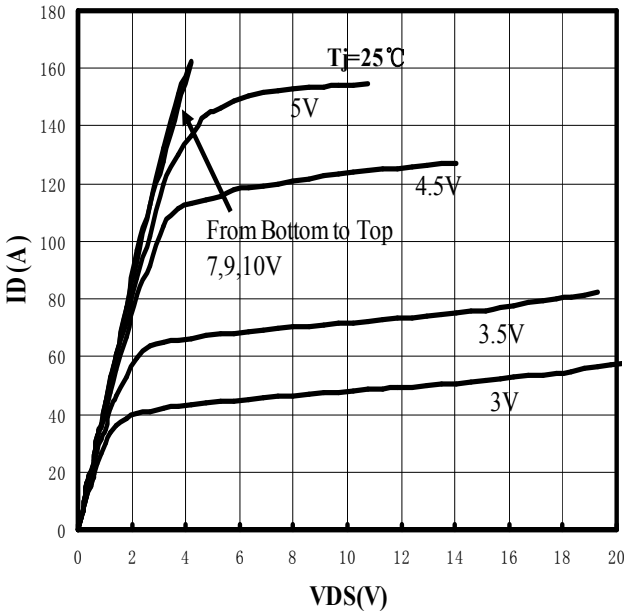


Figure 2. Typ. Output Characteristics

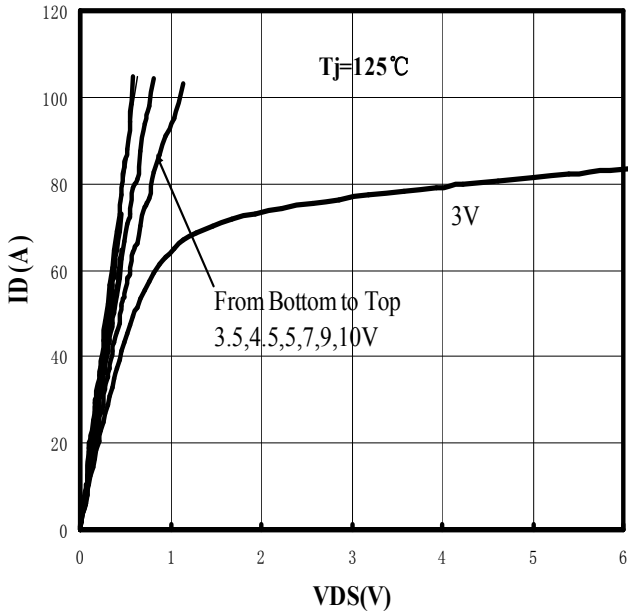


Figure 3. Transfer Characteristics

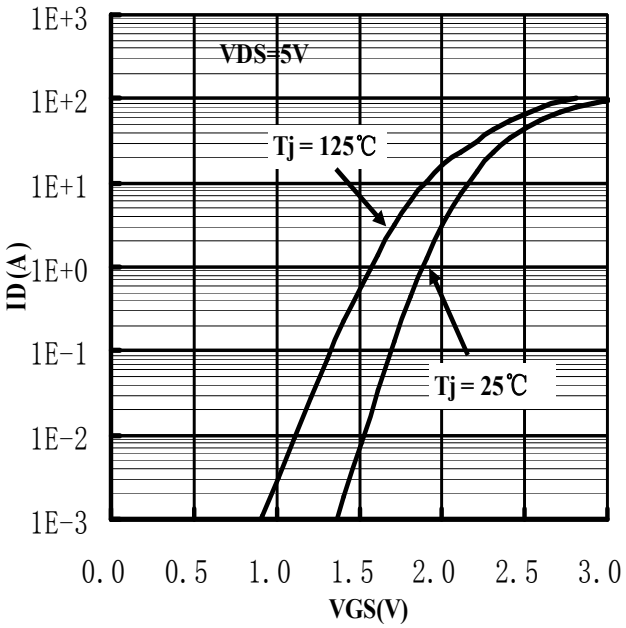
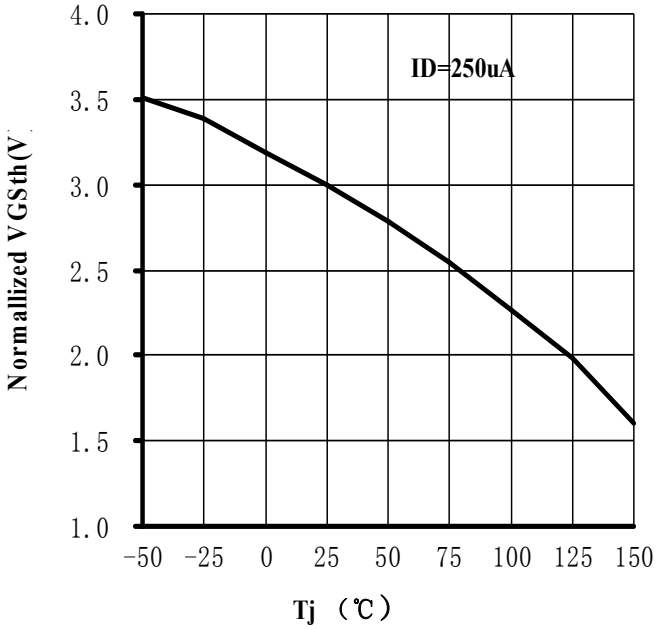


Figure 4. Gate Threshold Voltage Characteristics



Typical Operating Characteristics

Figure 5. Rdson vs. Drain Current Characteristics

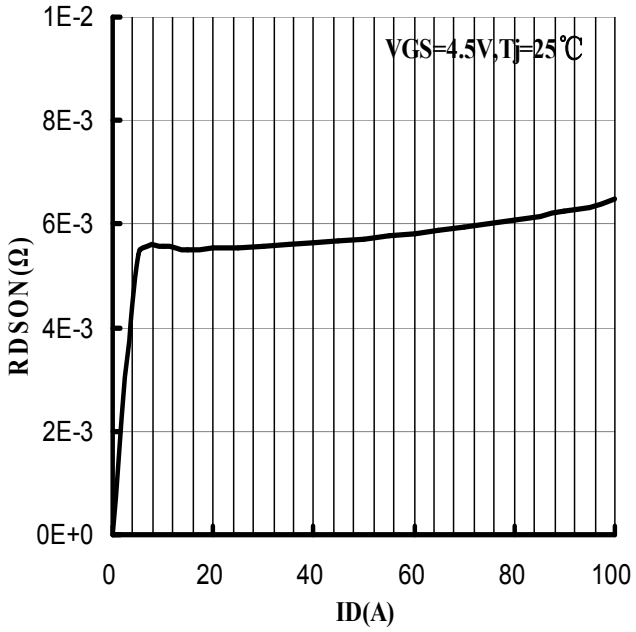


Figure 6. Rdson vs. Junction Tem Characteristics

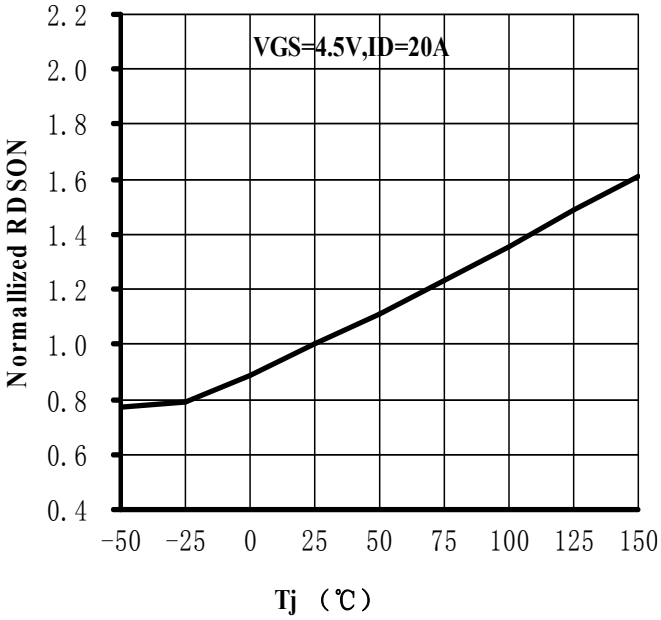


Figure 7. Rdson vs. VGS Characteristics

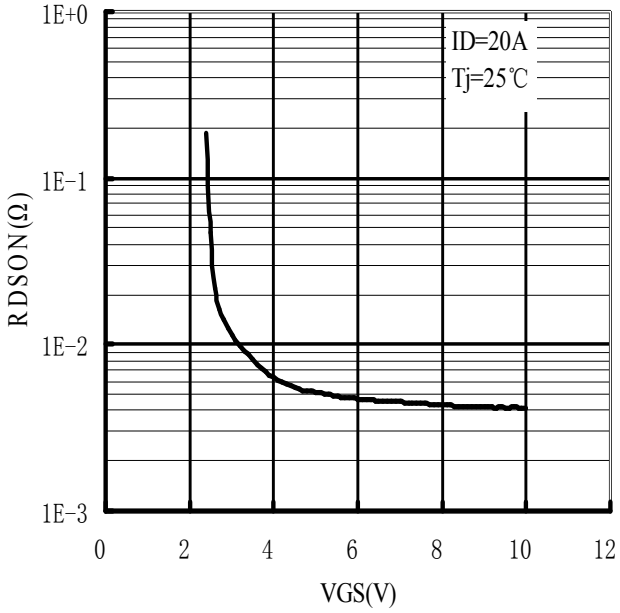
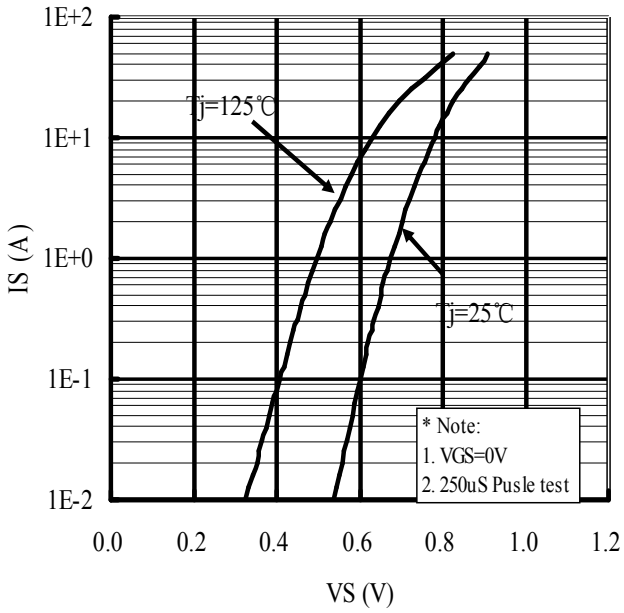


Figure 8. IS vs. VSD Characteristics



Typical Operating Characteristics

Figure 9. Gate Charge Characteristics

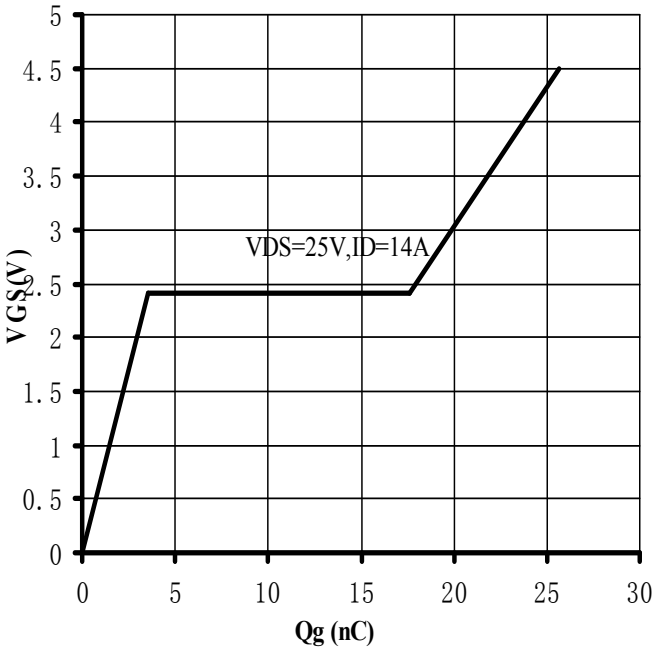


Figure 10. Capacitance Characteristics

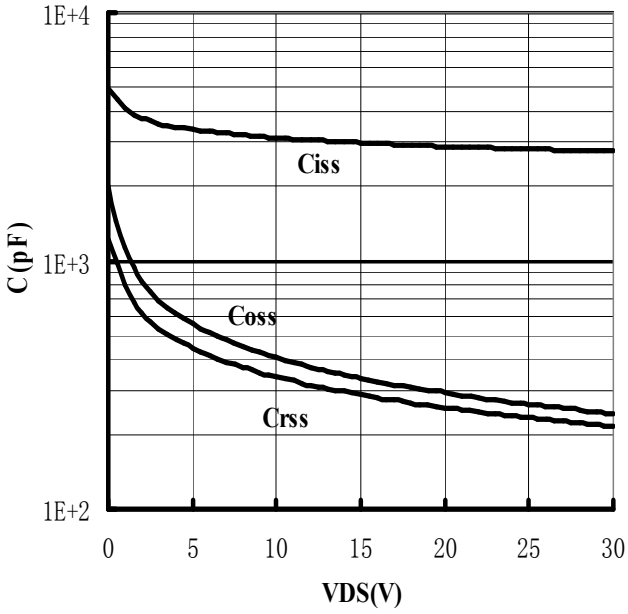
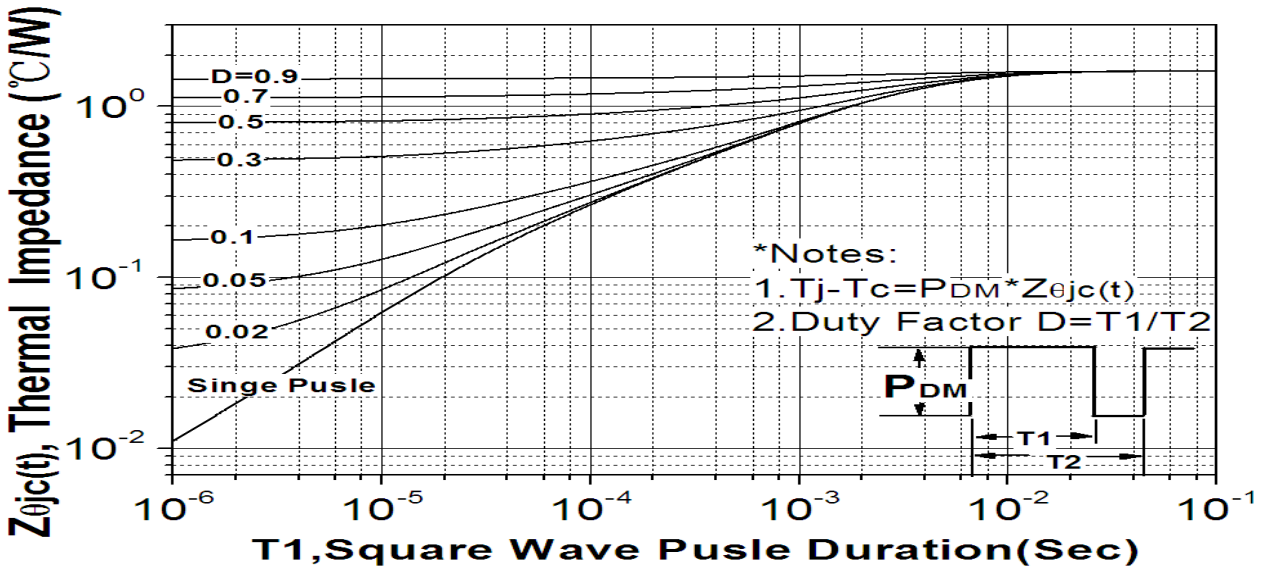
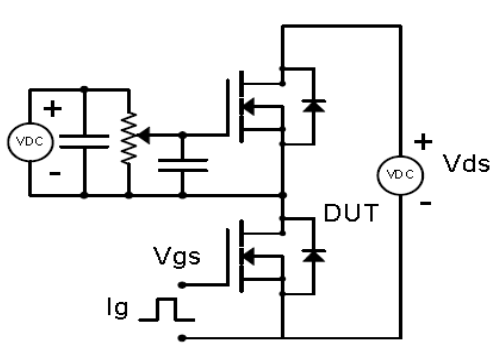


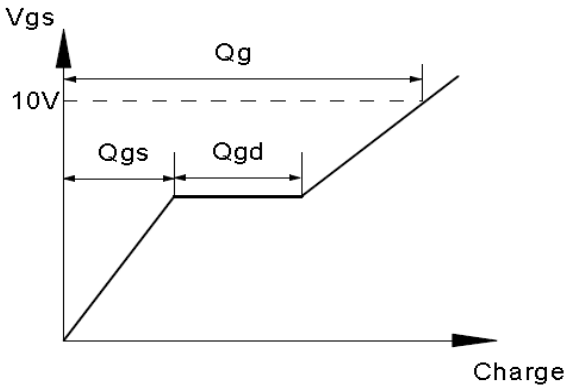
Figure 11. Thermal Resistance Characteristics



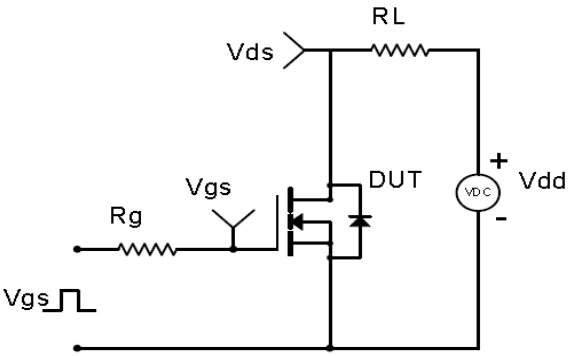
Test Circuit & Waveform

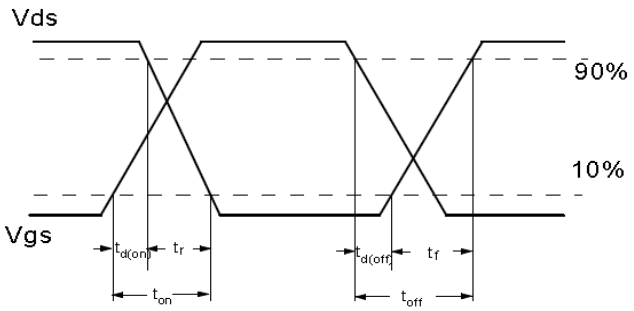
Gate Charge Test Circuit & Waveform



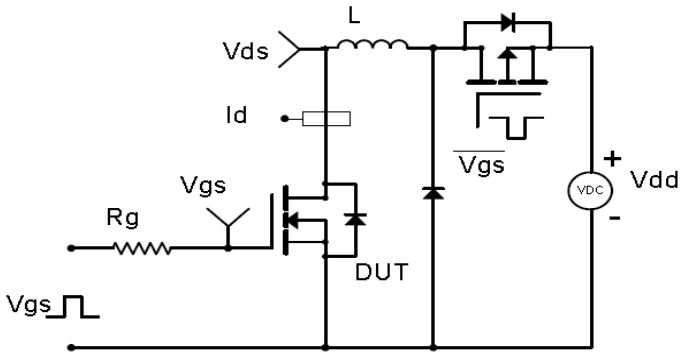


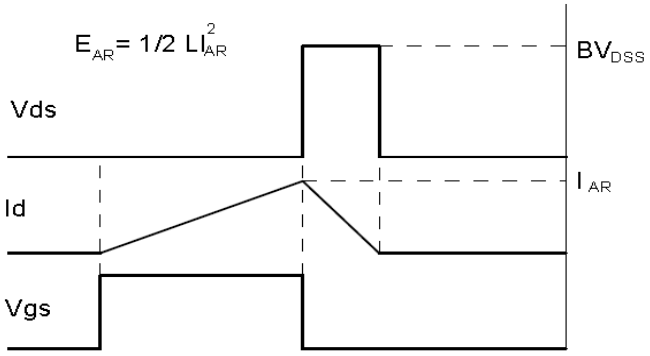
Resistive Switching Test Circuit & Waveforms



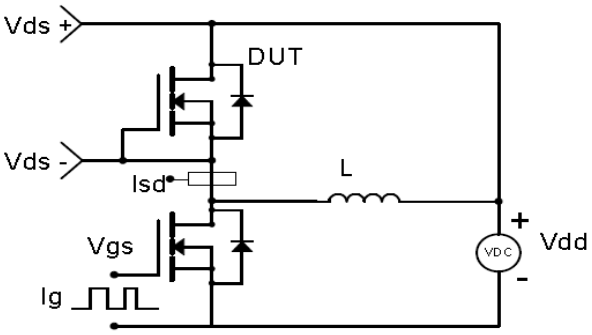


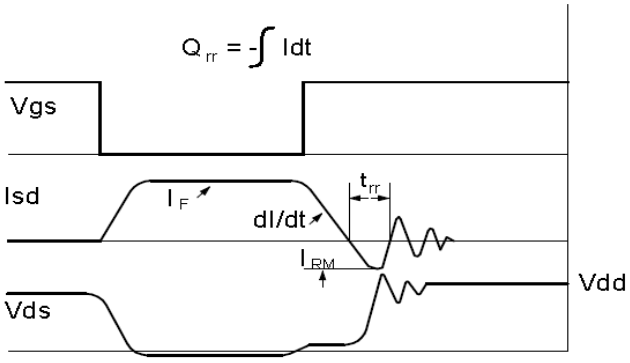
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



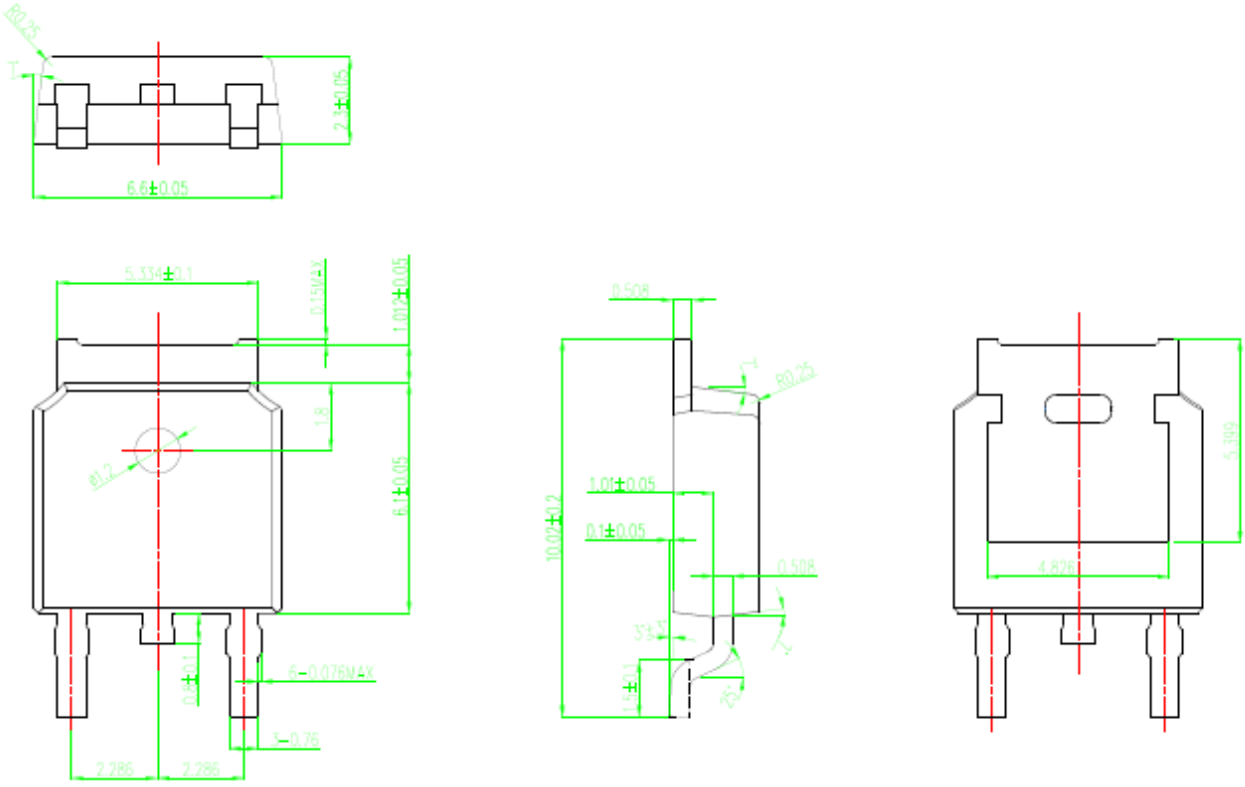


Diode Recovery Test Circuit & Waveforms





Package Information



技术要求：

1．塑封体中心与引线框架中心线偏差≤0．05，
上下塑封体中心偏差≤0．05；
2．塑封体不准有缺损、气泡、气孔、裂纹等缺陷；
3．塑封体表面除阴影部分为毛面，其余为光面；
4．未注脱模斜度≤5°；
5．未注公差为±0．05，未注圆角为R 0．15（max）