15W Stereo Class-D Audio Power Amplifier

Features

- **Supply Voltage is 8V ~ 26V**
- **Class D operation eliminates heat sink & reduce power supply requirement**
- **20,26, 32, 36, 4 steps gain setting**
- **15W/ch into an 8Ω Loads at 10% THD+N from a 16-V supply**
- **10W/ch into 8Ω Loads at 10% THD+N from a 13V supply**
- **30W into a 4Ω Mono Load at 10% THD+N from a 16V Supply**
- **Adjustable Power limit function plus DC Protection**
- **Thermal and Over-Current Protections with Auto-Recovery option**
- **TSSOP-28P with thermal pad packages**
- **QFN4x4-28 with thermal pad packages**

General Description

The APA2619 is a stereo, high efficiency, Class-D audio amplifier available in TSSOP-28Pand QFN4x4-28 pins packages.

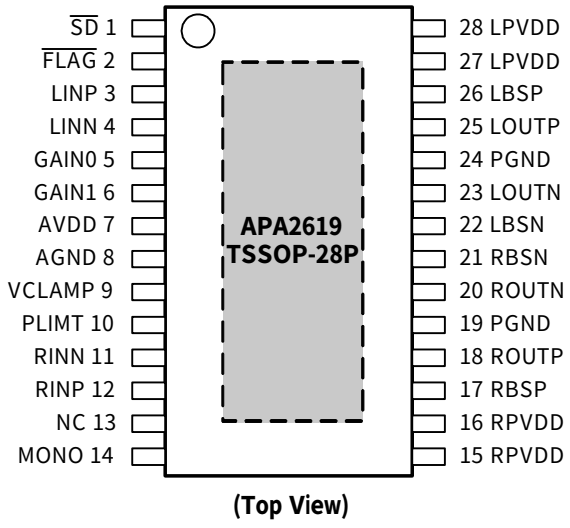
The Class-D power amplifier has higher efficiency compare to the tradition Class-AB power amplifier. The filter-free Class-D architecture eliminates the external low pass filters. The internal gain setting can minimum the external component counts, and for the flexible application the gain can be set to 4-step 20, 26, 32, 36dB by gain control ins (GAIN0 and GAIN1). The power limit function cans protection the speaker when output signal excess the speaker limit rating.

The integration of Class-D power amplifier is a best solution for power efficiency and lower the total BOM costs. The operating voltage is from 8V to 26V. The APA2619 power amplifiers are capable of driving 15 W at V_{DD}=16V into 8Ω speaker, and provides thermal and over-current protections also can detection the DC that prevent to destroy the speaker voice coil.

Applications

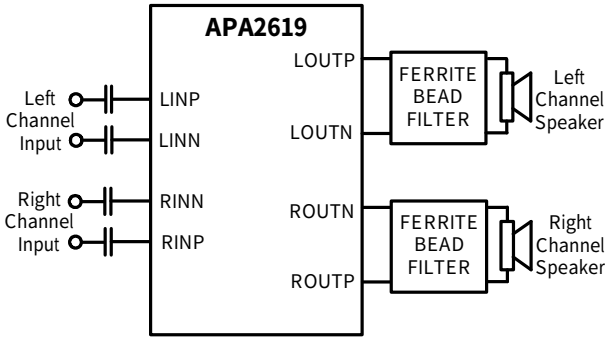
- **LCD Monitor, TV**
- **AIO**
- **Projector**

Pin Configuration

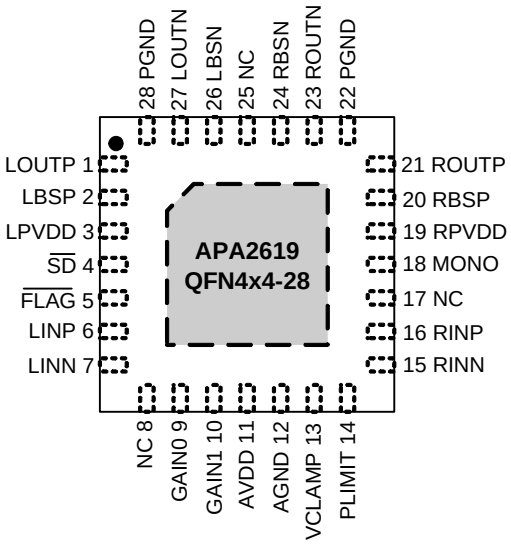


(Top View)

Simplified Application Circuit



Pin Configuration(Cont.)



(Top View)

Ordering and Marking Information

APA2619 □□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code R : TSSOP-28P QA : QFN4x4-28 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2619 R : APA2619 XXXXX	XXXXX - Date Code
APA2619 QA : APA2619 XXXXX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (PVDD, AVDD)	-0.3 to 30	V
V_I	Input Voltage ($\overline{SD}$, GAIN0 and GAIN1, MONO and $\overline{FLAG}$)	-0.3 to V_{DD}+0.3	
	PLIMIT	-0.3 to 6.3	
	LINP, LINN, RINP, RINN	-0.3 to 6.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	
T_{SDR}	Soldering Temperature Range, 10 Seconds	260	
R_L	STEREO Mode : V_{DD}＞15V	4.8	Ω
	STEREO Mode: V_{DD} ≦15V	3.2	
	MONO mode	3.2	
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) TSSOP-28P QFN4x4-28	 29 40	°C/W
θ_{JC}	Thermal Resistance -Junction to Case (Note 3) TSSOP-28P QFN4x4-28	 3 4	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TSSOP-28P is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TSSOP-28P package.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		8.0	26.0	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$	2.2	-	
		GAIN0, GAIN1, MONO	2.0	-	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$	-	0.8	
		GAIN0, GAIN1, MONO	-	0.8	
T_A	Ambient Temperature Range		-40	85	°C
T_J	Junction Temperature Range		-40	125	°C
R_L	Speaker Resistance		3.5	-	Ω

Electrical Characteristics

V_{DD}=12V, GND=0V, A_V=36dB, T_A= 25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions	APA2619			Unit
			Min.	Typ.	Max.	
V_{CLAMP}	Regulated Voltage	I_O=2mA, V_{DD}=8~26V T_J = -40°C ~ 125°C	4.5	5	5.5	V
V_O	Maximum Output Voltage Under PLIMIT Control	V_{PLIMIT} = 1V, V_I = 1Vrms	-	5.5	-	
$T_{SD(ON)}$	Shutdown Turn-On Time	$\overline{SD}$=2.2V	-	20	-	ms
$T_{SD(OFF)}$	Shutdown Turn-Off Time	$\overline{SD}$=0.8V	-	2	-	µs
I_{DD}	Quiescent Supply Current	No Load	-	20	35	mA
I_{SD}	Quiescent Supply Current in shutdown mode	$\overline{SD}$= 0V	-	10	100	µA
I_I	Input Current	$\overline{SD}$, GAIN0, GAIN1, MONO	-	5	50	
F_{OSC}	Internal Oscillator Frequency		350	400	450	kHz
R_{DSON}	Static Drain-Source On-State Resistance	V_{DD} = 12V, I_L= 0.5A	-	240	-	mΩ
A_V	Gain	Gain 0 = 0, Gain 1 = 0	-	20	-	dB
		Gain 0 = 1, Gain 1 = 0	-	26	-	
		Gain 0 = 0, Gain 1 = 1	-	32	-	
		Gain 0 = 1, Gain 1 = 1	-	36	-	
t_{DCDET}	DC Derect Time	VINP=5V, VINN=0V	-	500	-	ms

Stereo Mode

V_{DD}=12V, GND=0V, A_V=36dB, T_A= 25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions		APA2619			Unit
				Min.	Typ.	Max.	
V_{DD} = 24V, T_A= 25°C							
Po	Output Power	V_{DD}=16V THD+N=1%, F_{IN}=1kHz	R_L=8Ω	-	12	-	W
THD+N	Total Harmonic Distortion Pulse Noise	V_{DD}=16V F_{IN}=1kHz, Po=7.5W	R_L=8Ω	-	0.1	-	%
Crosstalk	Channel Separation	V_O=1Vrms, F_{IN} =1kHz, Gain=20dB		-	-85	-	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, input AC-Ground, f_{in}=1kHz		-	-65	-	
SNR	Signal-To-Noise Ratio	Maximum output at THD+N<1%, F_{IN}=1kHz, Gain = 20dB, A-weighted		-	95	-	
$Att_{shutdown}$	Shutdown Attenuation	F_{IN}=1kHz, R_L = 8Ω, V_{in} = $1V_{PP}$		-	-100	-	
I V_{OS} I	Offset Voltage	A_V=20dB		-	-	15	mV
V_n	Noise Output Voltage	With A-weighted Filter (A_V = 20dB)		-	160	-	µV (rms)
V_{DD} = 12V T_A= 25°C							
P_O	Output Power	V_{DD}=13V THD+N = 1% F_{IN}=1kHz	R_L=8Ω	-	8	-	W
		V_{DD}=13V THD+N = 10% F_{IN}=1kHz	R_L=8Ω	-	10	-	
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=13V F_{IN}=1kHz	R_L = 8Ω P_O = 5W	-	0.1	-	%

Stereo Mode (Con.t)

V_{DD}=12V, GND=0V, A_V=36dB, T_A= 25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions	APA2619			Unit
			Min.	Typ.	Max.	
V_{DD} = 12V T_A = 25℃						
Crosstalk	Channel Separation	V_O=1Vrms, F_{IN} =1kHz, Gain=20dB	-	-90	-	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, input AC-Ground, f_{in}=1kHz	-	-65	-	
SNR	Signal-To-Noise Ratio	Maximum output at THD+N<1%, F_{IN}=1kHz, Gain = 20dB, A-weighted	-	95	-	
$Att_{shutdown}$	Shutdown Attenuation	F_{IN}=1kHz, R_L = 8Ω, V_{in} = $1V_{PP}$	-	-100	-	
I V_{OS} I	Offset Voltage	A_V=20dB	-	-	15	mV
V_n	Noise Output Voltage	With A-weighted Filter (A_V = 20dB)	-	160	-	μV (rms)

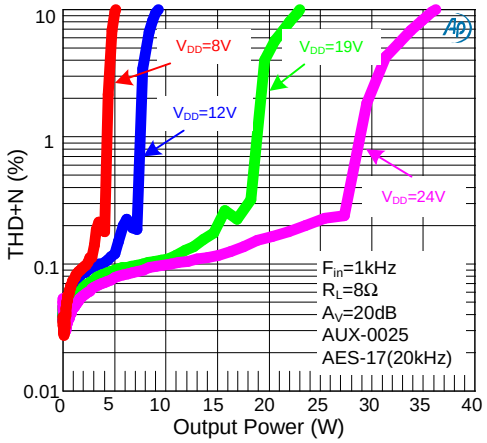
Mono Mode

V_{DD}=12V, GND=0V, A_V=36dB, T_A= 25°C (unless otherwise noted).

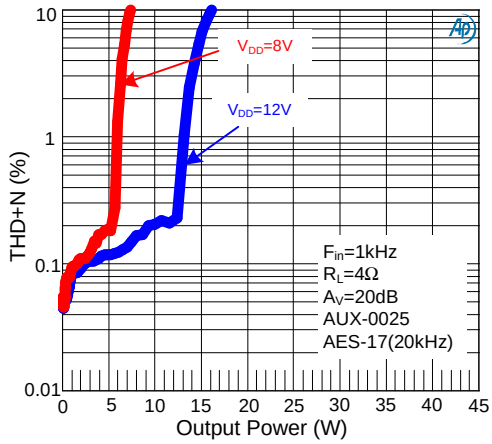
Symbol	Parameter	Test Conditions		APA2619			Unit
				Min.	Typ.	Max.	
V_{DD} = 12V T_A = 25℃							
P_O	Output Power	V_{DD}=16V THD+N = 1% F_{IN}=1kHz	R_L = 4Ω	-	24	-	W
		V_{DD}=16V THD+N = 10% F_{IN}=1kHz	R_L = 4Ω	-	30	-	
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=16V F_{IN}=1kHz	R_L = 4Ω P_O = 6W	-	0.1	-	%
PSRR	Power Supply Rejection Ratio	R_L=4Ω, input AC-Ground, f_{in}=1kHz		-	-65	-	dB
SNR	Signal-To-Noise Ratio	Maximum output at THD+N<1%, F_{IN}=1kHz, Gain = 20dB, A-weighted		-	95	-	
$Att_{shutdown}$	Shutdown Attenuation	F_{IN}=1kHz, R_L = 8Ω, V_{in} = 1Vrms		-	-100	-	
V_{OS}	Offset Voltage	A_V = 20dB		-	-	15	mV
V_n	Noise Output Voltage	With A-weighted Filter (A_V = 20dB)		-	160	-	μV (rms)

Typical Operating Characteristics

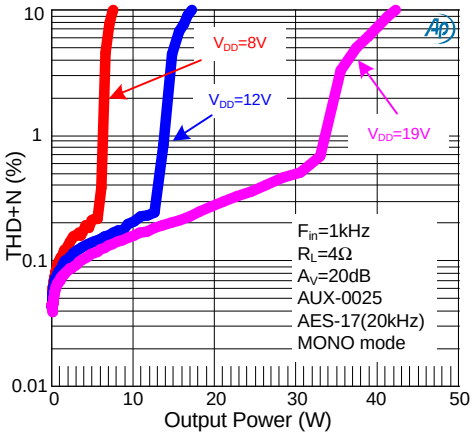
THD+N vs. Output Power



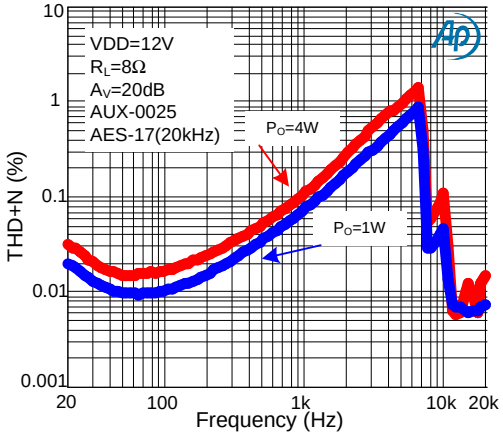
THD+N vs. Output Power



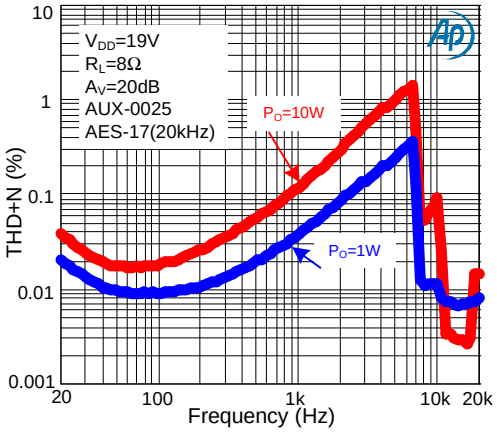
THD+N vs. Output Power



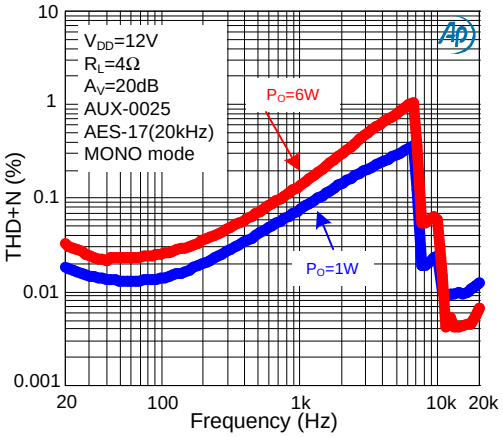
THD+N vs. Frequency



THD+N vs. Frequency

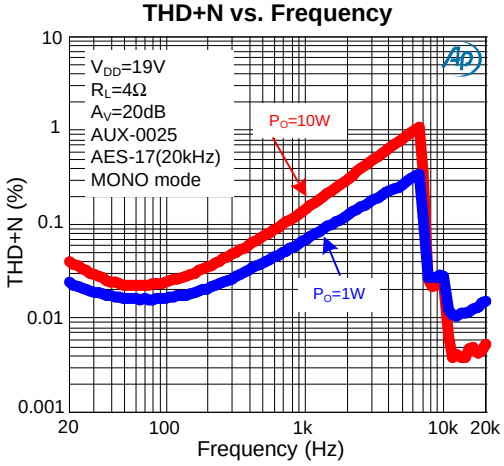


THD+N vs. Frequency

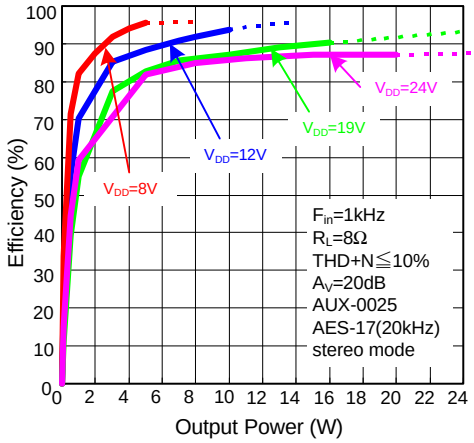


Typical Operating Characteristics

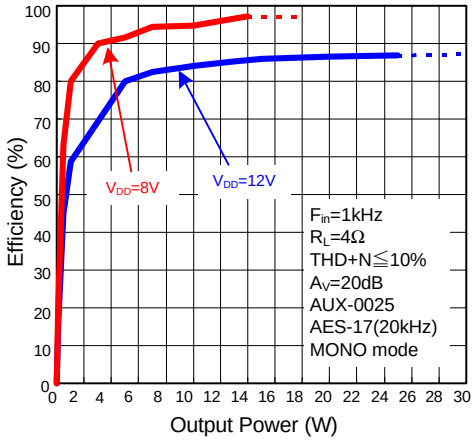
THD+N vs. Frequency



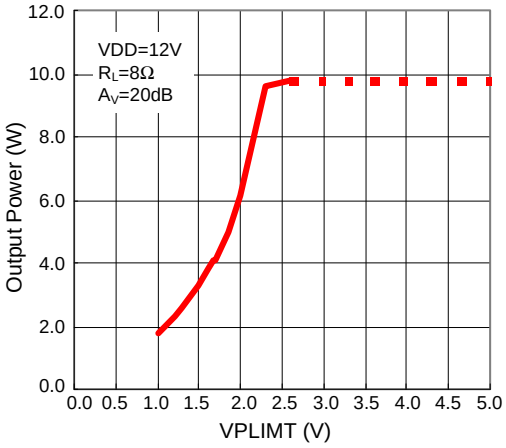
Efficiency vs. Ouput Power



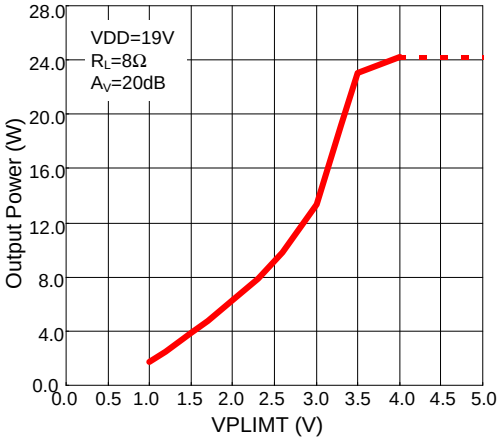
Efficiency vs. Ouput Power



Output Power vs. PLIMIT Voltage



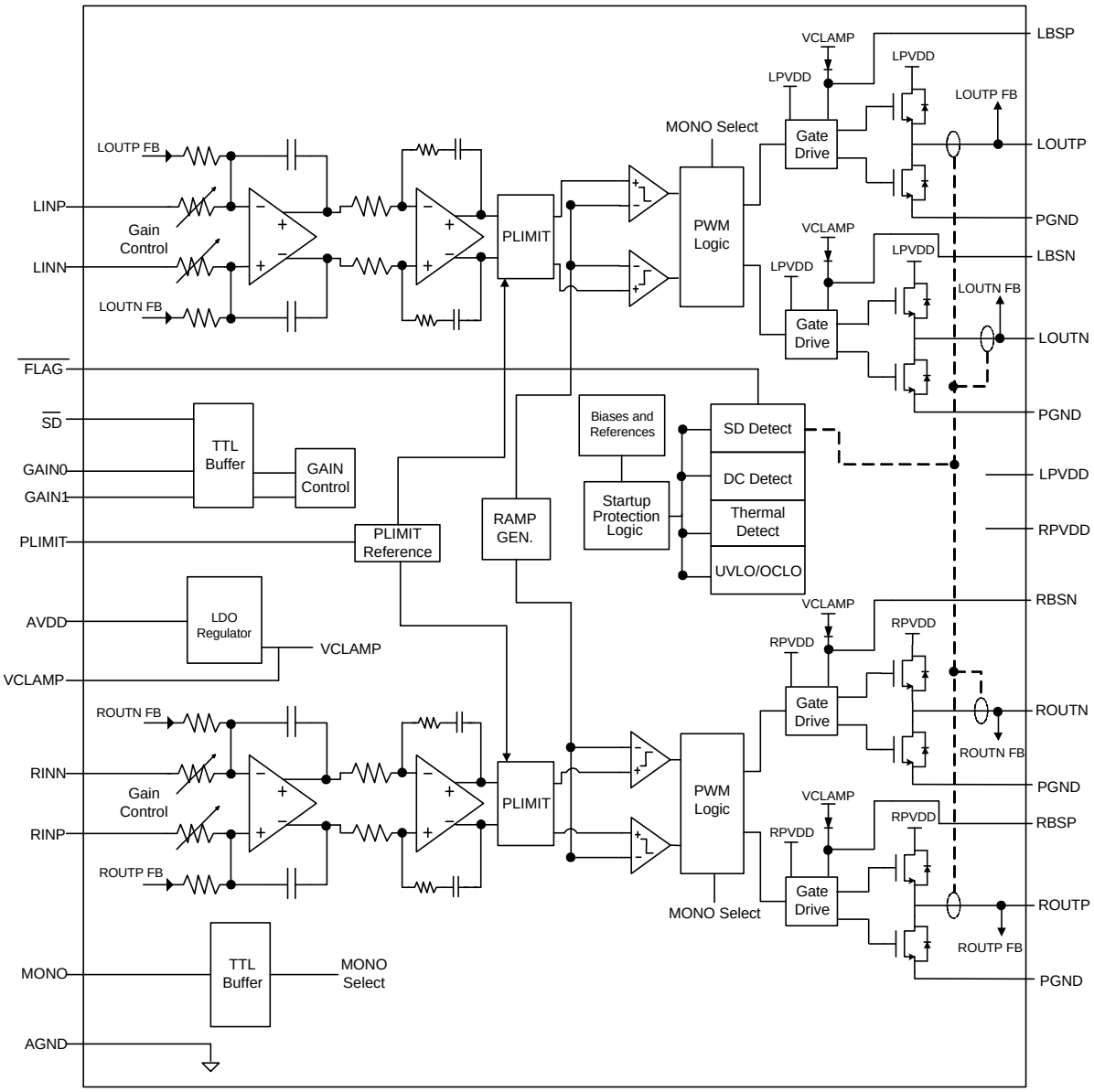
Output Power vs. PLIMIT Voltage



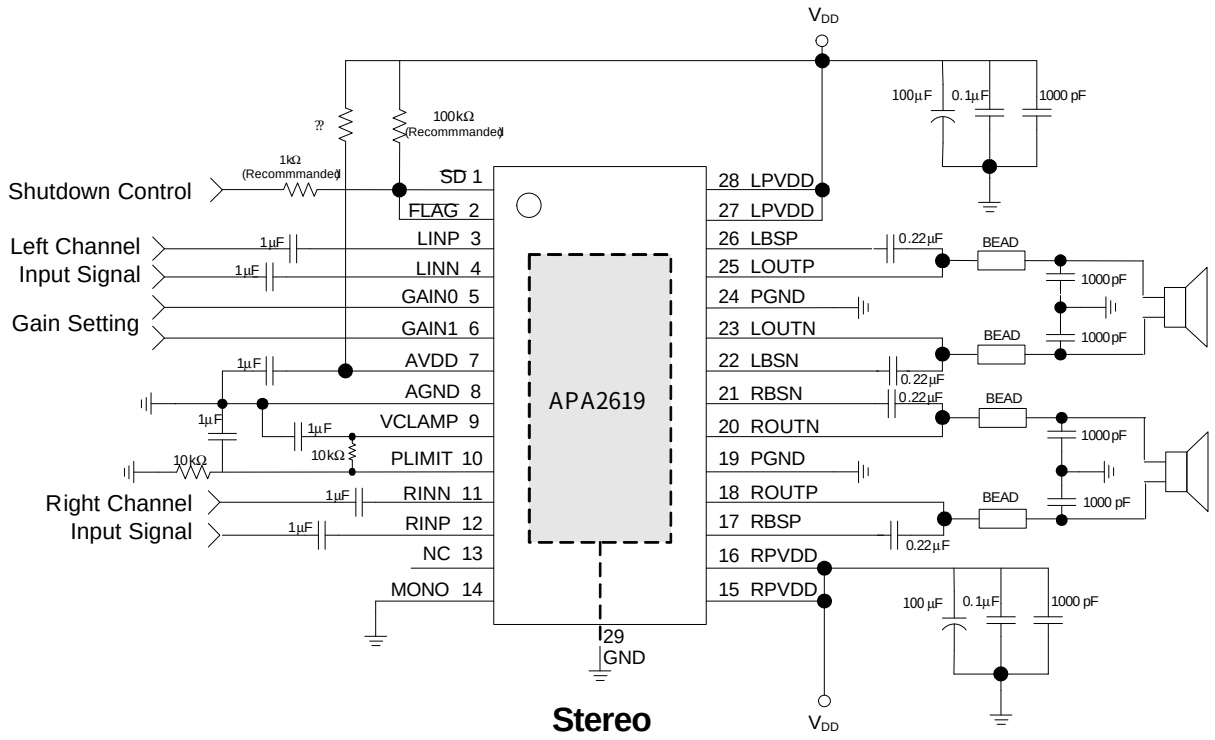
Pin Description

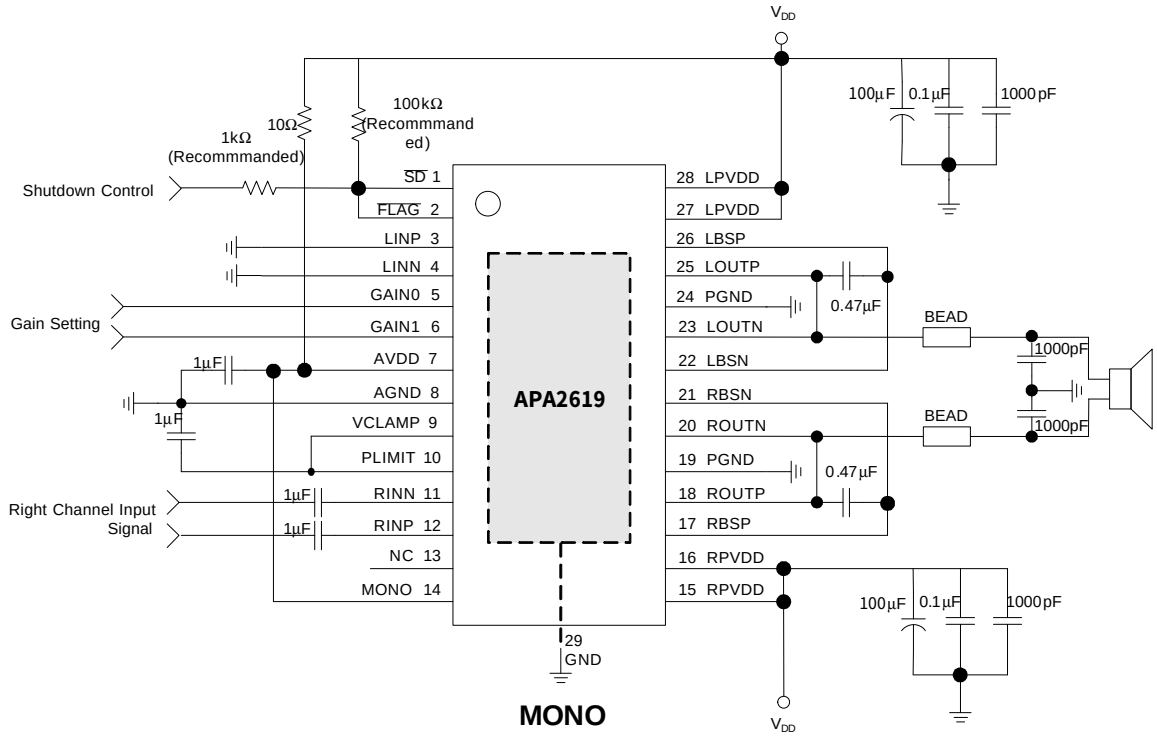
PIN			I/O/P	FUNCTION
NO.		NAME		
TSSOP -28P	QFN4x4 -28			
1	4	$\overline{SD}$	I	Shutdown logic input for audio amp (Low=outputs disabled, High=output enabled). TTL logic levels with compliance to AVDD.
2	5	$\overline{FLAG}$	O	Protection flag output (open drain). Connecting $\overline{FLAG}$ and $\overline{SD}$ can be set to auto-recovery. Otherwise need to reset by cyding AVDD
3	6	LINP	I	Positive audio input for left channel. Biased at $V_{CLAMP}/2$.
4	7	LINN	I	Negative audio input for left channel. Biased at $V_{CLAMP}/2$.
5	9	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVDD.
6	10	GAIN1	I	Gain select least significant bit. TTL logic levels with compliance to AVDD.
7	11	AVDD	P	Analog supply.
8	12	AGND	P	Analog signal ground. Connect to the thermal pad.
9	13	VCLAMP	O	Regulated voltage, Nominal voltage is 5V.
10	14	PLIMIT	I	Power limit level adjust. Connect a resistor divider from VCLAMP to GND to set power limit. Connect directly to VCLAMP for no power limit.
11	15	RINN	I	Negative audio input for right channel. Biased at $V_{CLAMP}/2$.
12	16	RINP	I	Positive audio input for right channel. Biased at $V_{CLAMP}/2$.
13	8, 17, 25	NC		Not connected.
14	18	MONO	I	Parallel BTL mode switch.
15,16	19	RPVDD	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
17	20	RBSP	I	Bootstrap I/O for right channel, positive high-side FET.
18	21	ROUTP	O	Class-D H-bridge positive output for right channel.
19, 24	22, 28	PGND	P	Power ground for the H-bridges.
20	23	ROUTN	O	Class-D H-bridge negative output for right channel.
21	24	RBSN	I	Bootstrap I/O for right channel, negative high-side FET.
22	26	LBSN	I	Bootstrap I/O for left channel, negative high-side FET.
23	27	LOUTN	O	Class-D H-bridge negative output for left channel.
25	1	LOUTP	O	Class-D H-bridge positive output for left channel.
26	2	LBSP	I	Bootstrap I/O for left channel, positive high-side FET.
27,28	3	LPVDD	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.

Block Diagram



Typical Application Circuit





Function Description

Class-D Operation

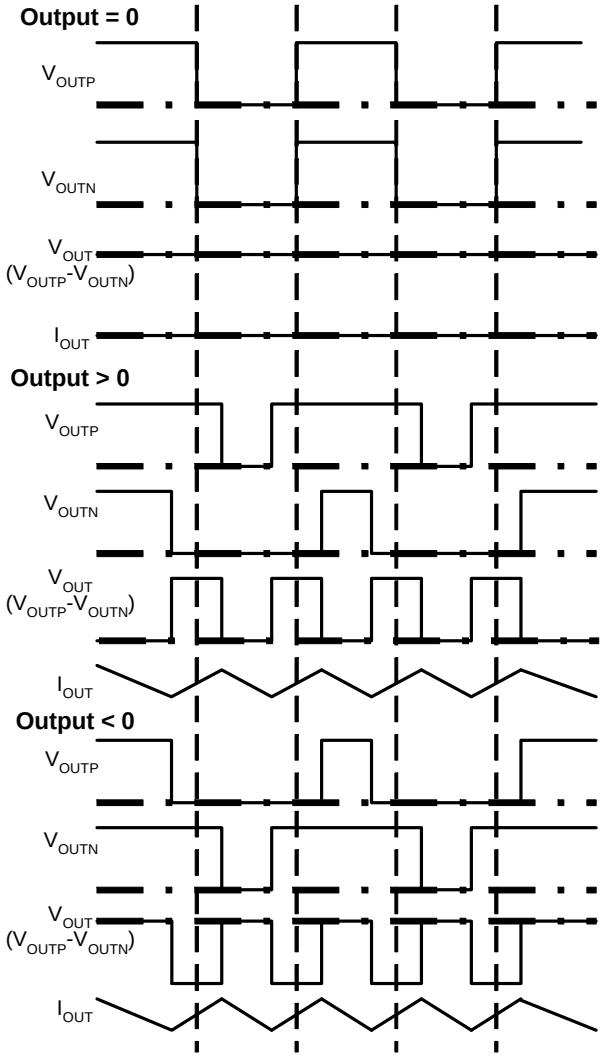


Figure1. The APA2619 Output Waveform

The APA2619 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The V_{OUTP} and V_{OUTN} are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50% for positive output voltages. The duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

Gain Setting Operation

GAIN1	GAIN0	Gain	Ri(W)
0	0	20dB	60k
0	1	26dB	30k
1	0	32dB	15k
1	1	36dB	9k

Table 1 : The Gain Setting

The APA2619's gain can be set by GAIN0, GAIN1. The detail gain setting value is list at table 1.

Shutdown Operation

In order to reduce power consumption while not in use, the APA2619 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA2619. The trigger point between a logic high and logic low level is typically 2.2V. It is best to switch between ground and the supply voltage VDD to provide maximum device performance. By switching the $\overline{SD}$ pin to low level, the amplifier enters a low-consumption- current state, I_{DD} for APA2619 is in shutdown mode. On normal operating, APA2619's $\overline{SD}$ pin should pull to high level to keeping the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Power Limit Operation

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from Vclamp to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1µF capacitor from pin 10 to ground.

Function Description (Cont.)

Power Limit Operation (Cont.)

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVDD. This "virtual" rail is 5.6 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

V_P = 5.6 × PLIMIT voltage if PLIMIT < 2.5 V

Test Condition	PLIMIT Voltage	MAX Output @	
		THD+N=1%	THD+N=10%
PVDD=12V, Rl=8Ω	1.13V	1.58W	2W
	1.4V	2.29W	3W
	1.68V	3.235W	4W
	1.86V	4.03W	5W
PVDD=12V, Rl=4Ω	0.91V	2W	2.6W
	1.16V	3W	3.96W
	1.38V	4W	5.1W
	1.57V	5W	6.3W
	1.85V	7W	8.5W

Table2. PLIMIT Typical Operation

VCLAMP Supply

The VCLAMP is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1μF capacitor to ground at this pin.

Stereo/mono switching Operation

APA2619 offers the feature of Stereo operation with two outputs of each channel connected directly. If the MONO pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this mono mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency.

MONO mode can increase more output power compare to the stereo mode single channel's output power.

DC Detect

When a DC signal applies to the input of APA2619 and the time excesses 500ms, the APA2619's DC detect fault will be reported on the $\overline{\text{FLAG}}$ pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVDD supply. Cycling SD will NOT clear a $\overline{\text{DC}}$ detect fault.

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Over-Current Protection

APA2619 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FLAG}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

Connect $\overline{\text{FLAG}}$ to $\overline{\text{SD}}$ pin, the over current protection will be auto recovery.

Thermal Protection

Thermal protection on the APA2619 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction. Thermal protection faults are NOT reported on the $\overline{\text{FLAG}}$ terminal.

Application Information

Input Resistance, R_i

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

Input Capacitor, C_i

In the typical application, an input capacitor C_i is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (R_i) form a high-pass filter with the corner frequency determined in Equation 1.

$$f_{C(hipass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_i is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 1 is reconfigured as Equation 2.

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

In this example, C_i is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use R_i from Table 1 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network C_i and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at V_{CLAMP}/2, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

Output Low-Pass Filter

If the traces form APA2619 to speaker are short, it doesn't require output filter for FCC & CE standard.

A ferrite bead may need if it's failing the test for FCC or CE tested without the LC filter. The figure 2 is the sample for added ferrite bead; the ferrite show choosing high impedance in high frequency.

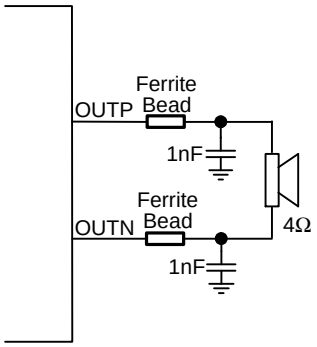


Figure 3. Ferrite Bead Output Filter

Figure 4 and Figure 5 are examples for added the LC filter (Butterworth), it's recommended for the situation that the trace form amplifier to speaker is too long, and needs to eliminate the radiated emission or EMI.

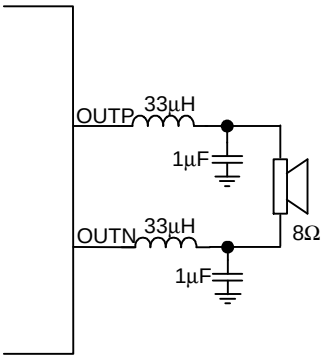


Figure 4. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8Ω

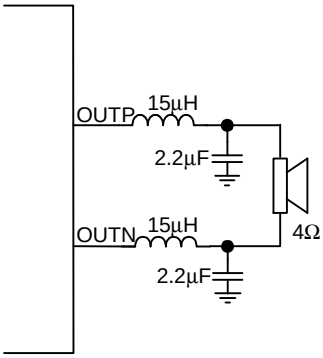


Figure 5. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4Ω

Application Information (Cont.)

Power-Supply Decoupling Capacitor, C_S

The APA2619 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF placed as close as possible to the device AVDD pin .

BSN and BSP Capactiors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22μF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22μF capacitor must be connected from OUTP to BSP, and one 0.22μF capacitor must be connected from OUTN to BSN.

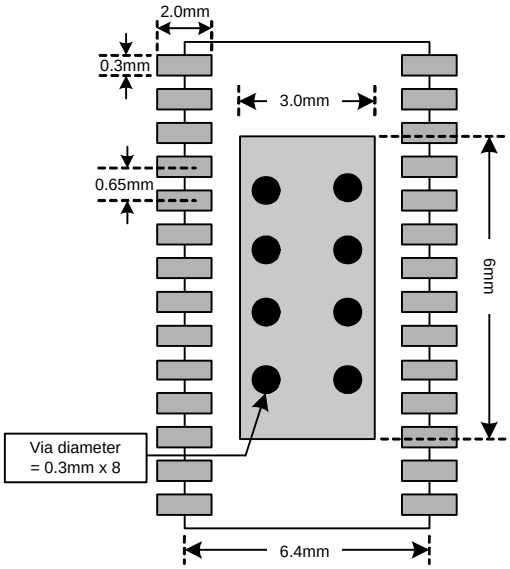
The bootstrap capacitors connected between the BSP or BSN pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Layout Recommendation

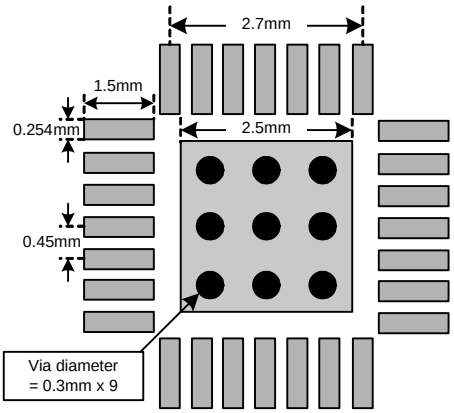
The APA2619 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

1. The high frequency decoupling capacitors should be placed as close to the PVDD and AVDD terminals as possible. Large (100μF or greater) bulk power supply decoupling capacitors should be placed near the APA2619 on the LPVDD and RPVDD supplies. Local, high-frequency bypass capacitors should be placed as close to the PVDD pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 1000 pF and 10nF and a larger mid-frequency cap of value between 0.1μF and 1μF also of good quality to the PVDD connections at each end of the chip.
2. Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
3. Grounding—The AVDD (pin 7) decoupling capacitor should be grounded to analog ground (AGND). The PVDD decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the APA2619.
4. Output filter—The ferrite EMI filter (Figure 3) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 4 and Figure 5) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
5. Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias.

Layout Recommendation(Cont.)



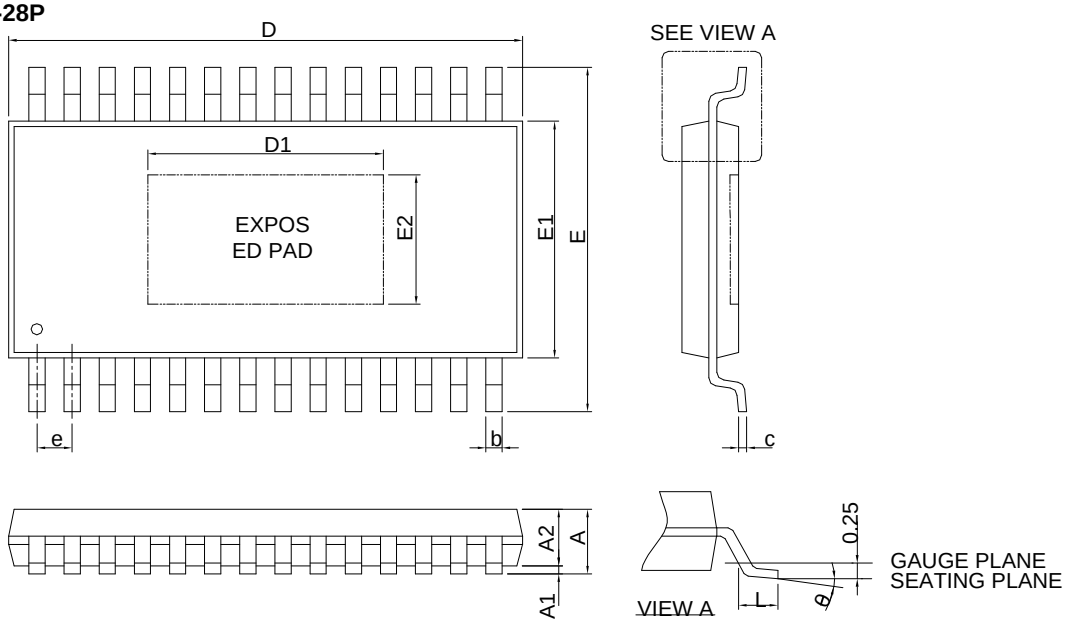
TSSOP-28P Land Pattern Recommendation



QFN4x4-28 Land Pattern Recommendation

Package Information

TSSOP-28P

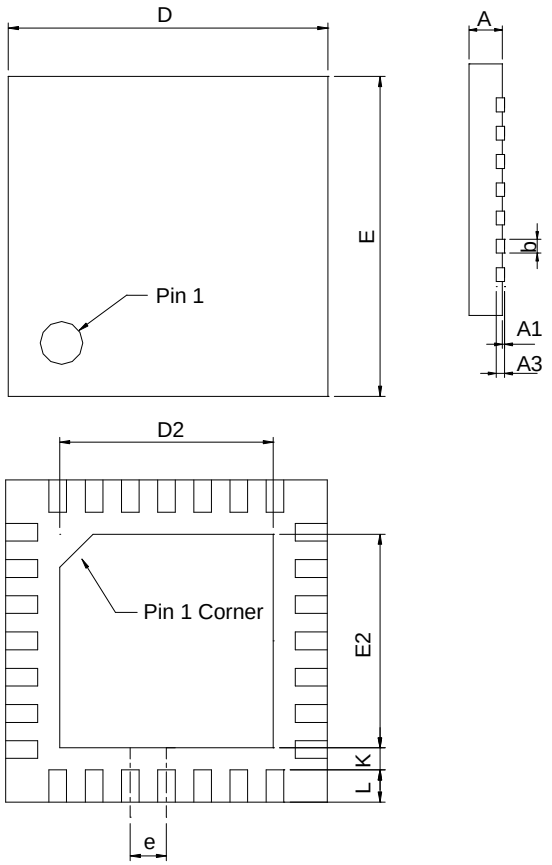


SYMBOL	TSSOP-28P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
D1	5.00	6.50	0.197	0.256
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.20	3.20	0.087	0.126
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0^o	8^o	0^o	8^o

Note : 1. Followed from JEDEC MO-153 AET.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

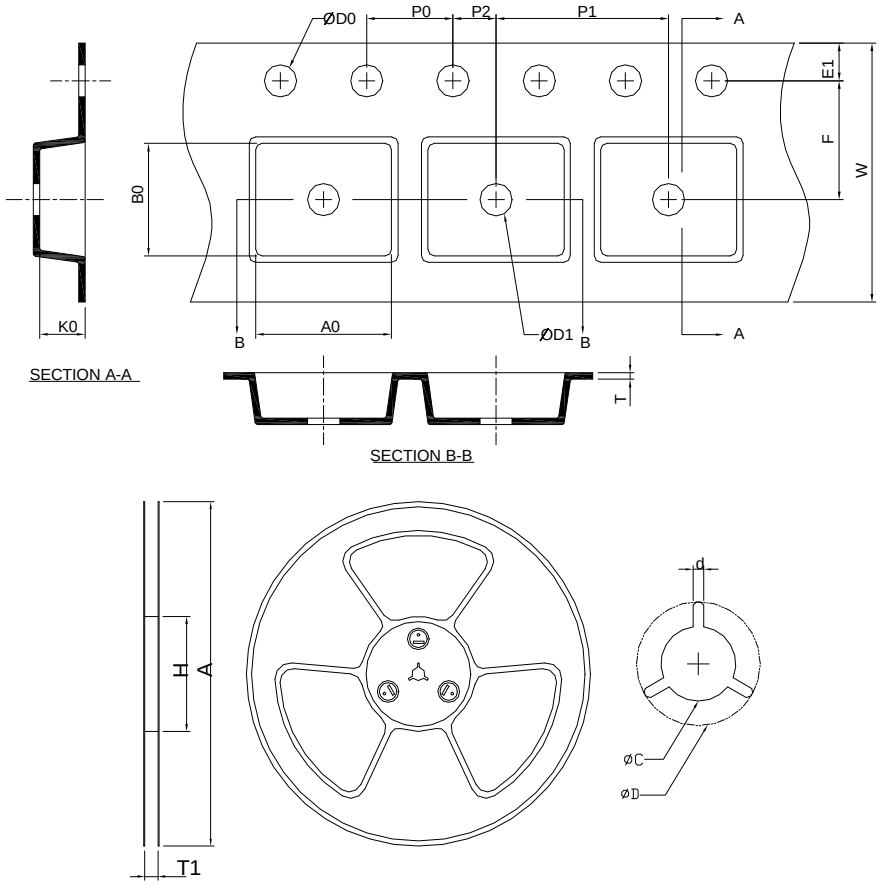
Package Information

QFN4x4-28



SYMBOL	QFN4x4-28			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.17	0.27	0.007	0.011
D	3.90	4.10	0.154	0.161
D2	2.10	2.50	0.083	0.098
E	3.90	4.10	0.154	0.161
E2	2.10	2.50	0.083	0.098
e	0.45 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Carrier Tape & Reel Dimensions



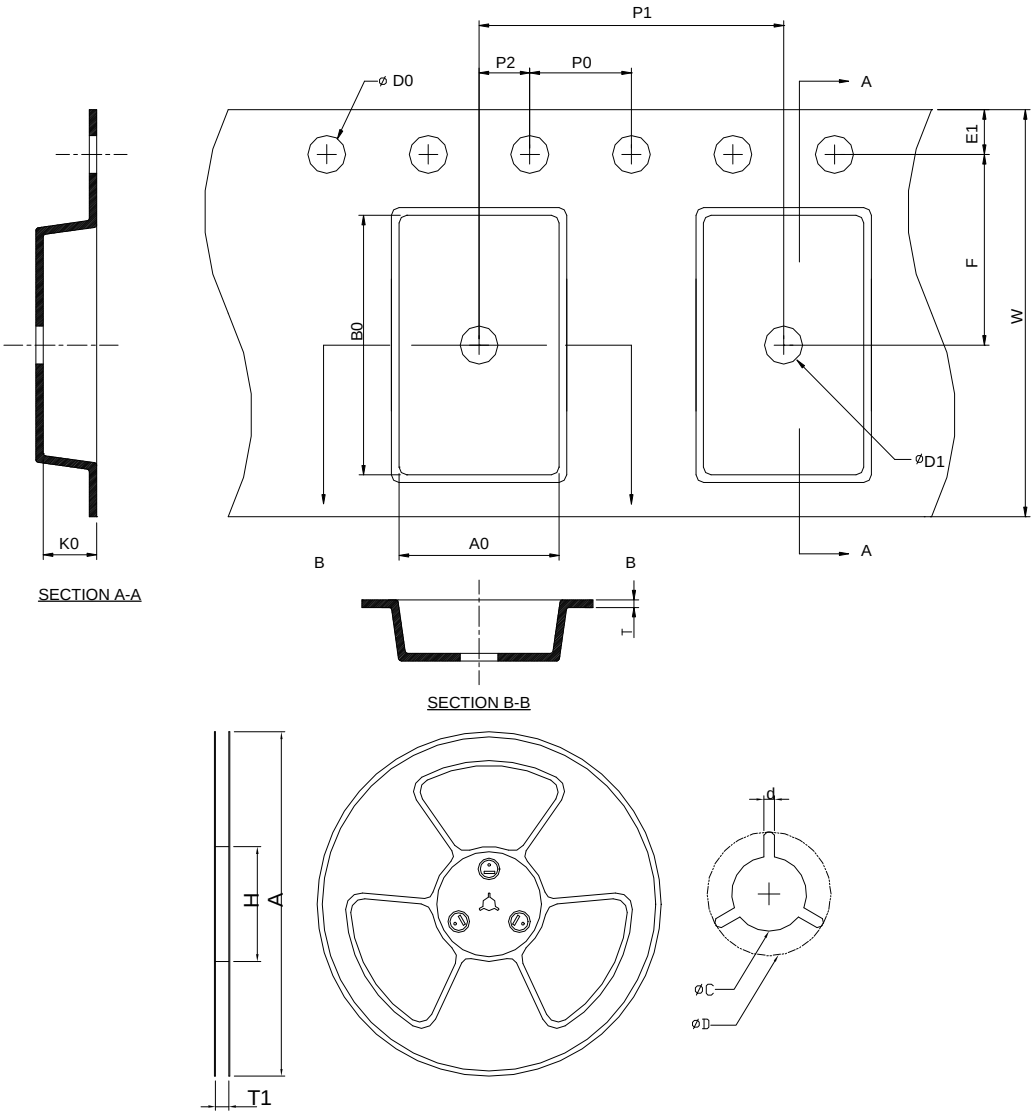
Application	A	H	T1	C	d	D	W	E1	F
QFN4x4-28	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
QFN4x4-28	Tape & Reel	3000

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSSOP-28P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	12.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.9±0.20	10.20.±0.20	1.50±0.20

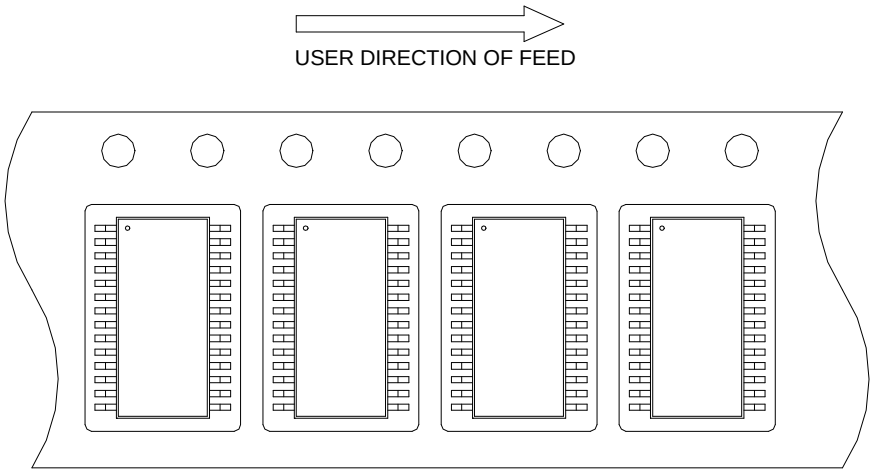
(mm)

Devices Per Unit

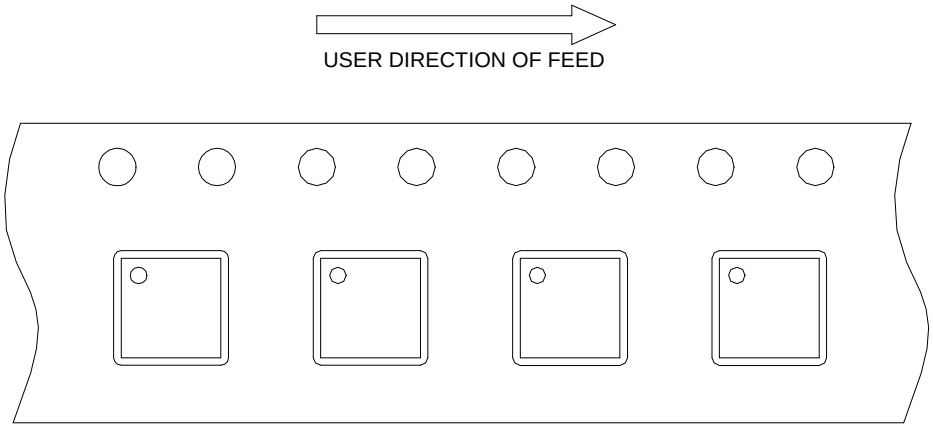
Package Type	Unit	Quantity
TSSOP-28P	Tape & Reel	2000

Taping Direction Information

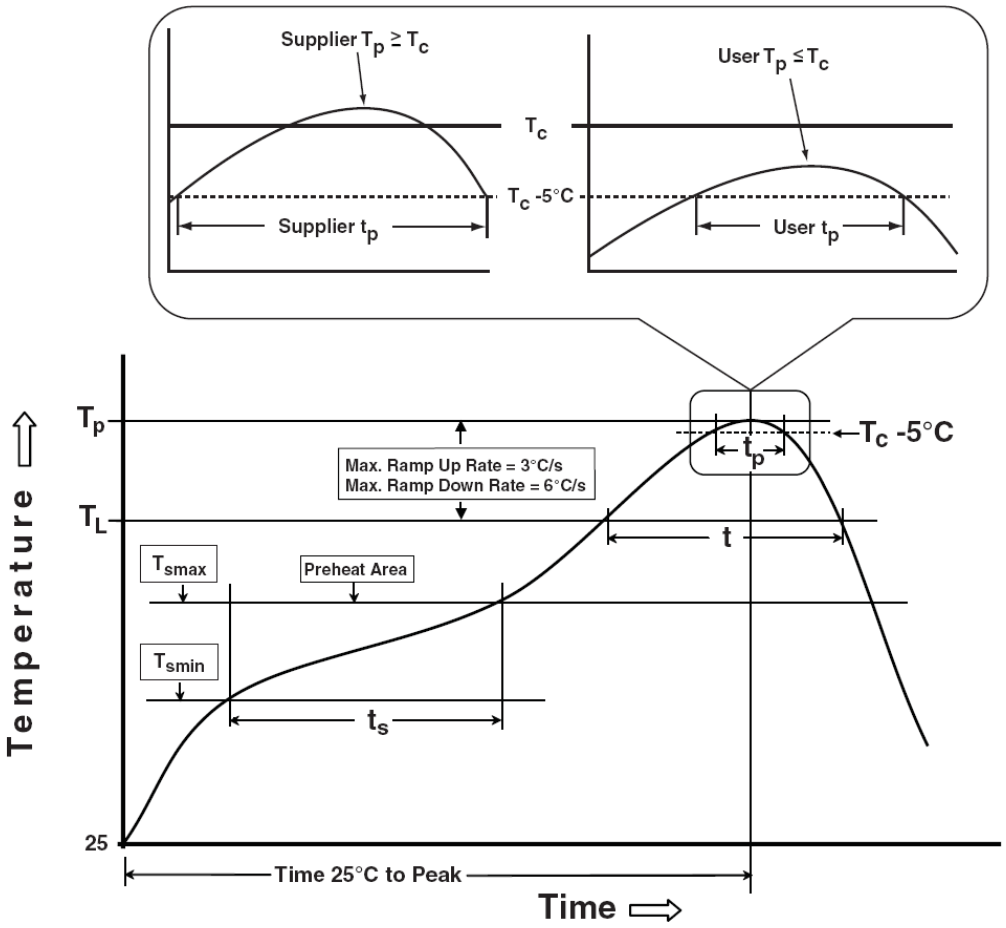
TSSOP-28P



QFN4x4-28



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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