



12N10

Power MOSFET

12A, 100V N-CHANNEL POWER MOSFET

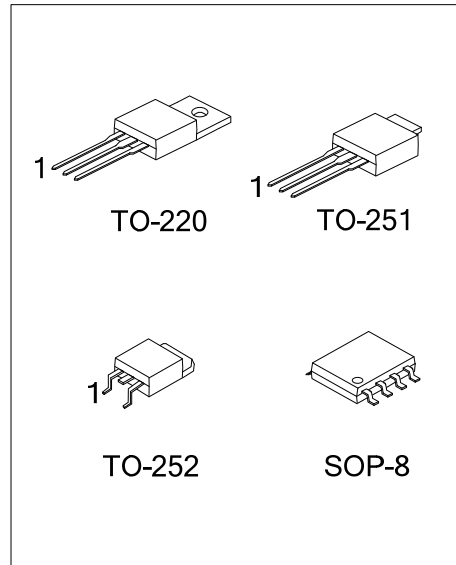
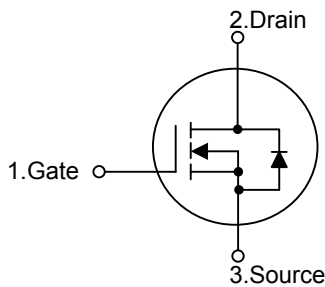
DESCRIPTION

The UTC **12N10** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with minimum on-state resistance for extremely high dense cell design, rugged avalanche characteristics and less critical alignment steps.

FEATURES

- * $R_{DS(on)} < 0.18\Omega @ V_{GS}=10V, I_D=6A$
- * High switching speed
- * Low gate charge

SYMBOL



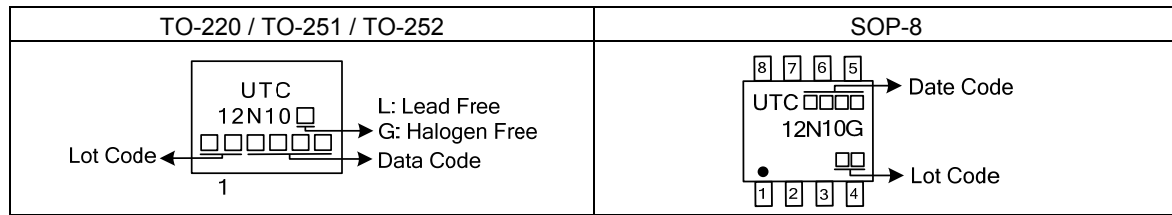
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
12N10L-TA3-T	12N10G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
12N10L-TM3-T	12N10G-TM3-T	TO-251	G	D	S	-	-	-	-	-	Tube
12N10L-TN3-R	12N10G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
-	12N10G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>12N10L-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TM3: TO-251, TN3: TO-252</p> <p>S08: SOP-8</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage ($V_{GS}=0$)		V_{DSS}	100	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous	I_D	$T_C=25^\circ\text{C}$	12	A
			$T_C=100^\circ\text{C}$	8.5	A
	Pulsed (Note 2)	I_{DM}	48	A	
Power Dissipation	TO-220	P_D	73	W	
	TO-251/TO-252		30		
	SOP-8		5		
Avalanche Energy (Note 3)		E_{AS}	100	mJ	
Junction Temperature		T_J	+150	$^\circ\text{C}$	
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by safe operating area

3. Starting $T_J = 25^\circ\text{C}$, $I_D = 12\text{A}$, $V_{DD} = 50\text{V}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^\circ\text{C/W}$
	TO-251/TO-252		100	
	SOP-8		75 (Note)	
Junction to Case	TO-220	θ_{JC}	1.71	$^\circ\text{C/W}$
	TO-251/TO-252		4.1	
	SOP-8		25 (Note)	

Note: Device mounted on 1in^2 FR-4 board with 2oz. Copper, $t = 10\text{sec}$.

■ ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=\text{Max rating}$, $V_{GS}=0\text{V}$			1	μA
Gate- Source Leakage Current	Forward	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1		3	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=6\text{A}$		0.15	0.18	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		430		pF
Output Capacitance	C_{OSS}			90		pF
Reverse Transfer Capacitance	C_{RSS}			20		pF
SWITCHING PARAMETERS (Note 1,2)						
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DD}=80\text{V}$, $I_D=12\text{A}$		7.5	10	nC
Gate to Source Charge	Q_{GS}			2.5		nC
Gate to Drain Charge	Q_{GD}			3.0		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=1\text{A}$, $R_G=9.1\Omega$, $V_{GS}=10\text{V}$ (Fig. 1)		12	24	ns
Rise Time	t_R			7	14	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			18	35	ns
Fall-Time	t_F			3	6	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				12	A
Maximum Body-Diode Pulsed Current	I_{SM}				48	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=12\text{A}$, $V_{GS}=0\text{V}$			1.2	V

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature

TEST CIRCUITS AND WAVEFORMS

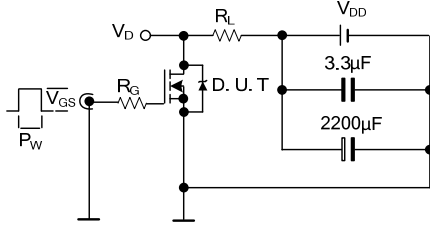


Fig. 1 Switching Times Test Circuit for Resistive Load

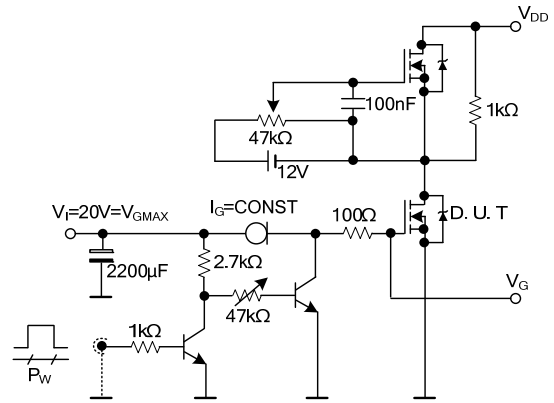


Fig. 2 Gate Charge Test Circuit

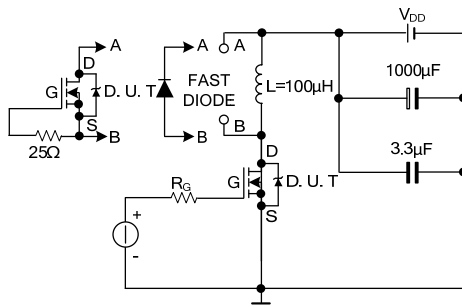


Fig. 3 Test Circuit for Inductive Load Switching and Diode Recovery Times

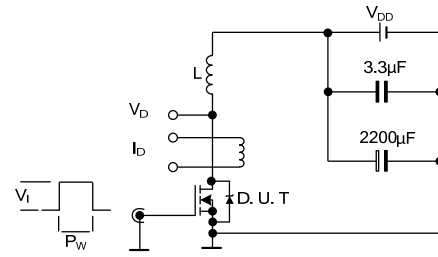


Fig. 4 Unclamped Inductive Load Test Circuit

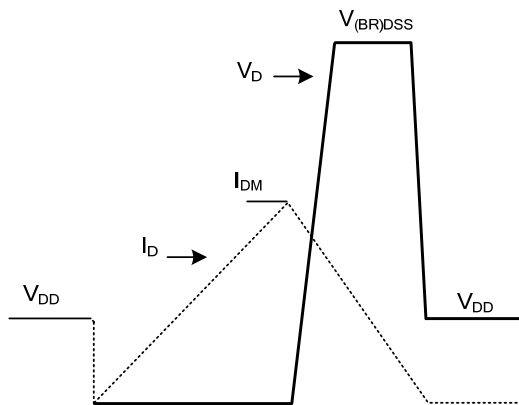
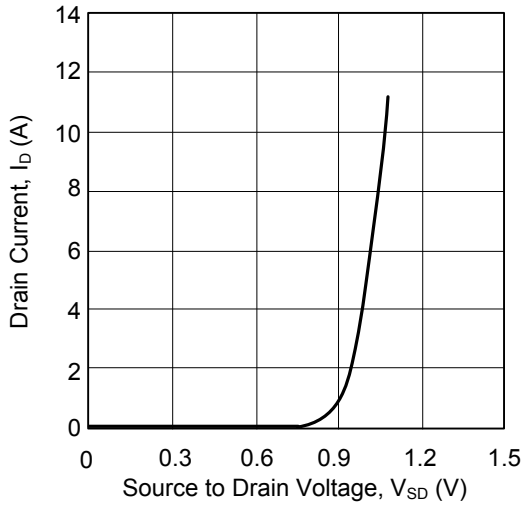


Fig. 5 Unclamped Inductive Waveform

■ TYPICAL CHARACTERISTICS

Drain Current vs. Source to Drain Voltage



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