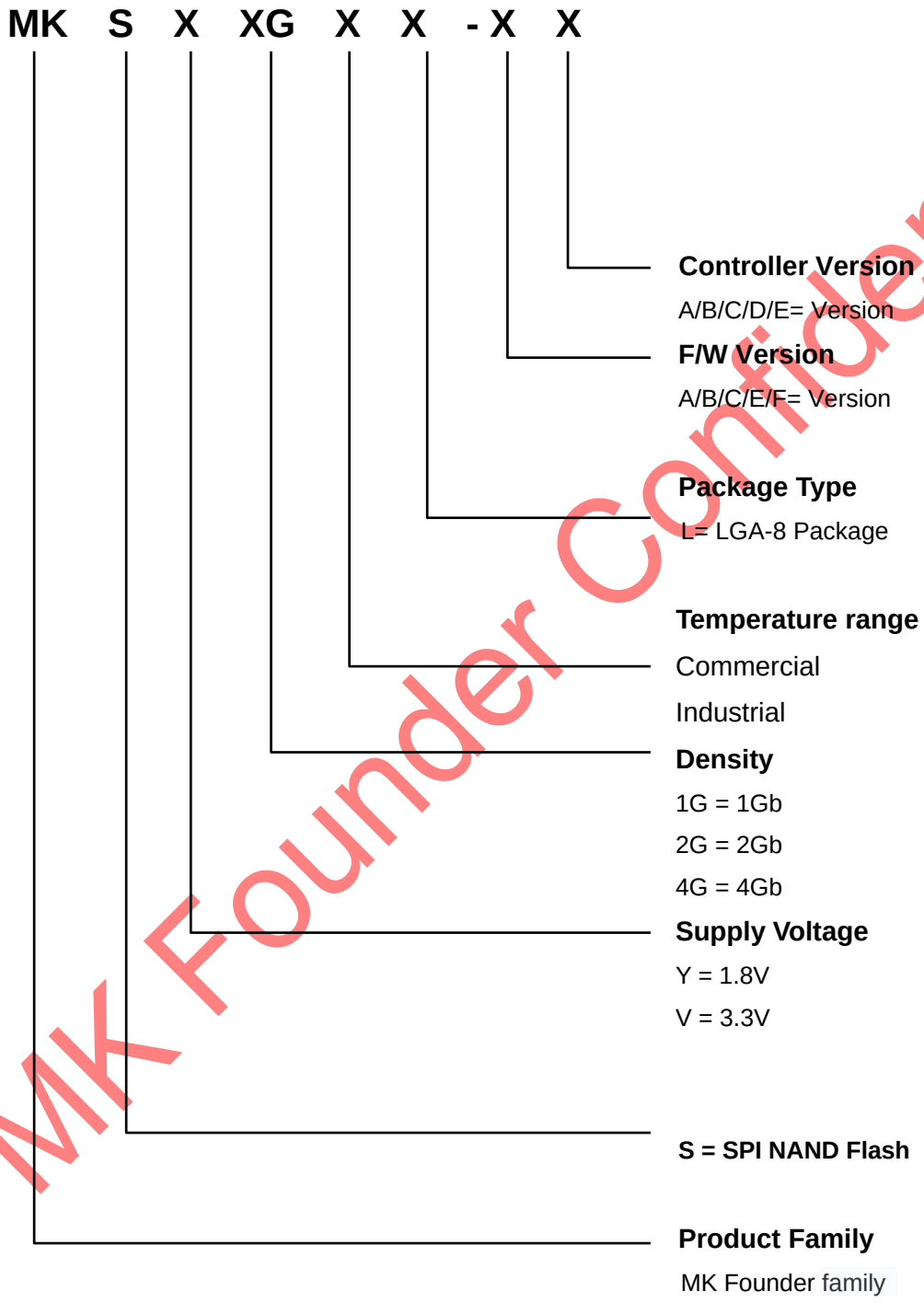
SPI NAND Flash Datasheet

Serial Peripheral Interface (SPI)

Advance
November 05, 2018

SPI NAND Part Numbering Information

MK Founder SPI NAND Flash devices are categorized in the following diagram based on the features and densities



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Revision History

Rev	Date	Comments
0.99A	February 23, 2018	Initial release.
0.99B	April 13, 2018	• Updated Table 4-1 • Updated Figure 5-5, Figure 5-7, Figure 6-1, Figure 6-2, Figure 7-1~ Figure 7-3 • Adjust Note 4 format on page 42
0.99C	October 17, 2018	• Revised the Operating Temperature: -40°C to +85°C
0.99D	November 05, 2018	• Revised the definition of SPI NAND Part Numbering Information • Revised the Operating Temperature Range • Revised the Table 2-1. SPI NAND Command Set • Revised the Figure 5-2 / Figure 6-3 / Figure 8-1

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1 Introduction

1.1 Features

- **Single-Level Cell (SLC) NAND Flash**
- **Operating Voltage Support**
  - VCC: 3.0 to 3.6V
- **Clock Frequency**
  - 80MHz
- **Standard, Dual and Quad SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- **ECC Protection**
  - 4bit & 8bit ECC for each 512bytes + Spare Area
- **Package (Pb Free and Halogen Free)**
  - 8-pin WSON-8 (8 x 6 x 0.75mm)
  - 8-pin LGA-8 (8 x 6 x 0.8mm)
- **OTP Protection**
  - 4 pages one time programmable
- **Performance (TYP)**
  - Page Program Time: 600us
  - Page Read Time: 40us
  - Block Erase Time: 3ms
- **Operating Current**
  - Read Operation Current: 25mA
  - Program Operation Current: 25mA
  - Erase Operation Current: 30mA
  - Standby Current: 120uA
- Endurance
  - P/E cycles: 60,000/cycles
- Data Retention
  - 10/years
- **Temperature**
  - Operating Temperature: -40°C to +85°C
  - Storage Temperature: -65°C to +150°C

Table 1-1. Product Information

Part Number	Density	VCC	ECC	Page Size	Block	Device	Package
MKSV1GIW-BE	1Gbits	3.3V	8bit	2048+120 Bytes	64 Pages	1024 Blocks	WSON-8
MKSV1GIL-DE	1Gbits	3.3V	4bit	2048+64 Bytes	64 Pages	1024 Blocks	LGA-8
MKSV2GIW-FE	2Gbits	3.3V	8bit	2048+128 Bytes	64 Pages	2048 Blocks	WSON-8
MKSV2GIL-DE	2Gbits	3.3V	8bit	2048+128 Bytes	64 Pages	2048 Blocks	LGA-8
MKSV2GIL-GE	2Gbits	3.3V	4bit	2048+64 Bytes	64 Pages	2048 Blocks	LGA-8

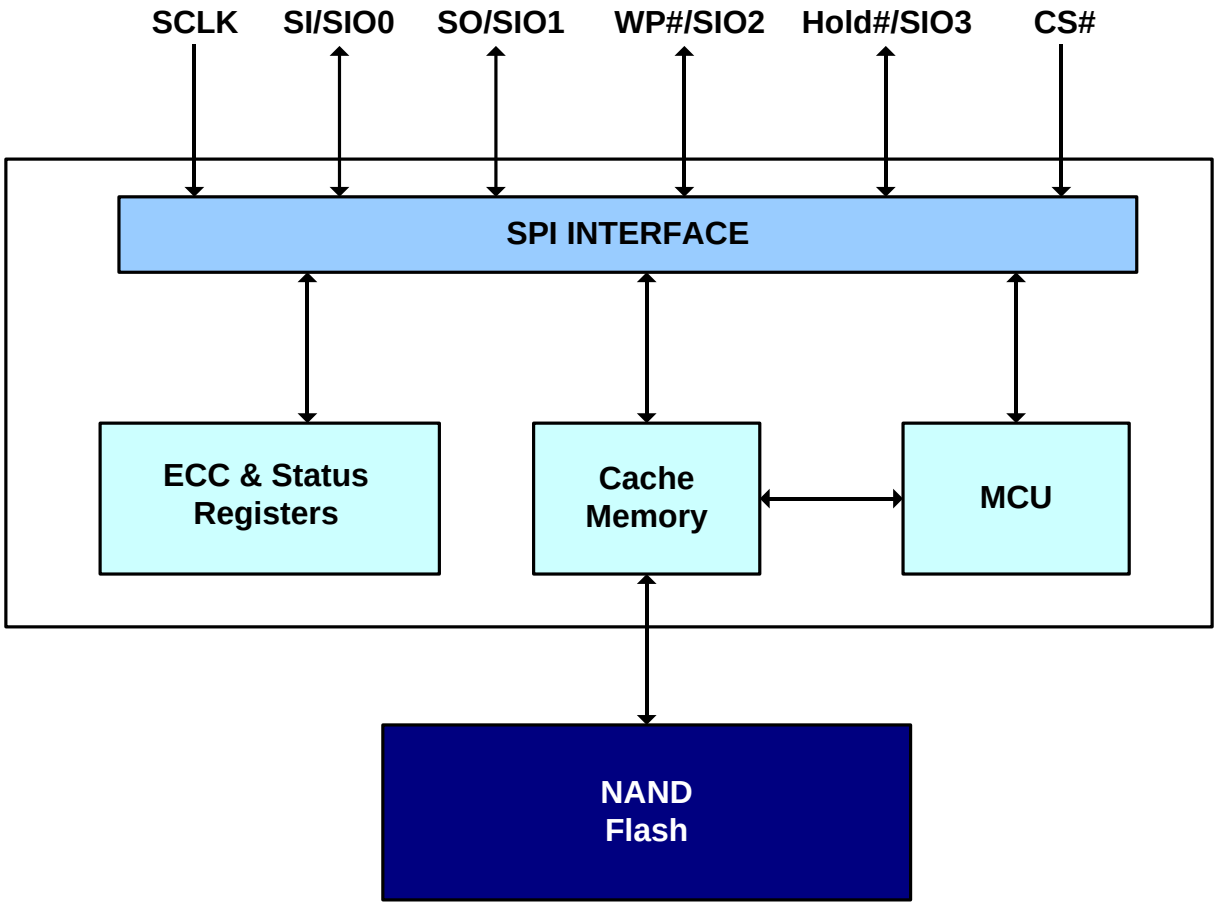
1.2 General Description

SPI (Serial Peripheral Interface) NAND provides a low cost and low pin count solution to alternate SPI-NOR in high density non-volatile memory storage solution for embedded systems.

SPI NAND is a flash memory device with SLC NAND of the standard parallel NAND. The serial electrical interface follows the industry-standard serial peripheral interface. The command sets are similar to SPI-NOR command sets. Some modifications have been made for handling NAND-specific functions. Besides, new features are added to extend applications. The SPI NAND has 8 pin counts in total, including six signal lines plus VCC and GND. The density is 512Mb through 4Gb.

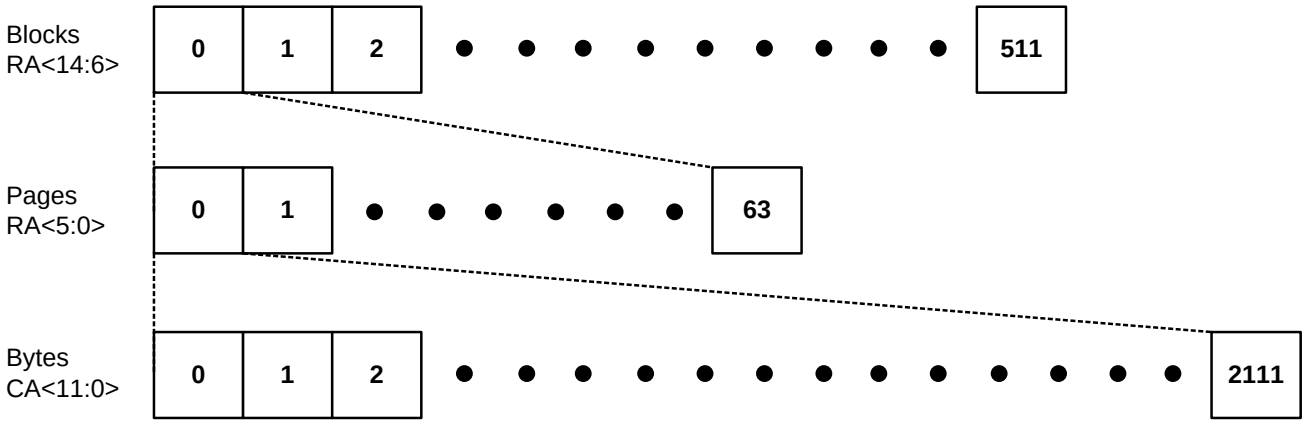
Each block of the serial NAND is subdivided into 64 programmable pages. Each page consists of a data storage region and a spare area. The data storage region is used to store user-programmed data and the spare area is typically used for memory management and error correction functions.

Figure 1-1. Functional Block Diagram



1.3 Memory Mapping Diagram

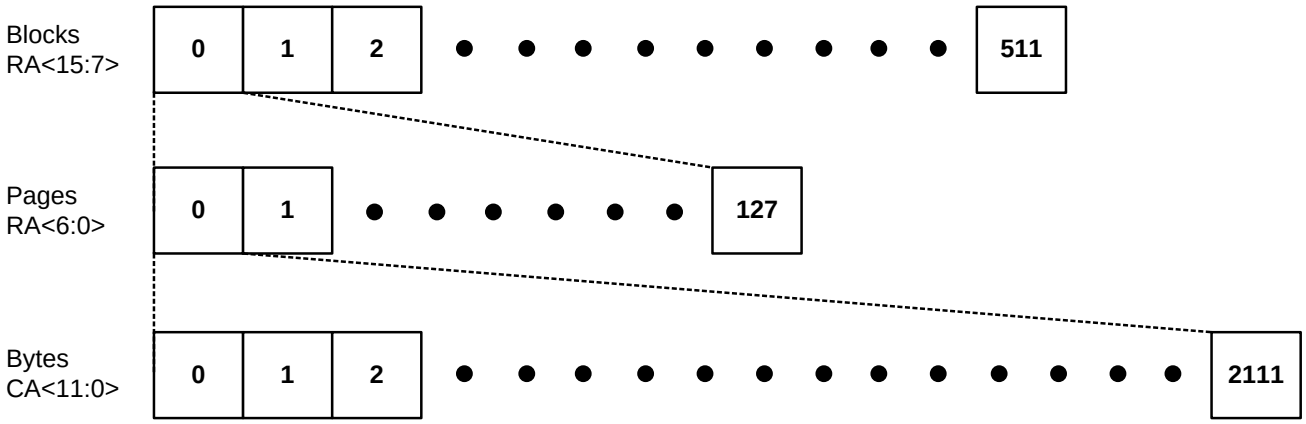
Figure 1-2. MKSV512MIL-AE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<14:6> selects a block.

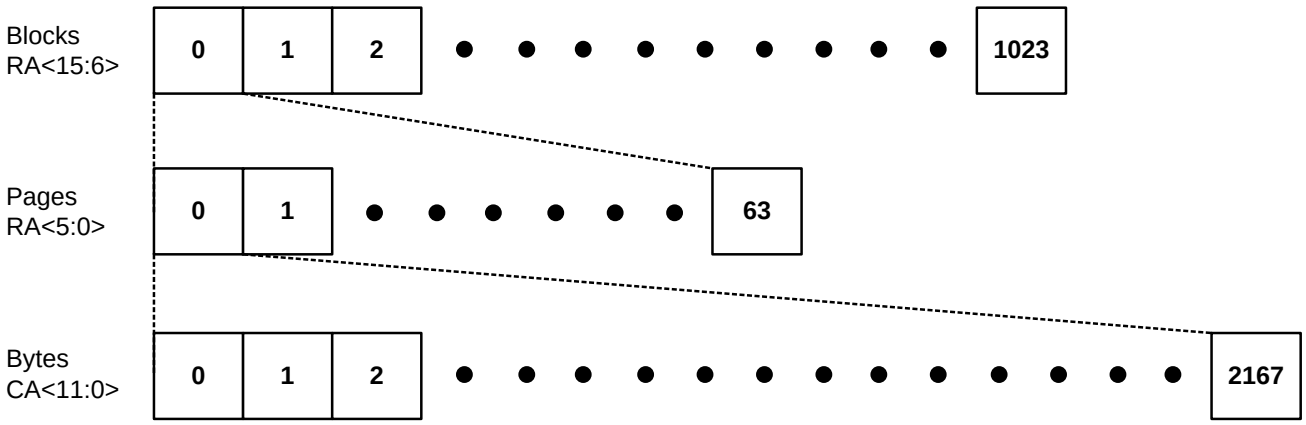
Figure 1-3. MKSV1GIW-AE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<6:0> selects a page inside a block, and RA<15:7> selects a block.

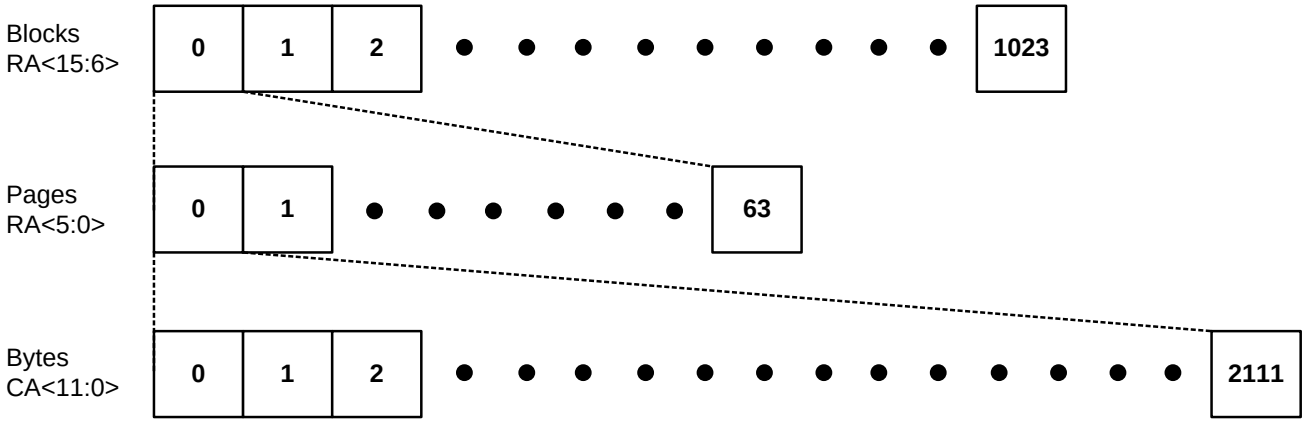
Figure 1-4. MKSV1GIW-BE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2167 are valid. Bytes 2168 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

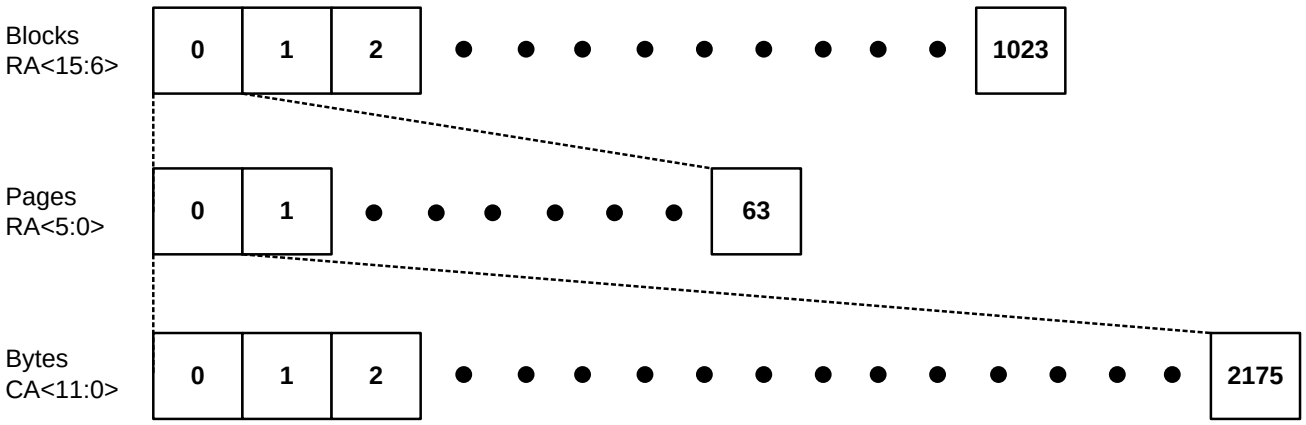
Figure 1-5. MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

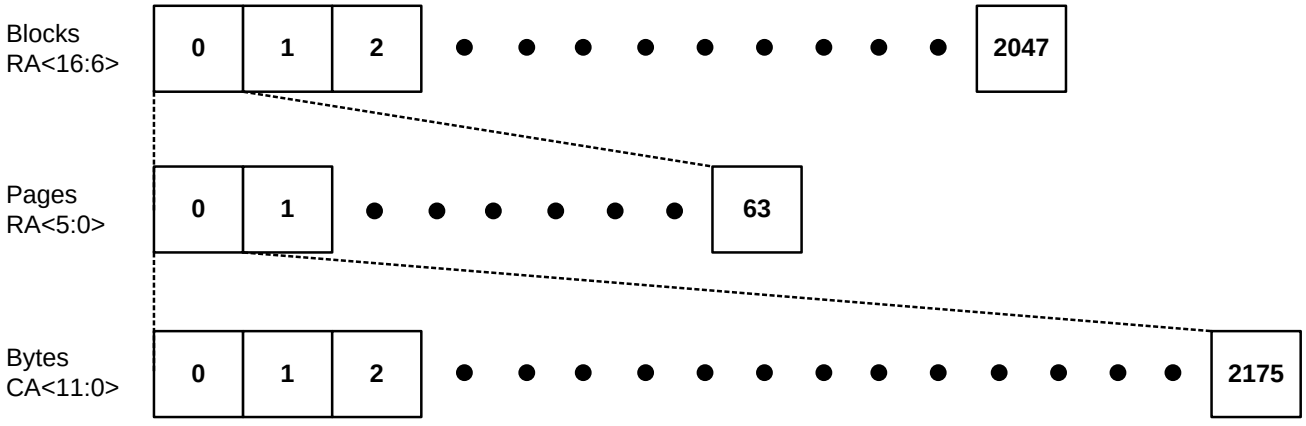
Figure 1-6. MKSV1GIW-FE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

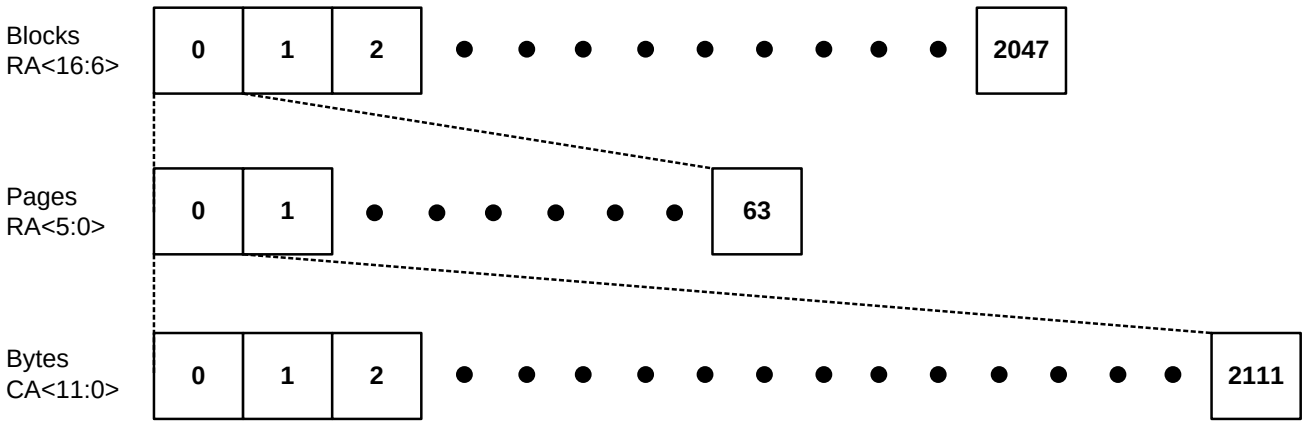
Figure 1-7. MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

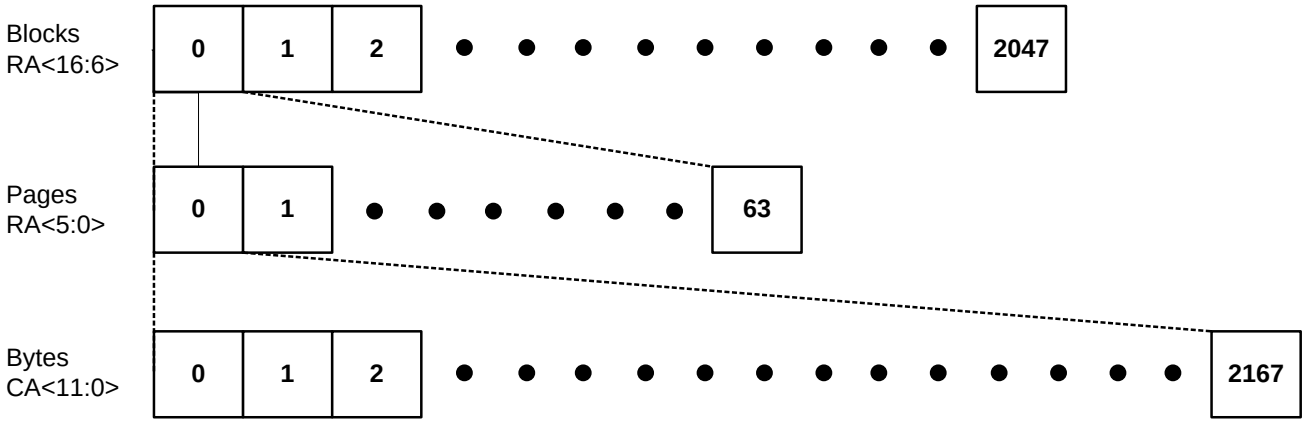
Figure 1-8. MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE



Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

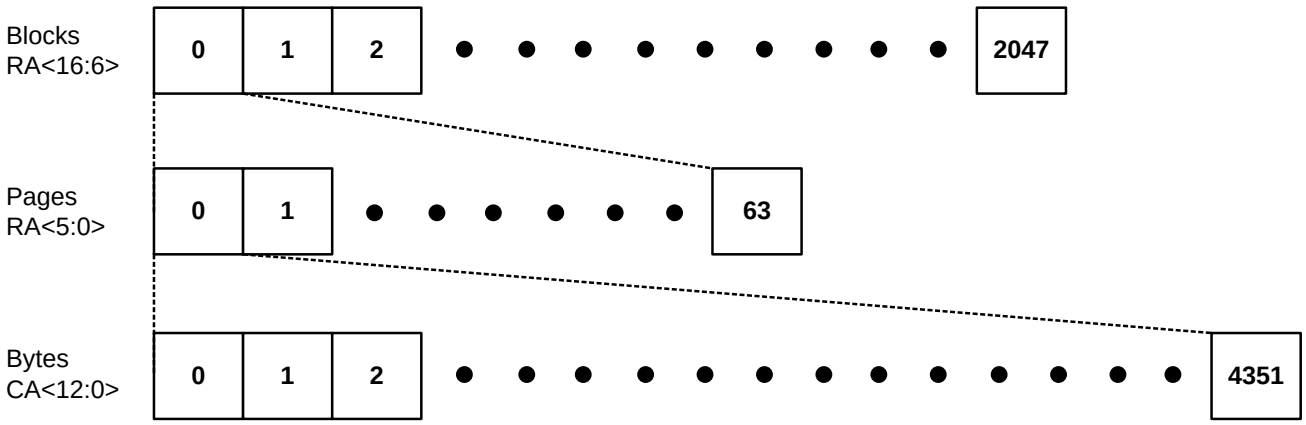
Figure 1-9. MKSV2GIW-CE



Notes:

3. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2167 are valid. Bytes 2168 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
4. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

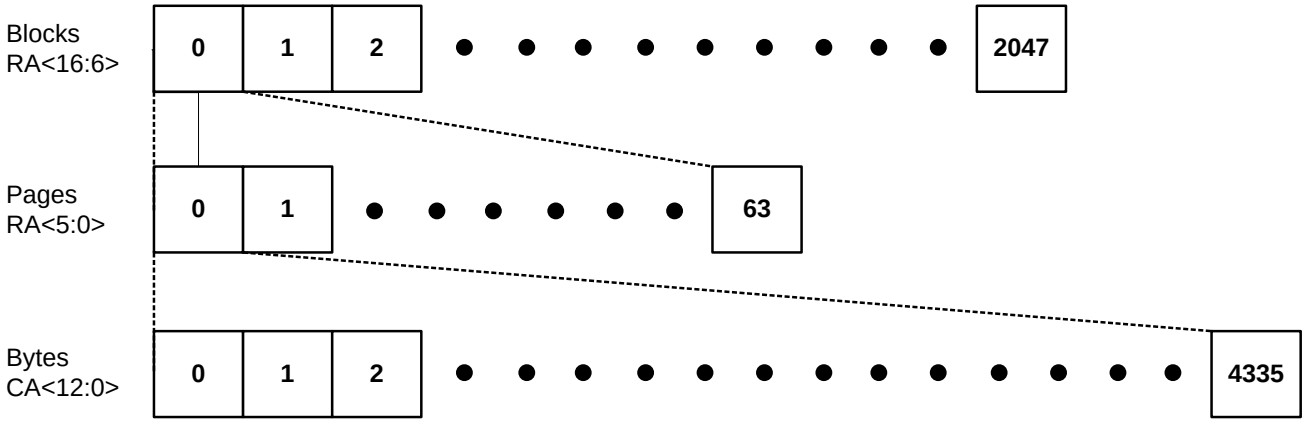
Figure 1-10. MKSV4GIW-AE



Notes:

1. CA: Column Address. The 13-bit address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4351 are valid. Bytes 4352 through 8191 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

Figure 1-11. MKSV4GIW-DE



Notes:

1. CA: Column Address. The 13-bit address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4335 are valid. Bytes 4336 through 8191 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

1.4 ECC Protection and Spare Area

Table 1-2. MKSV512MIL-AE; MKSV1GIW-DE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-GE; MKSV2GIL-HE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	803h	No	Spare Area 1	Meta data 1
804h	807h	Yes		Meta data 2
808h	80Fh	Yes		Internal ECC parity area
810h	813h	No	Spare Area 2	Meta data 1
814h	817h	Yes		Meta data 2
818h	81Fh	Yes		Internal ECC parity area
820h	823h	No	Spare Area 3	Meta data 1
824h	827h	Yes		Meta data 2
828h	82Fh	Yes		Internal ECC parity area
830h	833h	No	Spare Area 4	Meta data 1
834h	837h	Yes		Meta data 2
838h	83Fh	Yes		Internal ECC parity area

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-3. MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-DE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	803h	No	Spare Area 1	Meta data 1
804h	811h	Yes		Meta data 2
812h	81Fh	Yes		Internal ECC parity area
820h	823h	No	Spare Area 2	Meta data 1
824h	831h	Yes		Meta data 2
832h	83Fh	Yes		Internal ECC parity area
840h	843h	No	Spare Area 3	Meta data 1
844h	851h	Yes		Meta data 2
852h	85Fh	Yes		Internal ECC parity area
860h	863h	No	Spare Area 4	Meta data 1
864h	871h	Yes		Meta data 2
872h	87Fh	Yes		Internal ECC parity area

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-4. MKSV1GIW-BE; MKSV2GIW-CE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	803h	No	Spare Area 1	Meta data 1
804h	80Fh	Yes		Meta data 2
810h	81Dh	Yes		Internal ECC parity area
81Eh	821h	No	Spare Area 2	Meta data 1
822h	82Dh	Yes		Meta data 2
82Eh	83Bh	Yes		Internal ECC parity area
83Ch	83Fh	No	Spare Area 3	Meta data 1
840h	84Bh	Yes		Meta data 2
84Ch	859h	Yes		Internal ECC parity area
85Ah	85Dh	No	Spare Area 4	Meta data 1
85Eh	869h	Yes		Meta data 2
86Ah	877h	Yes		Internal ECC parity area
878h	87Fh	No	Dummy Area	

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-5. MKSV1GIW-AE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	801h	No	Spare Area 1	Meta data
802h	80Fh	Yes		Internal ECC parity area
810h	811h	No	Spare Area 2	Meta data
812h	81Fh	Yes		Internal ECC parity area
820h	821h	No	Spare Area 3	Meta data
822h	82Fh	Yes		Internal ECC parity area
830h	831h	No	Spare Area 4	Meta data
832h	83Fh	Yes		Internal ECC parity area

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-6. MKSV4GIW-AE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	9FFh	Yes	Main 5	User main data 5
A00h	BFFh	Yes	Main 6	User main data 6
C00h	DFFh	Yes	Main 7	User main data 7
E00h	FFFh	Yes	Main 8	User main data 8
1000h	1003h	No	Spare Area 1	Meta data 1
1004h	1011h	Yes		Meta data 2
1012h	101Fh	Yes		Internal ECC parity area
1020h	1023h	No	Spare Area 2	Meta data 1
1024h	1031h	Yes		Meta data 2
1032h	103Fh	Yes		Internal ECC parity area
1040h	1043h	No	Spare Area 3	Meta data 1
1044h	1051h	Yes		Meta data 2
1052h	105Fh	Yes		Internal ECC parity area
1060h	1063h	No	Spare Area 4	Meta data 1
1064h	1071h	Yes		Meta data 2
1072h	107Fh	Yes		Internal ECC parity area
1080h	1083h	No	Spare Area 5	Meta data 1
1084h	1091h	Yes		Meta data 2
1092h	109Fh	Yes		Internal ECC parity area
10A0h	10A3h	No	Spare Area 6	Meta data 1
10A4h	10B1h	Yes		Meta data 2
10B2h	10BFh	Yes		Internal ECC parity area
10C0h	10C3h	No	Spare Area 7	Meta data 1
10C4h	10D1h	Yes		Meta data 2
10D2h	10DFh	Yes		Internal ECC parity area
10E0h	10E3h	No	Spare Area 8	Meta data 1
10E4h	10F1h	Yes		Meta data 2
10F2h	10FFh	Yes		Internal ECC parity area

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-7. MKSV4GIW-DE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	9FFh	Yes	Main 5	User main data 5
A00h	BFFh	Yes	Main 6	User main data 6
C00h	DFFh	Yes	Main 7	User main data 7
E00h	FFFh	Yes	Main 8	User main data 8
1000h	1003h	No	Spare Area 1	Meta data 1
1004h	100Fh	Yes		Meta data 2
1010h	101Dh	Yes		Internal ECC parity area
101Eh	1021h	No	Spare Area 2	Meta data 1
1022h	102Dh	Yes		Meta data 2
102Eh	103Bh	Yes		Internal ECC parity area
103Ch	103Fh	No	Spare Area 3	Meta data 1
1040h	104Bh	Yes		Meta data 2
104Ch	1059h	Yes		Internal ECC parity area
105Ah	105Dh	No	Spare Area 4	Meta data 1
105Eh	1069h	Yes		Meta data 2
106Ah	1077h	Yes		Internal ECC parity area
1078h	107Bh	No	Spare Area 5	Meta data 1
107Ch	1087h	Yes		Meta data 2
1088h	1095h	Yes		Internal ECC parity area
1096h	1099h	No	Spare Area 6	Meta data 1
109Ah	10A5h	Yes		Meta data 2
10A6h	10B3h	Yes		Internal ECC parity area
10B4h	10B7h	No	Spare Area 7	Meta data 1
10B8h	10C3h	Yes		Meta data 2
10C4h	10D1h	Yes		Internal ECC parity area
10D2h	10D5h	No	Spare Area 8	Meta data 1
10D6h	10E1h	Yes		Meta data 2
10E2h	10EFh	Yes		Internal ECC parity area
10F0h	10FFh	No	Dummy Area	

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-8. MKSV1GIL-AE; MKSV2GIL-BE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	807h	Yes	Spare Area 1	Meta data
808h	80Fh	Yes		Internal ECC parity area
810h	817h	Yes	Spare Area 2	Meta data
818h	81Fh	Yes		Internal ECC parity area
820h	827h	Yes	Spare Area 3	Meta data
828h	82Fh	Yes		Internal ECC parity area
830h	837h	Yes	Spare Area 4	Meta data
838h	83Fh	Yes		Internal ECC parity area

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-9. MKSV2GIL-AE

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main 1	User main data 1
200h	3FFh	Yes	Main 2	User main data 2
400h	5FFh	Yes	Main 3	User main data 3
600h	7FFh	Yes	Main 4	User main data 4
800h	817h	Yes	Spare Area 1	Meta data
818h	81Fh	Yes		Internal ECC parity area
820h	837h	Yes	Spare Area 2	Meta data
838h	83Fh	Yes		Internal ECC parity area
840h	857h	Yes	Spare Area 3	Meta data
858h	85Fh	Yes		Internal ECC parity area
860h	877h	Yes	Spare Area 4	Meta data
878h	87Fh	Yes		Internal ECC parity area

Note: For ECC parity area the user can only get FF when ECC on.

Table 1-10. Pin Descriptions

Pin Name	Type	Description
SCLK	Input	Serial Clock
SI/SIO0	I/O	Serial Data Input / Serial Data IO0
SO/SIO1	I/O	Serial Data Output / Serial Data IO1
WP#/SIO2	I/O	Write Protect / Serial Data IO2
Hold#/SIO3	I/O	Hold / Serial Data IO3
CS#	Input	Chip Select
VCC	Supply	Power Supply
GND	Ground	Ground

Figure 1-12. Connection Diagram (including SPI controller and SPI NAND)

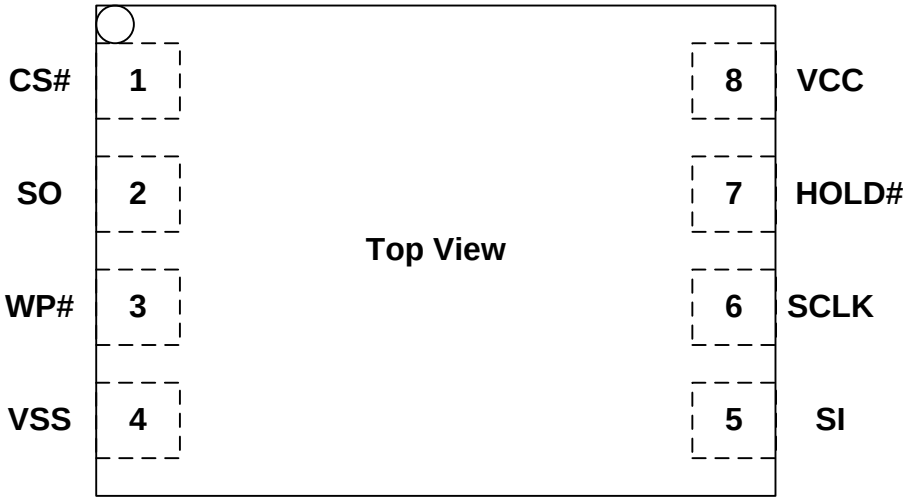


Figure 1-13. Ball Assignment (Top View) for ball array 4 x 6

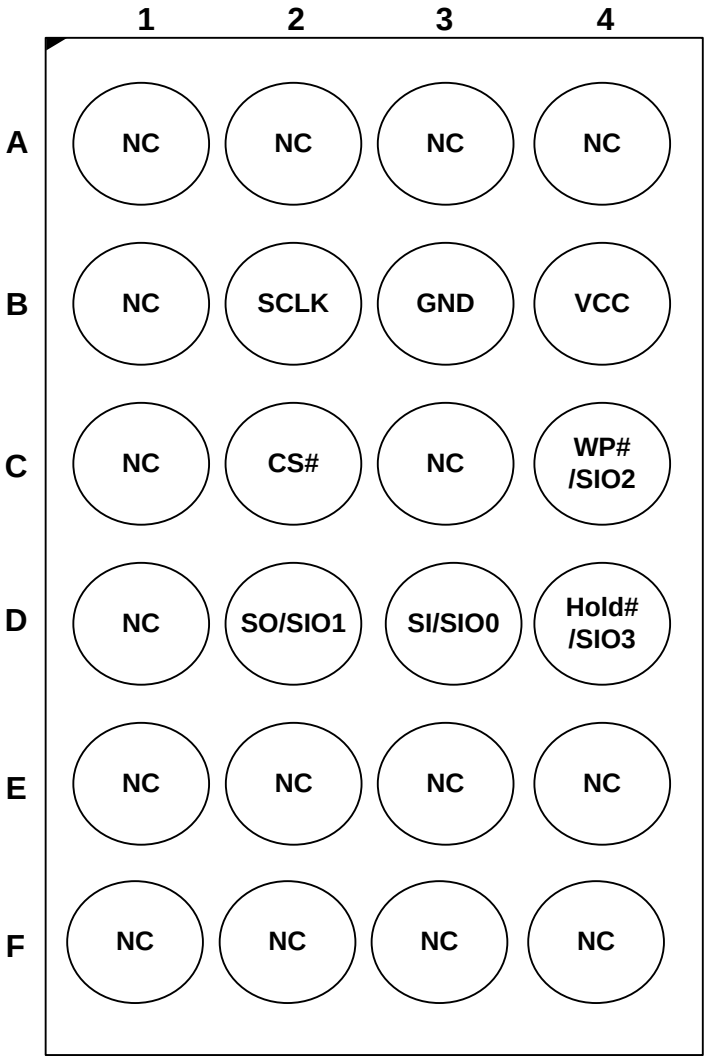
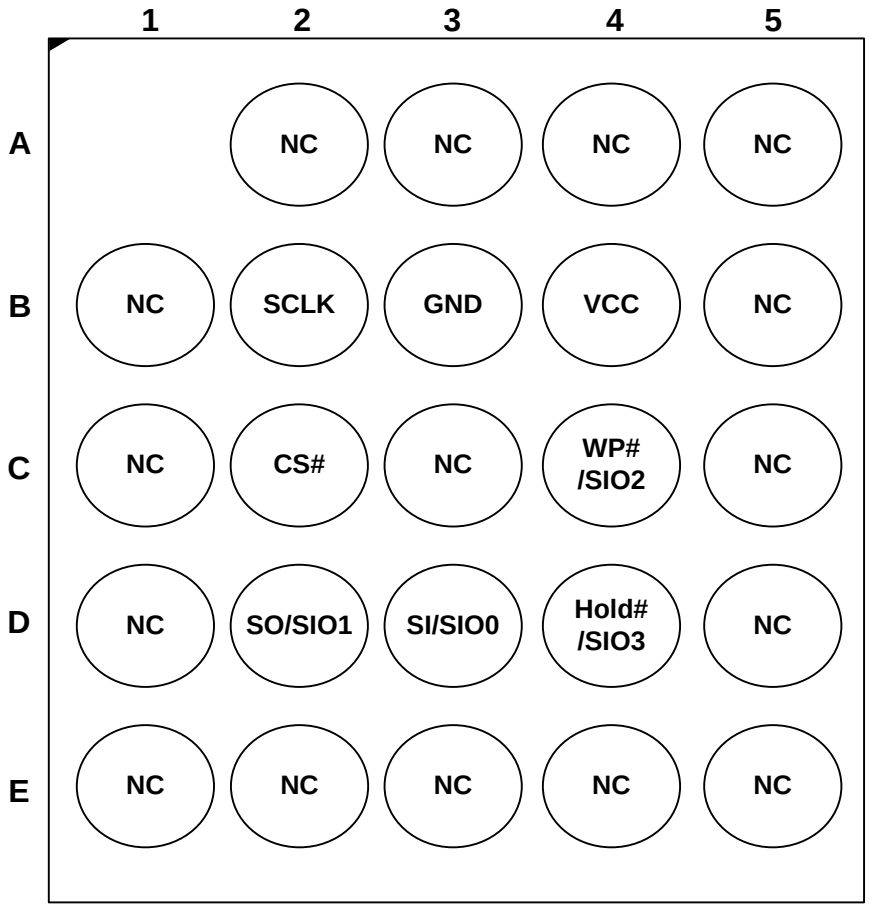


Figure 1-14. Ball Assignment (Top View) for ball array 5 x 5-1



2 Device Operation

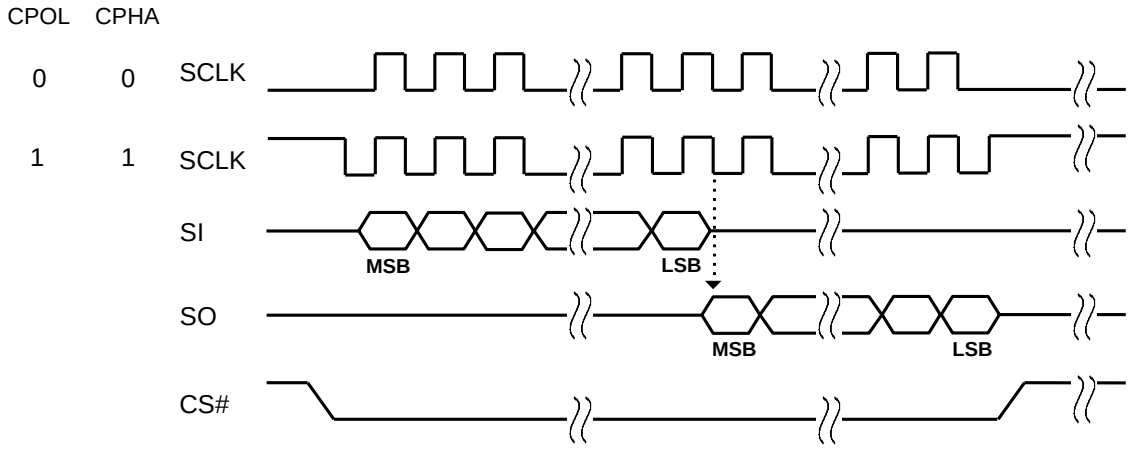
2.1 SPI Mode

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode 3. The timing diagrams shown in this data sheet are mode 0.

Figure 2-1. Timing Diagram of SPI Modes



Note:

1. SCLK provides interface timing for SPI NAND. Address, data and commands are latched on the rising edge of SCLK. Data is placed on SO at the falling edge of SCLK.
2. When CS# is 0, the device is placed in active mode. When CS# goes 1, the device is placed in inactive mode and SO is High-Z.

2.1.1 Standard SPI

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out (SO).

2.1.2 Dual SPI

The device supports dual SPI operation with x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1.

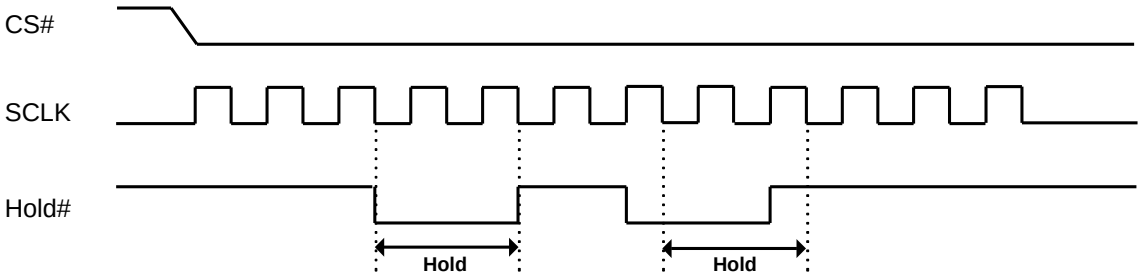
2.1.3 Quad SPI

The device supports the x4 and Quad commands operation. These commands allow data to be transferred to or from the device at four times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1. The WP# and the HOLD# pins become SIO2 and SIO3.

2.2 Hold Mode

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of writing status register, programming or erasing in progress.

Figure 2-2. Hold Condition Diagram



Note:
Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. When SCLK is HIGH and HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

2.3 Write Protection Mode

Write protect (WP#) provides hardware protection mode. The WP# prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

Table 2-1. SPI NAND Command Set

Command	Op Code	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Nth Byte
Write Disable	04H	-	-	-	-	-	-
Write Enable	06H	-	-	-	-	-	-
Block Erase (Block size)	D8H(3)	A23-A16	A15-A8	A7-A0	-	-	-
Program Load	02H	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load x4 IO	32H	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Execute	10H(3)	A23-A16	A15-A8	A7-A0	-	-	-
Program Load Random Data	84H(1)	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load Random Data x4 IO	C4H/34H(1)	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Load Random Data Quad IO	72H(1)(2)	A15-A0	(D7-D0)x4	Next data	Next data	Next data	-
Page Read (to Cache)	13H(3)	A23-A16	A15-A8	A7-A0	-	-	-
Read from Cache x1 IO	03H/0BH	A15-A8	A7-A0	Dummy	D7-D0	Next data	Wrap
Read from Cache x2 IO	3BH	A15-A8	A7-A0	Dummy	(D7-D0)x2	Next data	Wrap
Read from Cache x4 IO	6BH	A15-A8	A7-A0	Dummy	(D7-D0)x4	Next data	Wrap
Read from Cache Dual IO	BBH	A15-A0	Dummy	(D7-D0)x2	Next data	Next data	Wrap
Read from Cache Quad IO	EBH(2)	A15-A0	Dummy	(D7-D0)x4	Next data	Next data	Wrap
Read ID	9FH(3)	A7-A0	MID	DID	Wrap	Wrap	Wrap
Reset	FFH	-	-	-	-	-	-
Get Feature	0FH(3)	A7-A0	D7-D0	-	-	-	-
Set Feature	1FH(3)	A7-A0	D7-D0	-	-	-	-

Note:

1. These commands are only available in Internal Data Move operation.
2. Quad Enable (QE) bit needs to be set to 1 when these commands are issued.
3. If QE = 1, do not make HOLD#/SIO3 = 0, when these commands are issued.

3 Write Operations

The WRITE ENABLE (WREN, 06H) command is for setting the Write Enable Latch (WEL) bit. The WRITE DISABLE (WRDI, 04H) command is for clearing the WEL bit.

As with any command that changes the memory contents, the WRITE ENABLE command must be executed at first in order to set the WEL bit to 1. For more information, please refer to the Page Read operation sequence, PAGE PROGRAM operation sequence, Internal Data Move operation sequence, BLOCK ERASE operation sequence and OTP operation sequence.

Figure 3-1. Write Enable (06H) Sequence Diagram

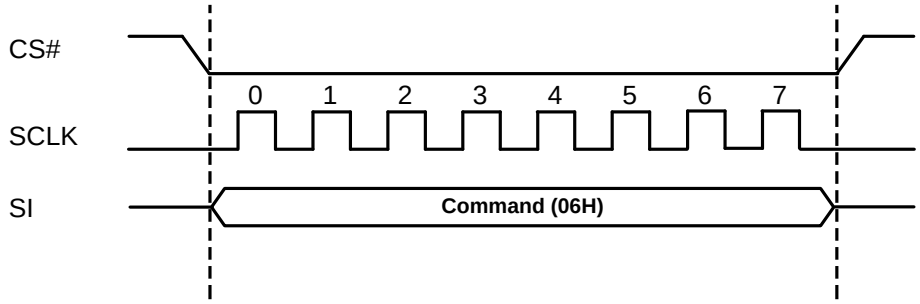
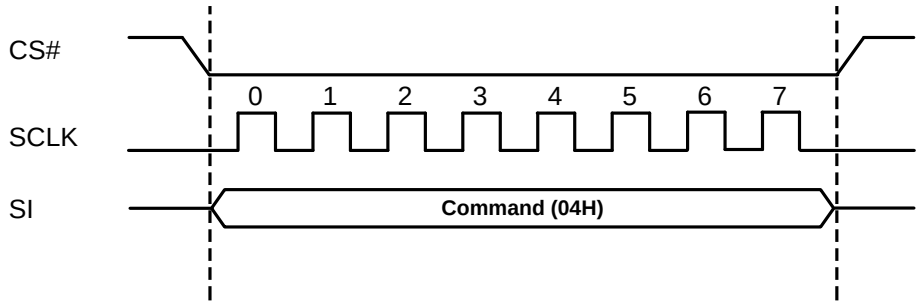


Figure 3-2. Write Disable (04H) Sequence Diagram



4 Feature Operations

The GET FEATURE (0FH) and SET FEATURE (1FH) commands are used to monitor the device status and alter the device behavior.

Figure 4-1. Get Feature (0FH) Sequence Diagram

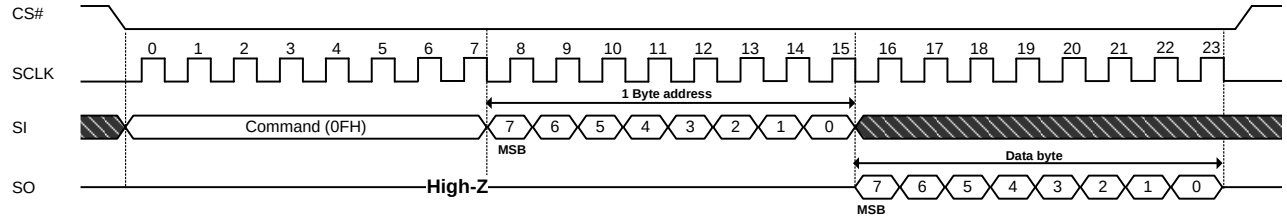
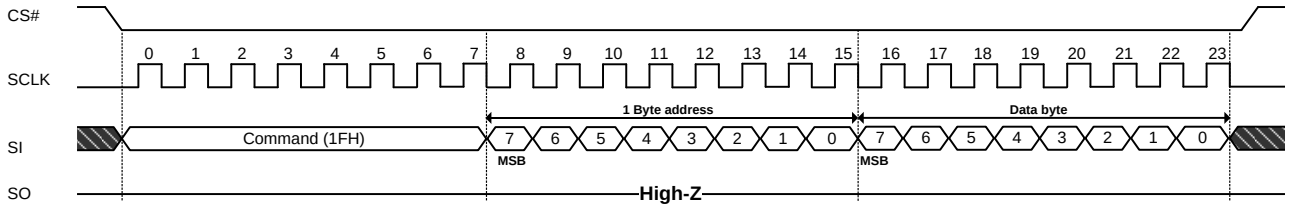


Figure 4-2. Set Feature (1FH) Sequence Diagram



Notes : If the status OIP = 1, the 'Set Feature (1FH)' command will be disable

Table 4-1. Feature Register Table

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0H	BRWD$^{(R/W)}$	Reserved	BP2$^{(R/W)}$	BP1$^{(R/W)}$	BP0$^{(R/W)}$	INV$^{(R/W)}$	CMP$^{(R/W)}$	Reserved
OTP	B0H	OTP_PRT$^{(R)}$	OTP_EN$^{(R/W)}$	Reserved	ECC_EN$^{(R/W)}$	Reserved	Reserved	Reserved	QE$^{(R/W)}$
Status	C0H	Reserved	Reserved	ECCS1$^{(R)}$	ECCS0$^{(R)}$	P_FAIL$^{(R)}$	E_FAIL$^{(R)}$	WEL$^{(R)}$	OIP$^{(R)}$

Note:

1. (R/W)：This bit can be read & programmed.
2. (R)：This bit only can be read.
3. Reserved：Default value 0h

5 Read Operations

5.1 Read ID (9FH)

The Read ID command is used to identify the SPI NAND. The Read ID command outputs the manufacturer ID with address byte 00H and outputs the device ID when address byte is 01H.

Figure 5-1. Read ID (9FH) Sequence Diagram

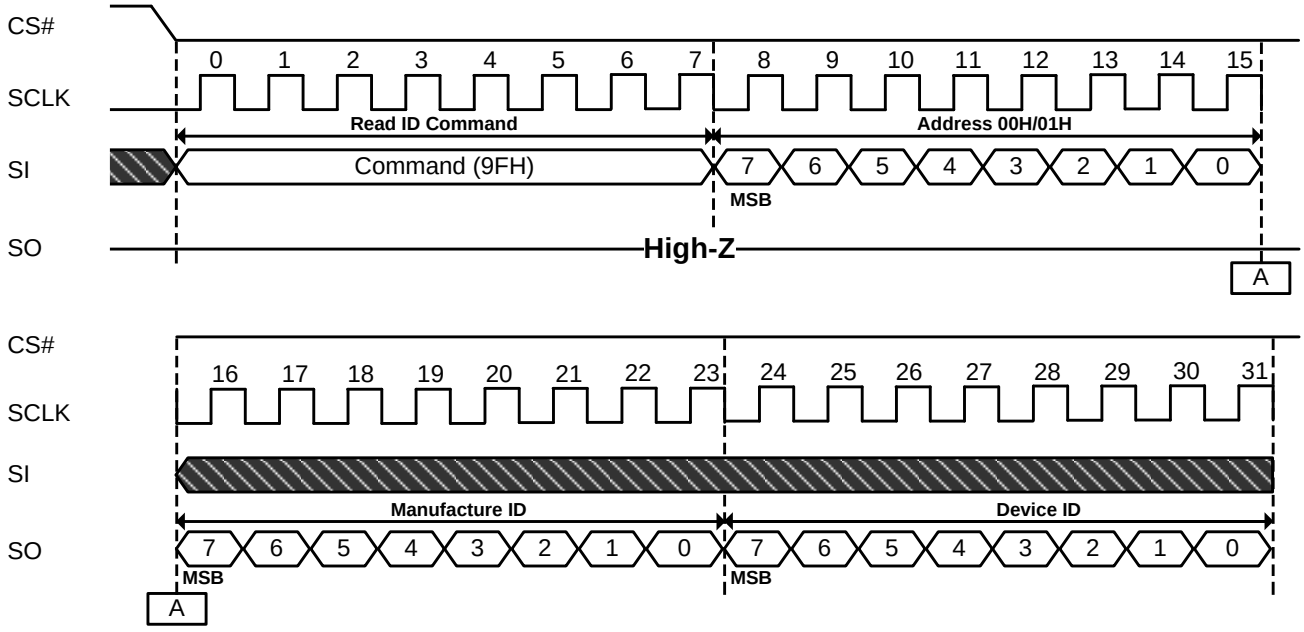


Table 5-1. ID Definition Table

Address Byte	Value	R/W	Description
00H	D5H	R	Manufacturer ID: MK Founder
01H	01H	R	Device ID: MKSV512MIL-AE
01H	19H	R	Device ID: MKSV1GIW-AE
01H	11H	R	Device ID: MKSV1GIW-BE
01H	1DH	R	Device ID: MKSV1GIW-DE
01H	09H	R	Device ID: MKSV1GIW-FE
01H	18H	R	Device ID: MKSV1GIL-AE
01H	1CH	R	Device ID: MKSV1GIL-DE
01H	12H	R	Device ID: MKSV2GIB-AE
01H	0AH	R	Device ID: MKSV2GIW-CE
01H	1EH	R	Device ID: MKSV2GIW-DE
01H	10H	R	Device ID: MKSV2GIW-FE
01H	13H	R	Device ID: MKSV2GIL-AE
01H	14H	R	Device ID: MKSV2GIL-BE
01H	17H	R	Device ID: MKSV2GIL-DE
01H	1FH	R	Device ID: MKSV2GIL-GE
01H	1BH	R	Device ID: MKSV2GIL-HE
01H	03H	R	Device ID: MKSV4GIW-AE
01H	0BH	R	Device ID: MKSV4GIW-DE

5.2 Page Read (13H)

The Page Read (13H) command transfers the data from the NAND array to the cache memory. The command sequence is described as follows:

I. 13H (Page Read to Cache)
II. 0FH (GET FEATURE command to read the status)
III. Read from Cache memory
- 03H or 0BH (Read from Cache x1 IO) / 3BH (Read from Cache x2 IO) / 6BH (Read from Cache x4 IO)
- BBH (Read from Cache Dual IO) / EBH (Read from Cache Quad IO)

The Page Read command requires a 24-bit address consisting of dummy bits and block/page address bits. After the block/page addresses are registered, the device starts transferring from the main array to the cache register, and is busy for tRD time. During the busy time, the GET FEATURE command needs to be issued to monitor the status of Page Read. After finishing the Page Read successfully, the Read from Cache command can be issued in order to read the data out of the cache. The Read from Cache command requires 16 bits of column address which consists of wrap bits and column address bits. The number of bits of column address depends on the page size in different flash.

Value of wrap bit is defined as follows:

Table 5-2. Wrap Bit (2K/page)

Wrap <3>	Wrap <2>	Wrap <1>	Wrap <0>	Wrap Length (Byte)	Part Number
0	0	X	X	2168(1)	MKSV1GIW-BE; MKSV2GIW-CE
				2112(2)	MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
				2176(3)	MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE
0	1	X	X	2048	-
1	0	X	X	64	-
1	1	X	X	16	-

Note:
1. When 2K/page, spare size is 120 bytes. Wrap bit has 4 bits and located at the first 4 bits in 16-bits column address.
2. When 2K/page, spare size is 64 bytes. Wrap bit has 4 bits and located at the first 4 bits in 16-bits column address.
3. When 2K/page, spare size is 128 bytes. Wrap bit has 4 bits and located at the first 4 bits in 16-bits column address.

Table 5-3. Wrap Bit (4K/page)

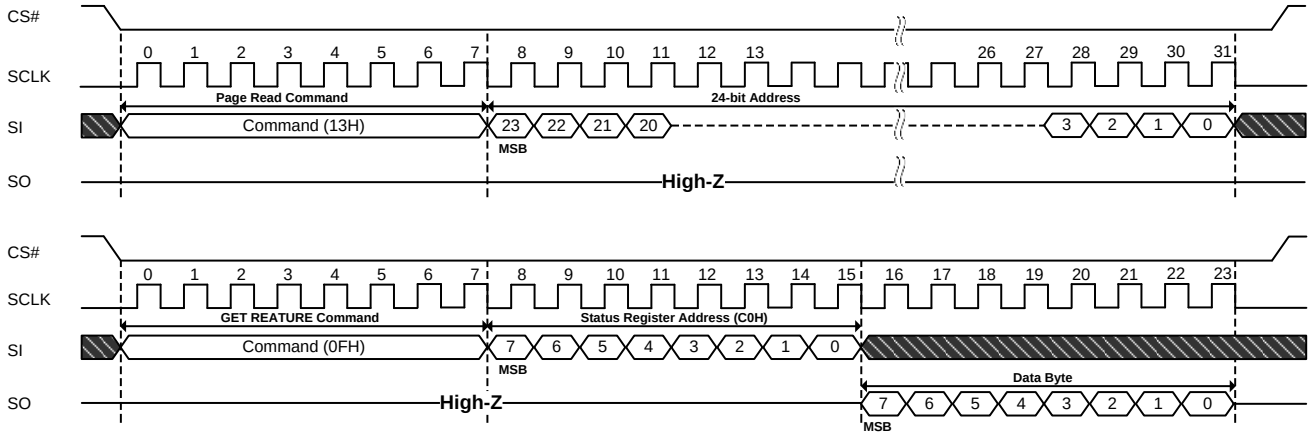
Wrap <2>	Wrap <1>	Wrap <0>	Wrap Length (Byte)	Part Number
0	0	X	4352(1)	MKSV1GIW-AE
			4336(2)	MKSV4GIW-DE
0	1	X	4096	-
1	0	X	64	-
1	1	X	16	-

Note:
4. When 4K/page, spare size is 256 bytes. Wrap bit has 3 bits and located at the first 3 bits in 16-bits column address.
5. When 4K/page, spare size is 240 bytes. Wrap bit has 3 bits and located at the first 3 bits in 16-bits column address.

5.2.1 Page Read to Cache (13H)

The waveform of Page Read to Cache (13H) is shown as follows:

Figure 5-2. Page Read to Cache (13H) Sequence Diagram



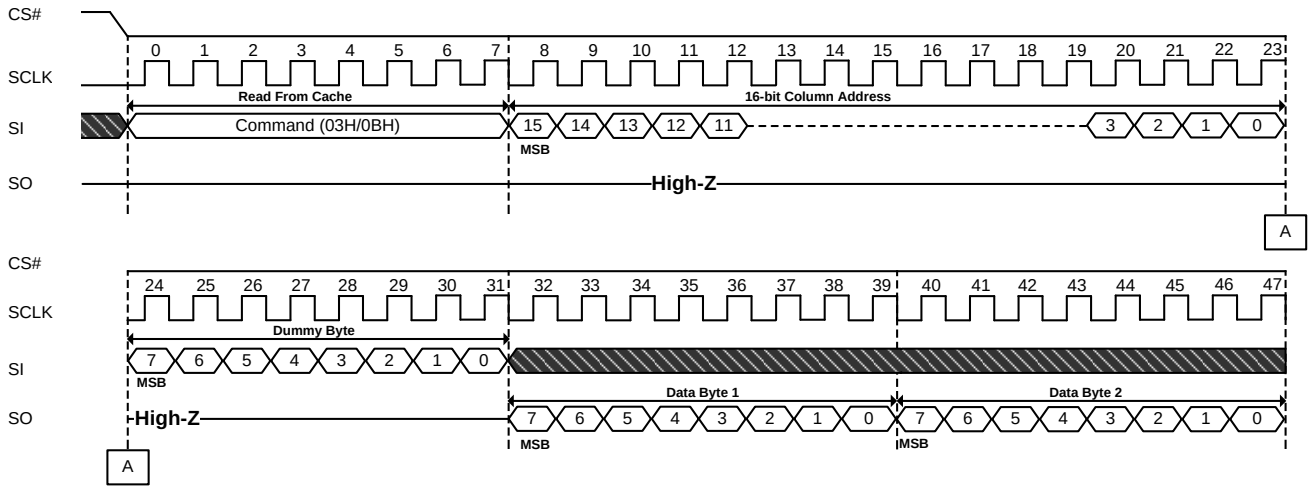
Note:

1. For MKSV512MIL-AE
   Block = 512, 24-bit address consists of 9 dummy bits and 15 page/block address bits.
2. For MKSV1GIW-AE Block = 512, 24-bit address consists of 8 dummy bits and 16 page/block address bits.
3. For MKSV1GIW-BE; MKSV1GIW-DE; MKSV1GIW-FE; MKSV1GIL-AE; MKSV1GIL-DE Block = 1024, 24-bit address consists of 8 dummy bits and 16 page/block address bits.
4. For MKSV2GIB-AE; MKSV2GIW-CE; MKSV2GIW-DE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-BE; MKSV2GIL-DE; MKSV2GIL-GE; MKSV2GIL-HE; MKSV4GIW-AE; MKSV4GIW-DE
   Block = 2048, 24-bit address consists of 7 dummy bits and 17 page/block address bits.

5.3 Read from Cache x1 IO (03H/0BH)

The Read from Cache x1 IO (03H/0BH) consists of an OP code followed by 16-bit column address. The column address is composed of wrap bits and column address bits. Refer the Read from Cache x1 IO sequence diagram as follows:

Figure 5-3. Read from Cache x1 IO (03H/0BH) Sequence Diagram



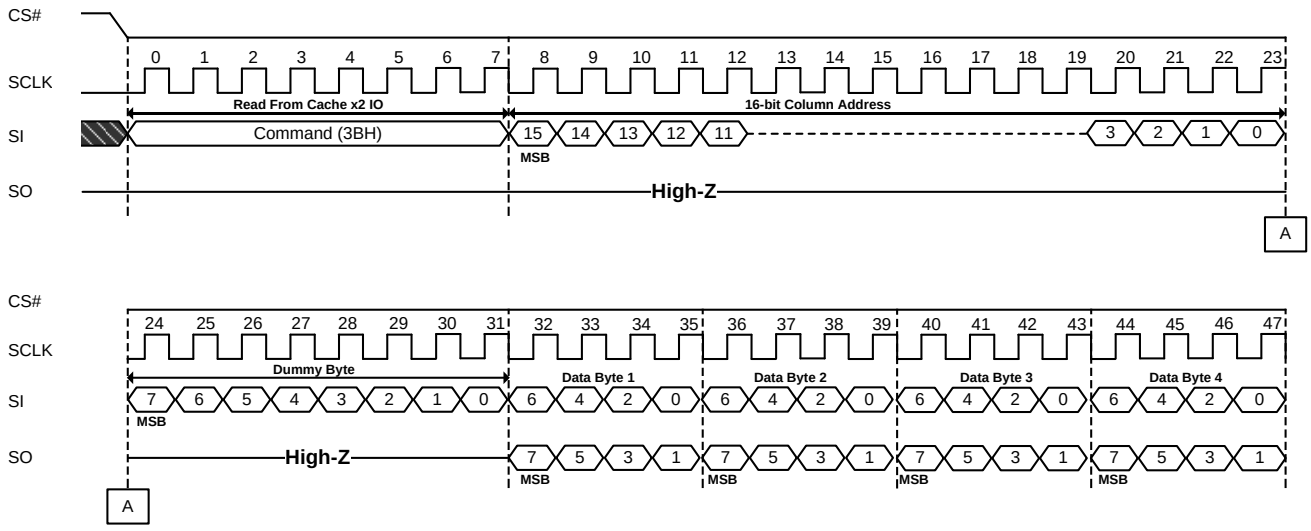
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.

5.4 Read from Cache x2 IO (3BH)

The Read from Cache x2 IO (3BH) command is similar to the Read from Cache x1 IO (03H/0BH) but the command uses two pins to output data. The data output pins include the SI (SIO0) and the SO (SIO1). The Read from Cache x2 IO (3BH) sequence diagram is shown as follows:

Figure 5-4. Read from Cache x2 IO (3BH) Sequence Diagram



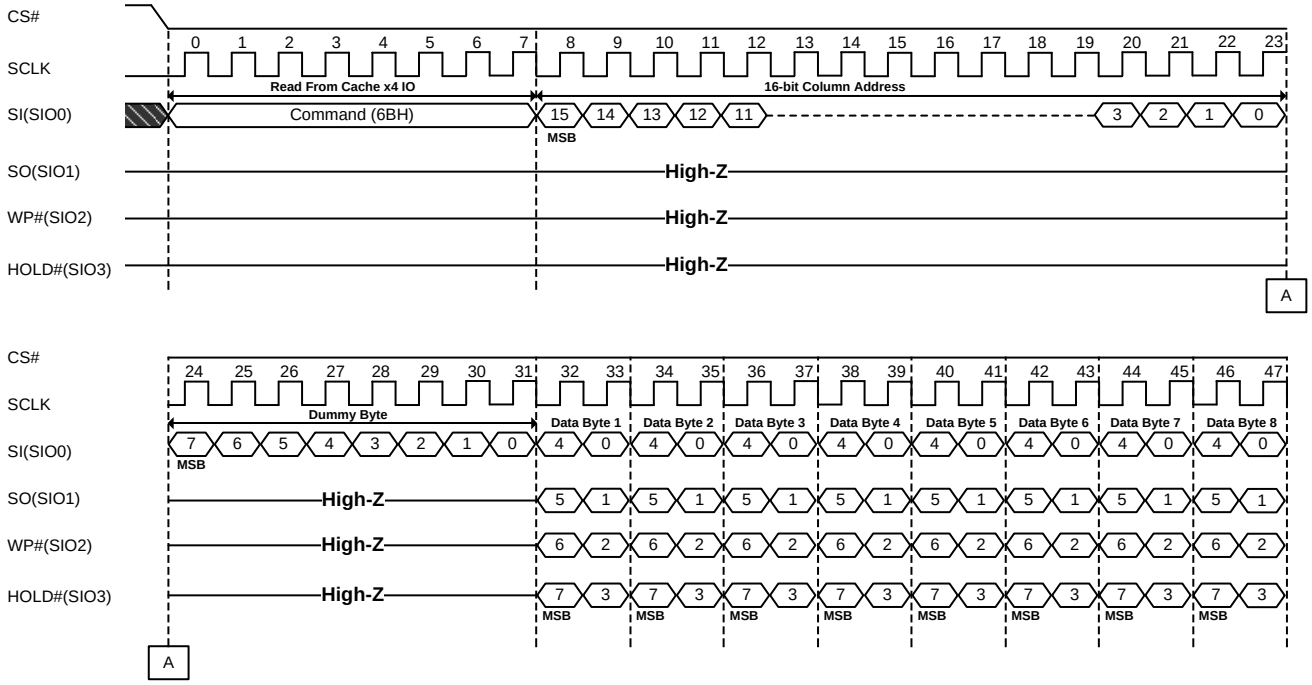
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.

5.5 Read from Cache x4 IO (6BH)

The Read from Cache x4 IO (6BH) command is similar to the Read from Cache x1 IO (03H/0BH) and the Read from Cache x2 IO (3BH) but the command uses four pins to output data. The four pins include the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). The Read from Cache x4 IO (6BH) sequence diagram is shown as follows:

Figure 5-5. Read from Cache x4 IO (6BH) Sequence Diagram



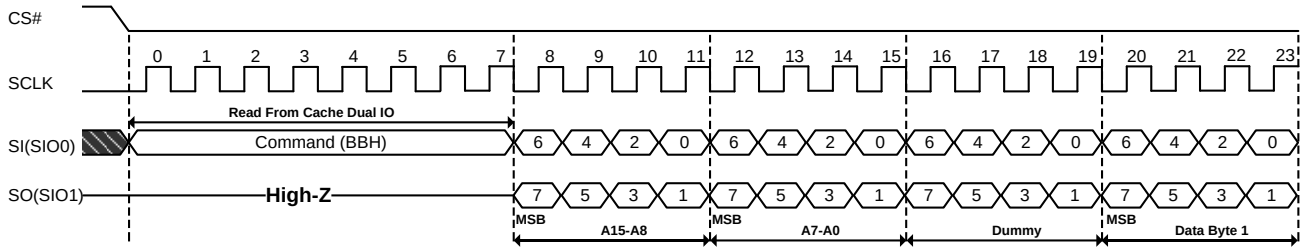
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.

5.6 Read from Cache Dual IO (BBH)

The Read from Cache Dual IO command (BBH) is similar to the Read from Cache x2 IO command (3BH) and uses both of SI (SIO0) and SO (SIO1) as input bin. Each bit in 16-bit column address and the followed dummy byte will be latched in during the falling edge of SCLK, then the cache contents will be shifted out 2-bit in a clock cycle through the SI (SIO0) and the SO (SIO1).

Figure 5-6. Read from Cache Dual IO (BBH) Sequence Diagram



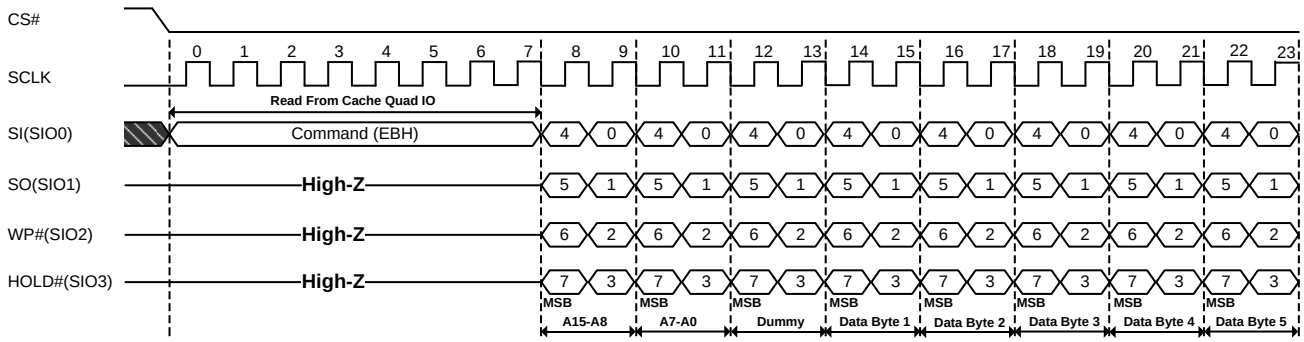
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits (Wrap<3:0>, A11-A0).
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits (Wrap<3:0>, A11-A0).
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits (Wrap<3:0>, A11-A0).
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits (Wrap<2:0>, A12-A0).
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits (Wrap<2:0>, A12-A0).

5.7 Read from Cache Quad IO (EBH)

The Read from Cache Quad IO (EBH) command is similar to the Read from Cache x4 IO (6BH) command and has 4 input pins which are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). Each bit in 16-bit column address and the followed dummy byte will be latched in during the raising edge of SCLK through these four input pins, and then the cache contents will be shifted out 4-bit in a clock cycle through SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3) The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the Read from Cache Quad IO (EBH) command .

Figure 5-7. Read from Cache Quad (EBH) Sequence Diagram



Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits (Wrap<3:0>, A11-A0).
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits (Wrap<3:0>, A11-A0).
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits (Wrap<3:0>, A11-A0).
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits (Wrap<2:0>, A12-A0).
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits (Wrap<2:0>, A12-A0).

6 Program Operations

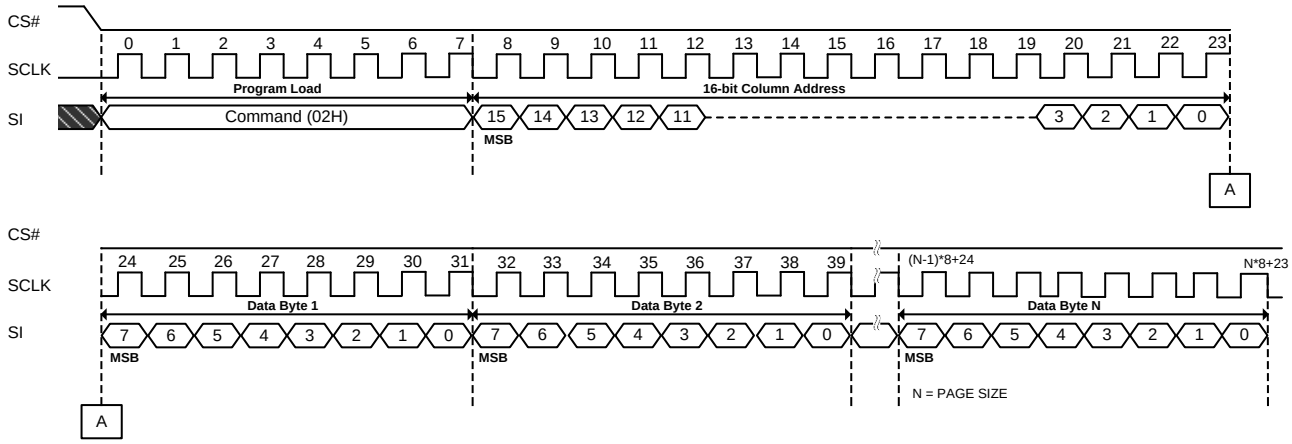
The PAGE PROGRAM sequence transfers the data from the host to NAND flash array through cache memory. The operation sequence programs the first byte to last byte of data within a page. If page size is not enough, those additional bytes will be ignored by the cache memory. The PAGE PROGRAM sequence is as follows:

I. 06H (WRITE ENABLE when WEL bit is 0)
II. PROGRAM LOAD
    - 02H (PROGRAM LOAD) / 32H (PROGRAM LOAD x4)
III. 10H (PROGRAM EXECUTE)
IV. 0FH (GET FEATURE command to read the status)

At first, the WRITE ENABLE (06H) command is used to set the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to issuing a program execute (10h). The PROGRAM LOAD (02H/32H) command is issued then and the PROGRAM LOAD command can only be issued one time in a PAGE PROGRAM sequence. Secondly, the PROGRAM EXECUTE (10H) command is issued to program the data into the page. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE PROGRAM. After finishing the PAGE PROGRAM successfully, the OIP and WEL bit in status register (C0H) will be set to 0.

6.1 Program Load (PL) (02H)

Figure 6-1. Program Load (02H) Sequence Diagram



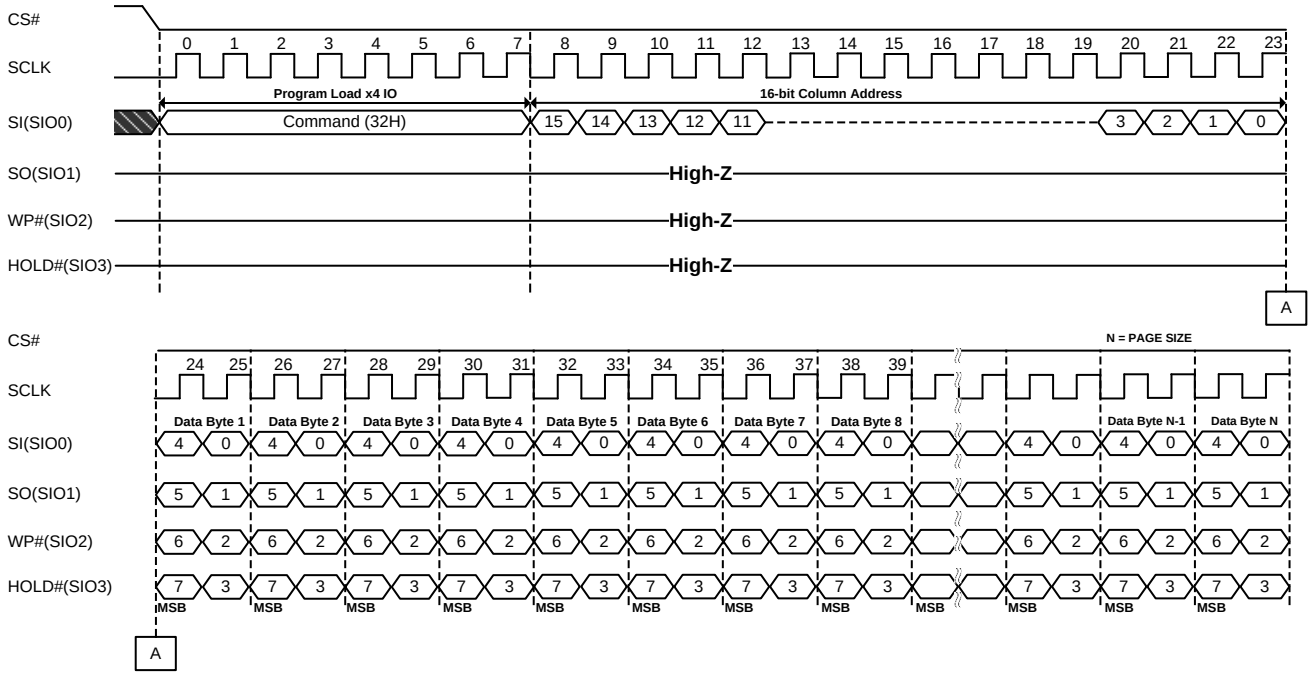
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.

6.2 Program Load x4 IO (PL x4) (32H)

The PROGRAM LOAD x4 IO (32H) command is similar to the PROGRAM LOAD (02H) command and uses four input pins to transfer data in. The four input pins are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the PROGRAM LOAD x4 IO (32H) command. The command sequence is shown as follows:

Figure 6-2. Program Load x4 IO (32H) Sequence Diagram



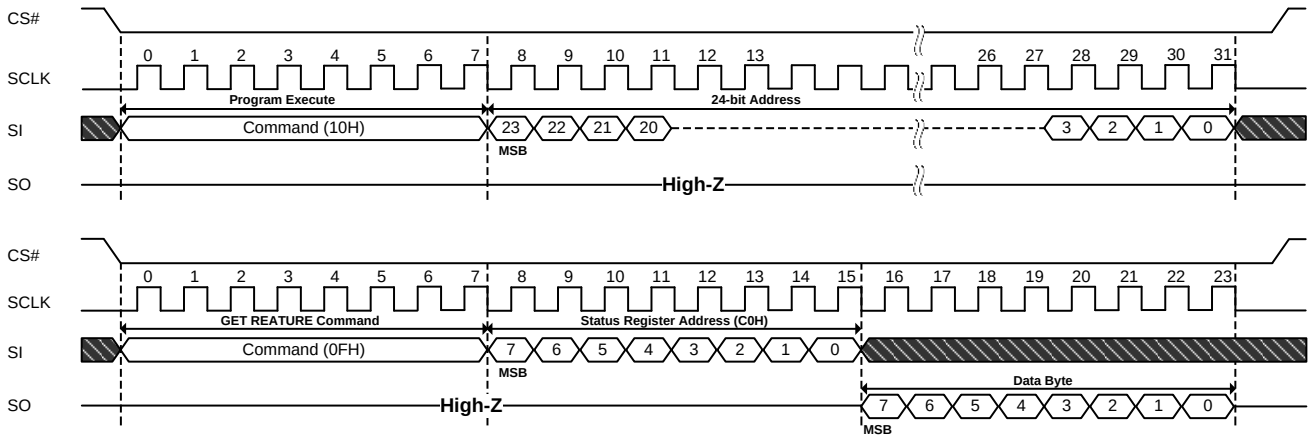
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.

6.3 Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) command must be issued after the data is loaded and the WEL bit is set to HIGH. The PROGRAM EXECUTE (10H) command will transfer data from the cache to the main array. The PROGRAM EXECUTE (10H) consists of an 8-bit Op code, followed by a 24-bit address which including dummy bits and page/block address. This operation needs to wait the busy time. The OIP bit in status register (C0H) will be HIGH until controller finishes the program. The P_FAIL bit in status register (C0H) will be set HIGH if program fail.

Figure 6-3. Program Execute (10H) Sequence Diagram



Note:

1. For MKSV512MIL-AE
   Block = 512, 24-bit address consists of 9 dummy bits and 15 page/block address bits.
2. For MKSV1GIW-AE
   Block = 512, 24-bit address consists of 8 dummy bits and 16 page/block address bits.
3. For MKSV1GIW-BE; MKSV1GIW-DE; MKSV1GIW-FE; MKSV1GIL-AE; MKSV1GIL-DE Block = 1024, 24-bit address consists of 8 dummy bits and 16 page/block address bits.
4. For MKSV2GIB-AE; MKSV2GIW-CE; MKSV2GIW-DE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-BE; MKSV2GIL-DE; MKSV2GIL-GE; MKSV2GIL-HE; MKSV4GIW-AE; MKSV4GIW-DE
   Block = 2048, 24-bit address consists of 7 dummy bits and 17 page/block address bits.

7 Internal Data Move

The Internal Data Move sequence programs or replaces data in a page with existing data. The Internal Data Move operation sequence is as follows:

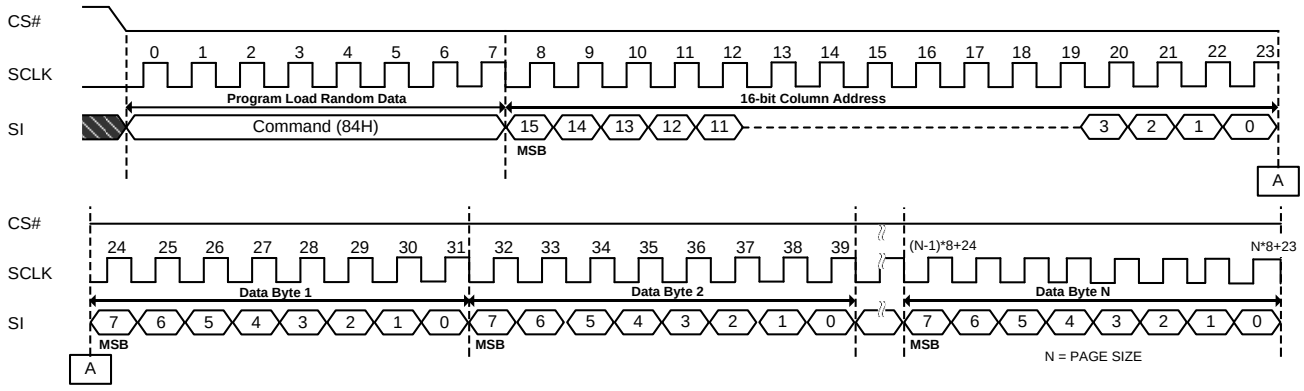
I. 13H (Page Read to cache)
II. 0FH (GET FEATURE command to read the status).
III. Optional 84H/C4H/34H/72H **(PROGRAM LOAD RANDOM DATA. The command of Program load random data can be operated several times in this step.)
IV. 06H (WRITE ENABLE)
V. 10H (PROGRAM EXECUTE)
VI. 0FH (GET FEATURE command to read the status)

- 84H/C4H/34H/72H commands are only available in Internal Data Move operation.

7.1 Program Load Random Data (84H)

Program Load Random Data (84H) command consists of an OP code, followed by 16 bit column address which includes dummy bits and column address bits. This command can only be used in Internal Data Move sequence.

Figure 7-1. Program Load Random Data (84H) Sequence Diagram



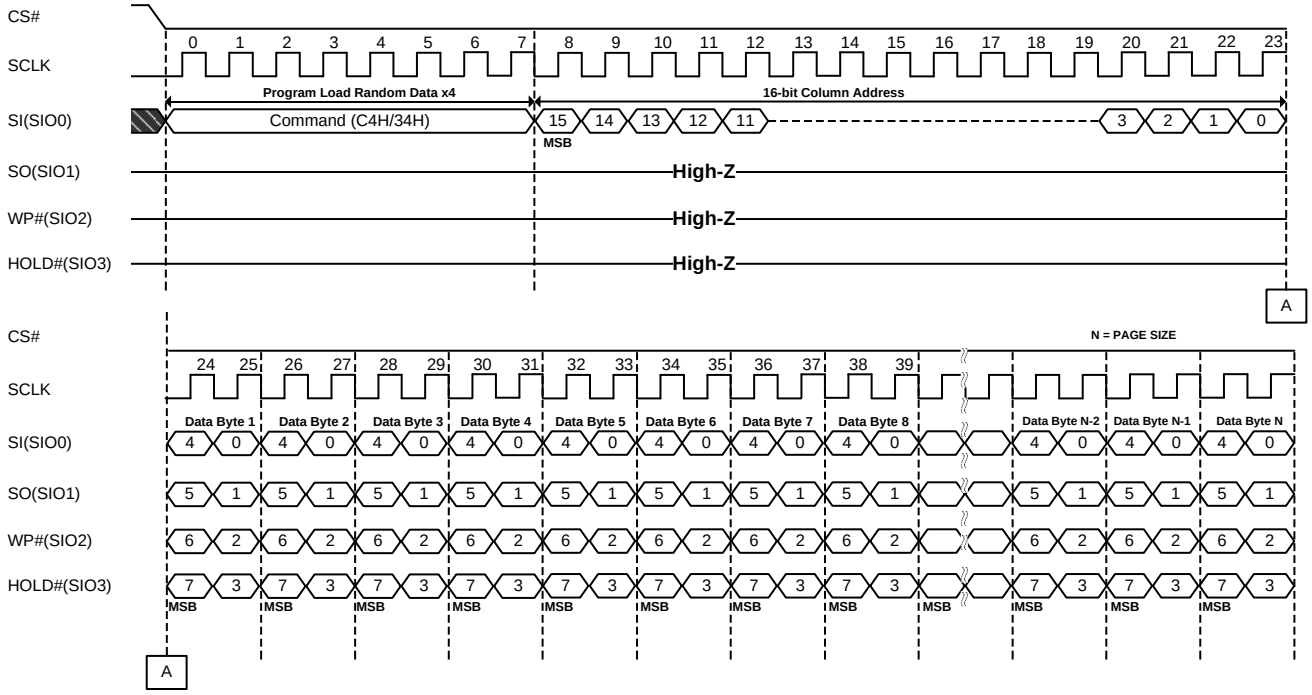
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 wrap bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 wrap bits and 13 column address bits.

7.2 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 (C4H/34H) command is similar to the Program Load Random Data Command (84H) and has four input pins. The four input pins are SI(SIO0), SO(SIO1), WP#(SIO2) and HOLD#(SIO3). The Quad Enable bit needs to be set before the Program Load Random Data x4 command be used. The command is only available during the Internal Data Move sequence.

Figure 7-2. Program Load Random Data x4 (C4H/34H) Sequence Diagram



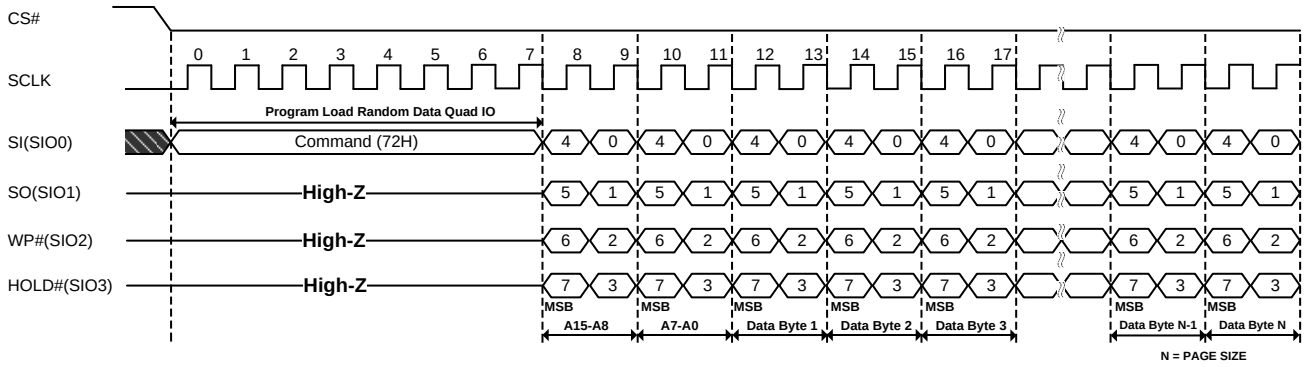
Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 dummy bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 dummy bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 dummy bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 dummy bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 dummy bits and 13 column address bits.

7.3 Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO (72H) is similar to the Program Load Random Data x4 (C4H/34H) command and has 4 input pins: SI(SIO0), SO(SIO1), WP#(SIO2) and HOLD#(SIO3). The Quad Enable (QE) bit in feature register (B0[0]) needs to be set to 1 for the Program Load Random Data Quad IO command. This command is only available during Internal Data Move sequence.

Figure 7-3. Program Load Random Data Quad IO (72H) Sequence Diagram



Note:

1. For MKSV512MIL-AE; MKSV1GIW-AE; MKSV1GIW-DE; MKSV1GIL-AE; MKSV1GIL-DE; MKSV2GIW-DE; MKSV2GIL-BE; MKSV2GIL-GE; MKSV2GIL-HE
   Page size = 2K+ 64 bytes, 16-bit column address consists of 4 dummy bits and 12 column address bits.
2. For MKSV1GIW-BE; MKSV2GIW-CE
   Page size = 2K+ 120 bytes, 16-bit column address consists of 4 dummy bits and 12 column address bits.
3. For MKSV1GIW-FE; MKSV2GIB-AE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-DE;
   Page size = 2K+ 128 bytes, 16-bit column address consists of 4 dummy bits and 12 column address bits.
4. For MKSV4GIW-AE
   Page size = 4K+ 256 bytes, 16-bit column address consists of 3 dummy bits and 13 column address bits.
5. For MKSV4GIW-DE
   Page size = 4K+ 240 bytes, 16-bit column address consists of 3 dummy bits and 13 column address bits.

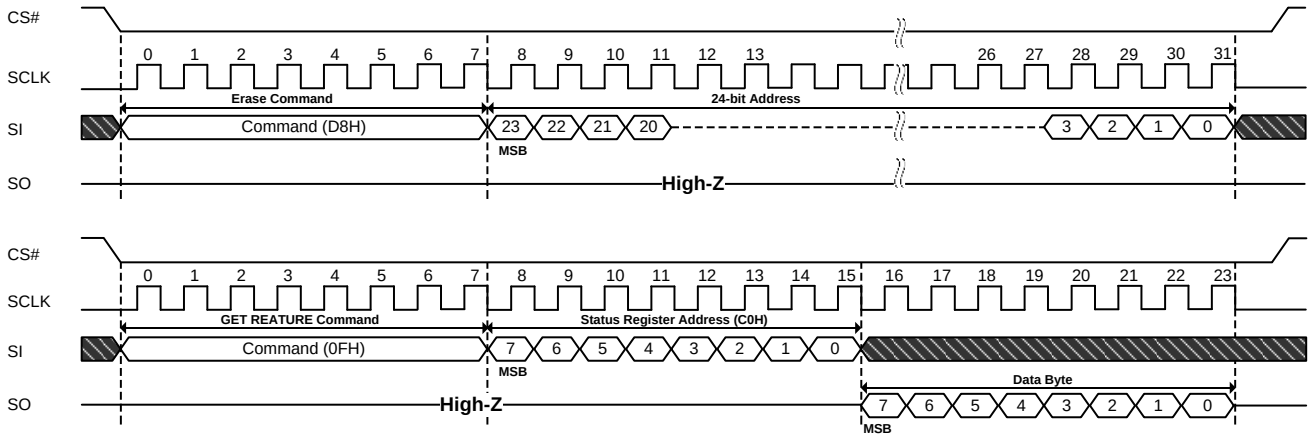
8 Erase Operation- Block Erase (D8H)

The BLOCK ERASE (D8H) command is used to erase at block level. The command sequence for BLOCK ERASE operation is as follows:

I. 06H (WRITE ENABLE command)
II. D8H (BLOCK ERASE command)
III. 0FH (GET FEATURE command to read the status register)

Erase Operation sequence starts from a WRITE ENABLE (06H) command to set WEL bit to 1. After executing the WRITE ENABLE command, BLOCK ERASE (D8H) command can be issued. BLOCK ERASE (D8H) requires a 24-bit address which consists of dummy bits and row address (page address in row address will be ignored automatically). Issue the GET FEATURE (0FH) command to monitor the erase operation after issuing the BLOCK ERASE. The E_FAIL bit in status register can reflect whether the block be erased successfully or not.

Figure 8-1. Block Erase (D8H) Sequence Diagram

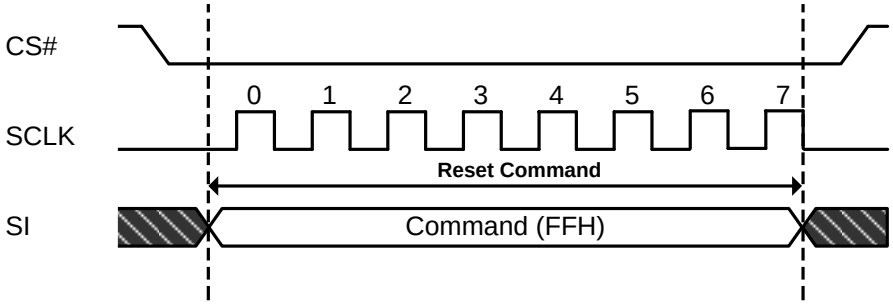


Note:
1. For MKSV512MIL-AE
   Block = 512, 24-bit address consists of 9 dummy bits and 15 page/block address bits.
2. For MKSV1GIW-AE
   Block = 512, 24-bit address consists of 8 dummy bits and 16 page/block address bits.
3. For MKSV1GIW-BE; MKSV1GIW-DE; MKSV1GIW-FE; MKSV1GIL-AE; MKSV1GIL-DE Block = 1024, 24-bit address consists of 8 dummy bits and 16 page/block address bits.
4. For MKSV2GIB-AE; MKSV2GIW-CE; MKSV2GIW-DE; MKSV2GIW-FE; MKSV2GIL-AE; MKSV2GIL-BE; MKSV2GIL-DE; MKSV2GIL-GE; MKSV2GIL-HE; MKSV4GIW-AE; MKSV4GIW-DE
   Block = 2048, 24-bit address consists of 7 dummy bits and 17 page/block address bits.

9 Reset Operation - Reset (FFH)

The RESET (FFH) command stops all operations. For example, the RESET command can stop the previous operation and the pending operations during a cache program or a cache read command.

Figure 9-1. Reset (FFH) Sequence Diagram



10 One-Time Programmable (OTP) Function

The serial device offers a protected, OTP area. 4 full pages are available on the device. Users can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

Table 10-1. OTP State

OTP_PRT	OTP_EN	State
X	0	Normal operation. Cannot access the OTP region.
0	1	Access OTP region. PAGE READ and PAGE PROGRAM are allowed.
1	1	The OTP_PRT has two situations when the device power on, 1. OTP_PRT is 0 when the device power on: User can use SET FEATURE command to set the OTP_PRT and OTP_EN bit to 1, and then issue PROGRAM EXECUTE (10H) to lock OTP region. Once the OTP region was locked, the OTP_PRT will permanently be 1. 2. OTP_PRT is 1 when the device power on: user can only read the OTP region data.

How to access to OTP region:

1. Issue the GET FEATUTE command (0FH).
2. Set Feature bit OTP_EN.
3. Issue the PAGE READ command or PAGE PROGRAM command. The PAGE PROGRAM command can be allowed only when OTP_PRT is 0. The PAGE READ command will automatically be ignored if OTP_PRT is 1.

How to protect OTP region:

Only when the following steps are completed, the OTP_PRT will be set to 1.

1. Issue the SET FEATURE (1FH) command.
2. Set feature bit OTP_EN and OTP_PRT.
3. 06H (WRITE ENABLE)
4. Issue the PROGRAM EXECUTE (10H) command.
5. Issue the GET FEATURE (0FH) command to wait the device goes to ready state from busy.

11 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE commands. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1 and BP2 are set to 1, INV, CMP and BRWD are set to 0. Some block operations relating to the block protection are listed as follows:

- SET FEATURE command must be issued to alter the state of protection feature bit.
- When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set.
- When a PROGRAM/ERASE command is issued to a locked block, status bit OIP in status register (C0H) remains 0. The status register (C0H) will return 08H when a PROGRAM command is issued to program a locked block. The status register (C0H) will return 04H when an ERASE command is issued to erase a locked block.
- When WP# is not LOW, user can issue SET FEATURE command and use the protection register (A0H) and the block protect bits table below to alter the protection rows.

Table 11-1. Block Protection Bits Table

CMP	INV	BP2	BP1	BP0	Protect Rows
X	X	0	0	0	All unlocked
0	0	0	0	1	Upper 1/64 locked
0	0	0	1	0	Upper 1/32 locked
0	0	0	1	1	Upper 1/16 locked
0	0	1	0	0	Upper 1/8 locked
0	0	1	0	1	Upper 1/4 locked
0	0	1	1	0	Upper 1/2 locked
X	X	1	1	1	All locked (Default)
0	1	0	0	1	Lower 1/64 locked
0	1	0	1	0	Lower 1/32 locked
0	1	0	1	1	Lower 1/16 locked
0	1	1	0	0	Lower 1/8 locked
0	1	1	0	1	Lower 1/4 locked
0	1	1	1	0	Lower 1/2 locked
1	0	0	0	1	Lower 63/64 locked
1	0	0	1	0	Lower 31/32 locked
1	0	0	1	1	Lower 15/16 locked
1	0	1	0	0	Lower 7/8 locked
1	0	1	0	1	Lower 3/4 locked
1	0	1	1	0	Block 0
1	1	0	0	1	Upper 63/64 locked
1	1	0	1	0	Upper 31/32 locked
1	1	0	1	1	Upper 15/16 locked
1	1	1	0	0	Upper 7/8 locked
1	1	1	0	1	Upper 3/4 locked
1	1	1	1	0	Block 0

12 Status Register

The content of status register can be read by issuing the GET FEATURE (0FH) command, followed by the status register address C0H. The meaning of each bit in status register is listed as follows:

Table 12-1. Status Register Bit Description

Bit	Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred. It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command.
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred. It will also be set if the user attempts to erase a locked region. This bit is cleared at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates that the current status of the write enable latch(WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
ECCS1, ECCS0	ECC Status	This bit provides ECC status as follows: 00b = No bit errors were detected 01b = bit error was detected and corrected 10b = bit error was detected and not corrected 11b = bit error was detected and corrected, error bit number = ECC max which is according to extended register. ECCS is set to 00b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid operation. After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.

13 Block Management

A NAND Flash device is specified to have a minimum number of valid blocks of the total available blocks per die, which means the devices may have blocks that are invalid when shipped from the factory. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark but the first spare area location in each bad block is guaranteed to contain the bad-block mark. System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device.

Table 13-1. Valid Block Information

Description	512Mb	1Gb	1Gb	2Gb	4Gb
Total available blocks	512	512	1024	2048	2048
Minimum number of valid blocks	502	507	1004	2008	2008
Spare area for bad block mark	All 00h				

14 Power-On Process

When the chip reached the power on level, the internal power on reset signal will be released. The device can response host commands after tPUW (Max 4ms). The host should issue GET FEATURE (0Fh). The device will use the OIP bit in the status register to inform the host that initialization in power-on process is completed. Setting OIP bit to1 indicates that the device is still initializing. Setting the OIP bit to 0 indicates that the power on process is finished. If OIP bit is 1, the host will repeatedly issues GET FEATURE (0Fh) command to monitor the power-on process until the OIP bit is set to 0.

Figure 14-1. Power-On Process

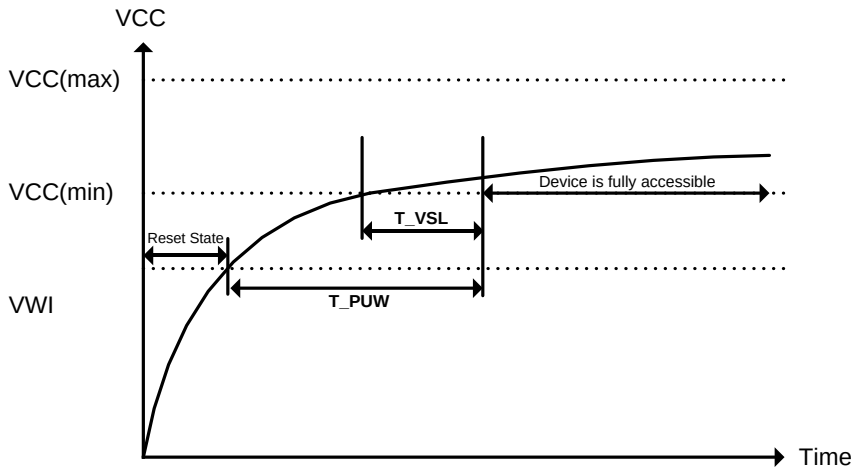


Table 14-1. Power-On Process Parameters

Parameters	Symbol	Min	Typical	Max	Unit
VCC (min) to CS# Low	tVSL	-	-	1	ms
Time Delay Before Read/Write Instruction	tPUW	-	-	4	ms
Write Inhibit Threshold Voltage	vWI	2.5	-	-	V

15 Electrical Characteristics

Table 15-1. 3.3V SPI NAND DC Characteristics

Parameters	Symbol	Min	Typical	Max	Unit
SPI Supply Voltage	VCC	3.0	3.3	3.6	V
VCC standby current	ISB	-	-	120	uA
VCC active current (sequential read)	ICC1	-	-	25	mA
VCC active current (Program)	ICC2	-	-	25	mA
VCC active current (Erase)	ICC3	-	-	30	mA
Input low level	V_IL	-0.3	-	0.2 x VCC	V
Input high level	V_IH	0.8 x VCC	-	VCC + 0.3	V
Output High Voltage	V_OH	VCC - 0.2	-	-	V
Output Low Voltage	V_OL	-	-	0.4	V
Input Leakage Current	I_LI	-	-	+/- 10	uA
Output Leakage Current	I_LO	-	-	+/- 10	uA

Table 15-2. AC Time Characteristics (T_A = -40 ~ 85°C, C_L = 10pF)

Parameters	Symbol	Min	Typical	Max	Unit
Clock Frequency	FC	-	-	80	MHz
Page Program Time	tPROG	-	-	600	us
Clock High Time	tCLH	6.25	-	-	ns
Clock Low Time	tCLL	6.25	-	-	ns
Command deselect Time	tSHSL	30			ns
CS# Setup Time	tSLCH	6.25	-	-	ns
CS# Hold Time	tCHSL	6.25	-	-	ns
Data In Setup Time	tDVCH	2	-	-	ns
Data In Hold Time	tCHDX	2	-	-	ns
Output Hold time	tCLQX	2	-	-	ns
Clock to output Valid	tCLQV	-	-	8.5	ns
CS# High to Output Invalid	tSHQZ	-	-	10	ns
CS# Active Hold time relative to CLK	tCHSH	6.25	-	-	ns
CS# Not Active Setup time relative to CLK	tSHCH	4	-	-	ns

Figure 15-1. Serial Input Timing

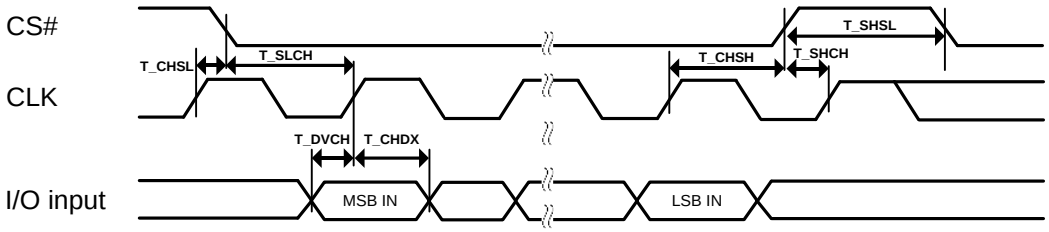
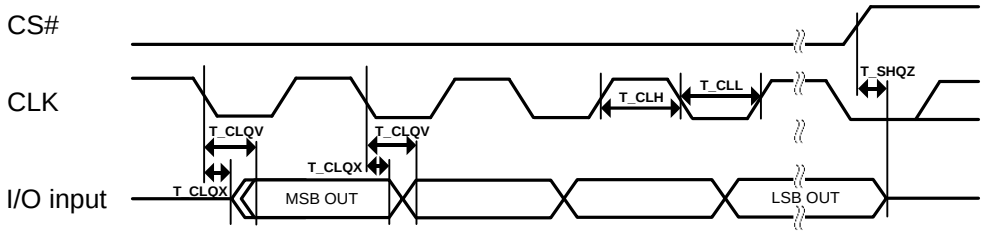


Figure 15-2. Serial Output Timing



16 Package Outline Information

Table 16-1. WSON-8 (8 x 6 x 0.75mm) Dimension Table

Symbol	Dimension (MM)			Dimension (MIL)		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	27.5	29.5	31.5
A1	0.00	0.02	0.05	0.00	0.79	1.97
A3		0.203 REF			8.0 REF	
b	0.35	0.40	0.45	13.8	15.8	17.7
D	7.90	8.00	8.10	311.02	314.96	318.90
D2	3.35	3.40	3.45	132	134	136
E	5.90	6.00	6.10	232.28	236.22	240.16
E2	4.25	4.30	4.35	167	169	171
e		1.27 BSC			50.0 BSC	
L	0.45	0.50	0.55	18	20	22
y	0.00	--	0.08	0.00	--	3.15
k	0.20	--	--	7.8	--	--

Table 16-2. TFBGA 24-ball (6 x 8 x 1.2mm) Dimension Table for ball array 4 x 6

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.010	0.012	0.014	0.25	0.30	0.35
A2	0.026	--	--	0.65	--	--
D	0.232	0.236	0.240	5.90	6.00	6.10
E	0.311	0.315	0.319	7.90	8.00	8.10
D1	--	0.120	--	--	3.00	--
E1	--	0.200	--	--	5.00	--
SD	--	0.02	--	--	0.5	--
SE	--	0.02	--	--	0.5	--
e	--	0.039	--	--	1.00	--
b	0.014	0.016	0.018	0.35	0.40	0.45

Table 16-3. TFBGA 24-ball (6 x 8 x 1.2mm) Dimension Table for ball array 5 x 5-1

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.010	0.012	0.014	0.25	0.30	0.35
A2	0.026	--	--	0.65	--	--
D	0.232	0.236	0.240	5.90	6.00	6.10
E	0.311	0.315	0.319	7.90	8.00	8.10
D1	--	0.157	--	--	4.00	--
E1	--	0.157	--	--	4.00	--
e	--	0.039	--	--	1.00	--
b	0.014	0.016	0.018	0.35	0.40	0.45

Table 16-4. LGA (8 x 6 x 0.8mm) Dimension Table

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.031	--	--	0.800
A2	0.005	0.006	0.007	0.150	0.170	0.190
A3	0.020	0.020	0.021	0.510	0.530	0.540
L	0.015	0.019	0.023	0.400	0.500	0.600
b	0.013	0.015	0.017	0.350	0.400	0.450
e	0.05			1.270		
n	8			8		
D	0.311	0.314	0.318	7.900	8.000	8.100
E	0.232	0.236	0.240	5.900	6.000	6.100
aaa	0.0039			0.100		
bbb	0.0059			0.150		
ccc	0.0039			0.100		
ddd	0.0059			0.150		
eee	0.0031			0.080		

Figure 16-1. Package Outline Drawing Information for WSON-8

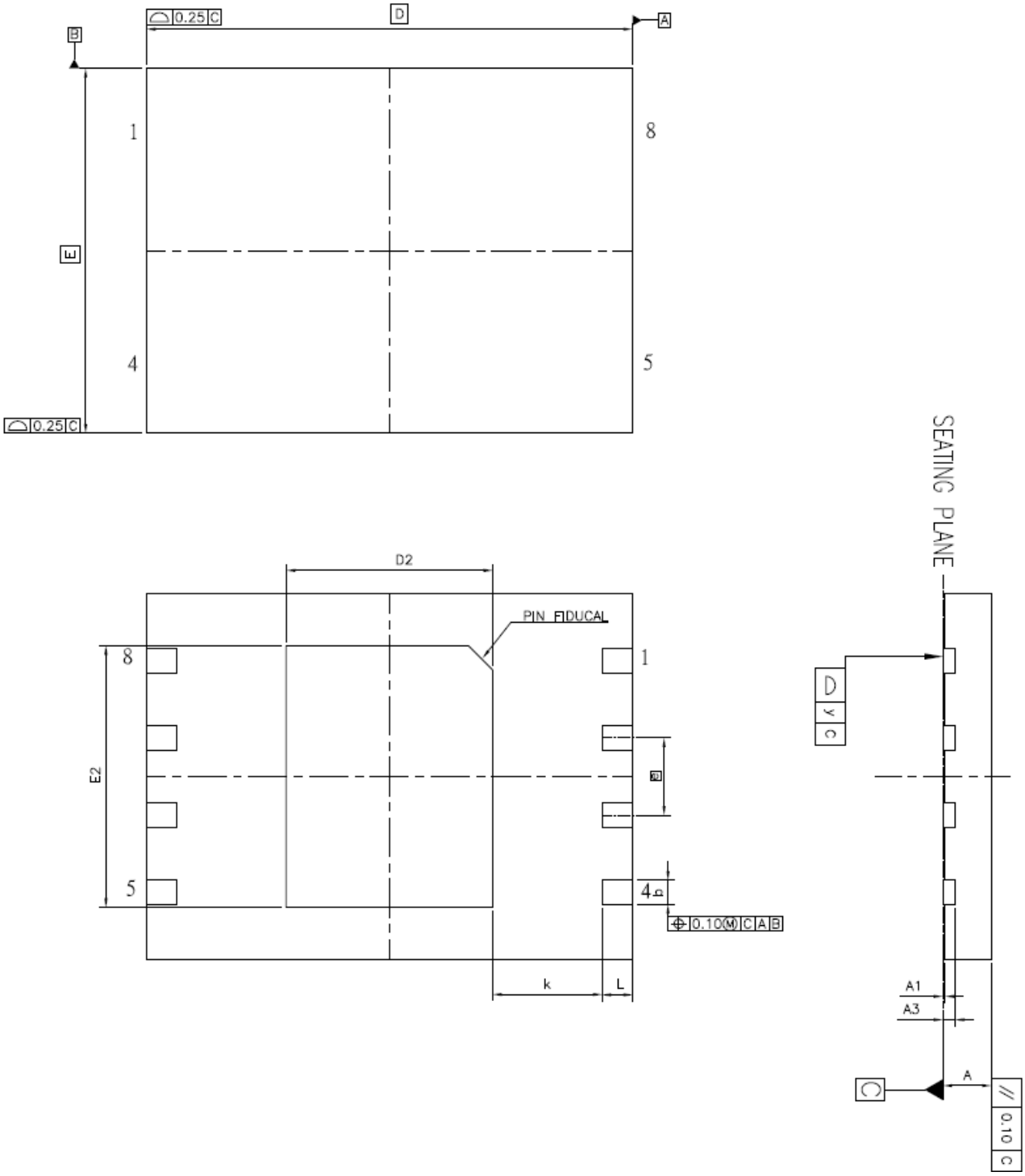


Figure 16-2. Package Outline Drawing Information for 24-ball TFBGA (ball array 4 x 6)

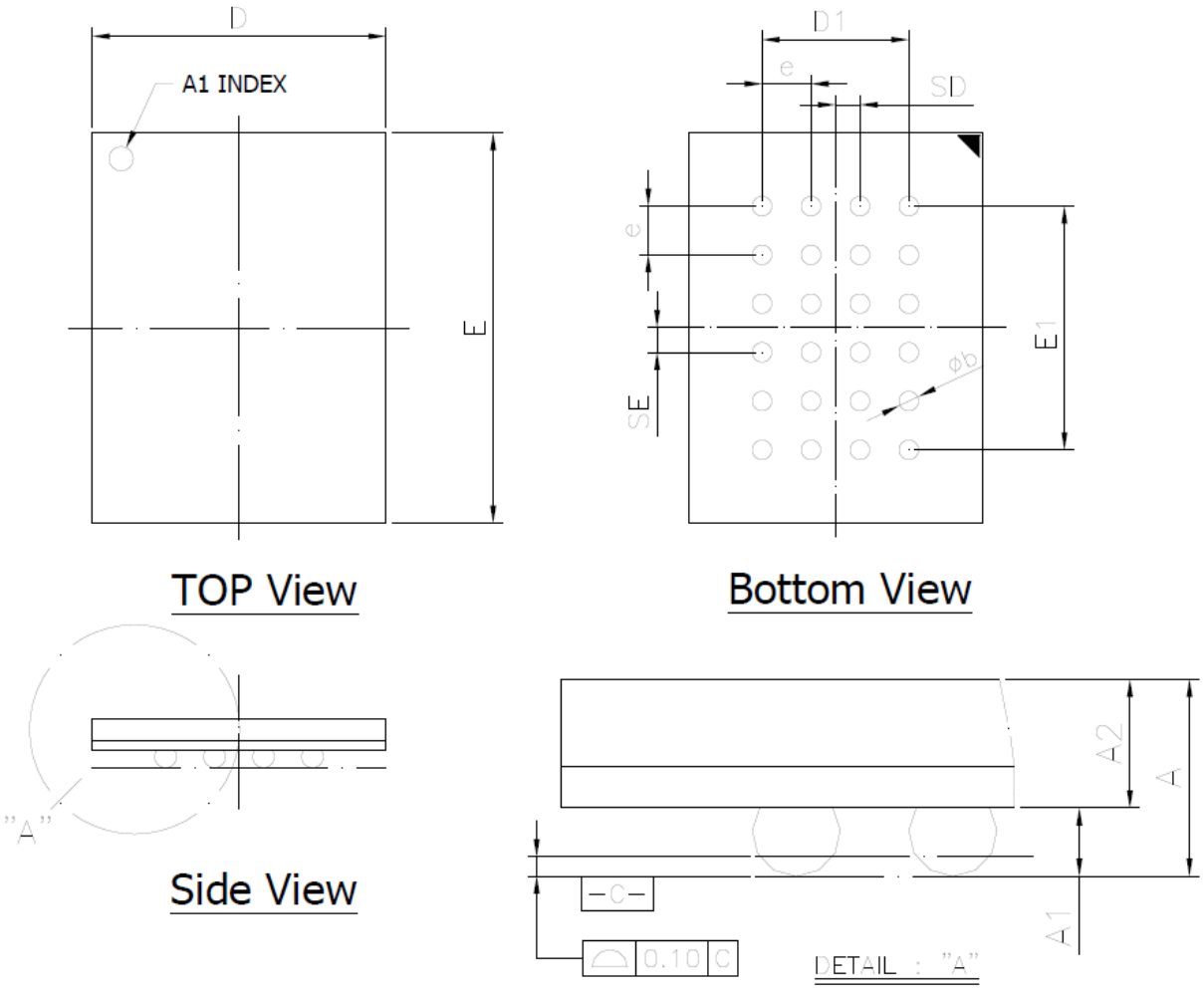


Figure 16-3. Package Outline Drawing Information for 24-ball TFBGA (ball array 5 x 5-1)

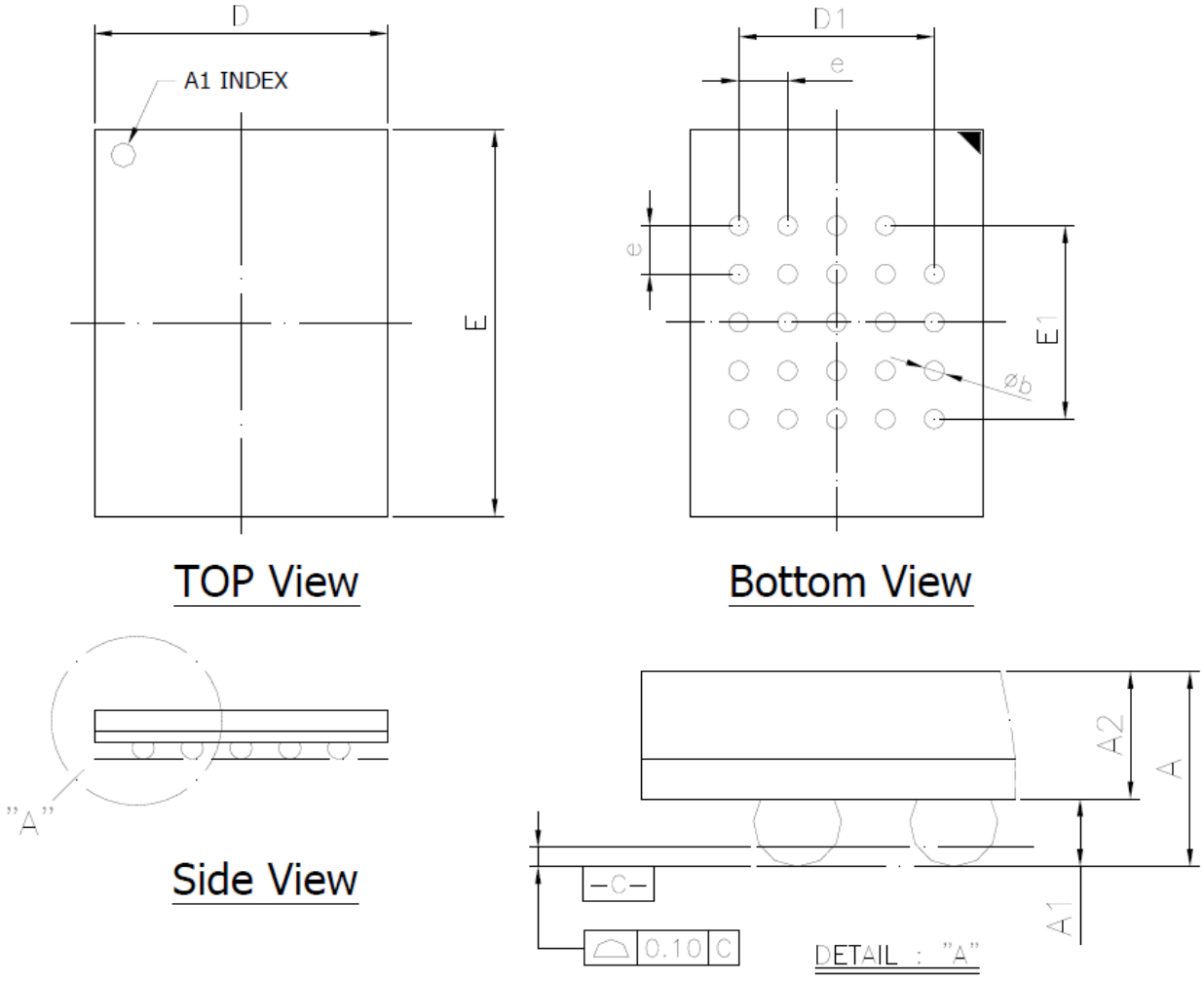


Figure 16-4. Package Outline Drawing Information for LGA