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September 2013

FAN73901 High- and Low-Side, Gate-Drive IC

Features

- Floating Channels for Bootstrap Operation to +600 V
- Typically 2.5 A / 2.5 A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3 V and 5 V Input Logic Compatible
- Output In-Phase with Input

Applications

- Half-Bridge Driver
- HID Lamp Ballast
- SMPS
- Motor Driver

Description

The FAN73901 is a monolithic high- and low-side gatedrive IC, which can drive high-speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to V_S =-9.8 V (typical) for V_{BS} =15 V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop features mak sFAN73901 suitable for switching power supply, motor driver, and high-power DC-DC converter applications.





Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN73901M	8-SOP	-40°C ~ 125°C	Tube
FAN73901MX	0-30F	-40 C ~ 125 C	Tape & Reel

Typical Application Circuit

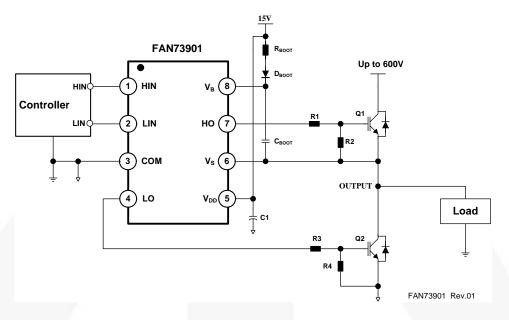


Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

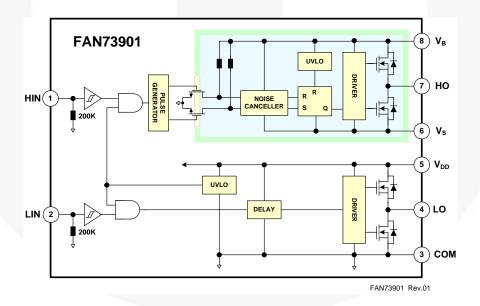
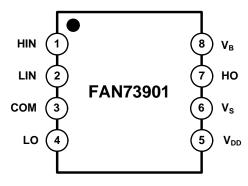


Figure 2. Functional Block Diagram

Pin Configuration



FAN73901 Rev.01

Figure 3. Pin Assignments (Top View)

Pin Definitions

Pin#	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	COM	Low-Side Driver Return
4	LO	Low-Side Driver Output
5	V _{DD}	Low-Side and Logic Part Supply Voltage
6	Vs	High-Voltage Floating Supply Return
7	НО	High-Side Driver Output
8	V _B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}C$, unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V _S	High-Side Floating Supply Offset Voltage	V _B -25	V _B +0.3	V
V _B	High-Side Floating Supply Voltage	-0.3	625.0	V
V _{HO}	High-Side Floating Output Voltage HO	V _S -0.3	V _B +0.3	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
V_{LO}	Low-Side Output Voltage LO	-0.3	V _{DD} +0.3	V
V _{IN}	Logic Input Voltage (HIN and LIN)	-0.3	V _{DD} +0.3	V
dV _S /dt	Allowable Offset Voltage Slew Rate		50	V/ns
P _D	Power Dissipation ⁽¹⁾⁽²⁾⁽³⁾		0.625	W
θ_{JA}	Thermal Resistance, Junction-to-Ambient		200	°C/W
TJ	Junction Temperature		+150	°C
T _{STG}	Storage Temperature		+150	°C

Notes:

- 1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
- 2. Refer to the following standards:
 - JESD51-2: Integral circuits thermal test method environmental conditions natural convection JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
- 3. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V _B	High-Side Floating Supply Voltage	V _S +10	V _S +20	V
V_S	High-Side Floating Supply Offset Voltage	6-V _{DD}	600	V
V _{HO}	High-Side Output Voltage	Vs	V _B	V
V _{DD}	Low-Side and Logic Supply Voltage	10	20	V
V _{LO}	Low-Side Output Voltage	СОМ	V _{DD}	V
V _{IN}	Logic Input Voltage (HIN and LIN)	СОМ	V _{DD}	V
T _A	Operating Ambient Temperature	-40	+125	°C

Electrical Characteristics

 V_{BIAS} (V_{DD} , V_{BS})=15.0 V, V_{S} =COM, T_{A} =25°C, unless otherwise specified. The V_{IL} , V_{IH} , and I_{IN} parameters are referenced to COM and are applicable to the respective input signals HIN and LIN. The V_{O} and I_{O} parameters are referenced to COM and V_{S} is applicable to the respective output signals HO and LO.

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
POWER S	SUPPLY SECTION (V _{DD} AND V _{BS})				•	
V _{DDUV+} V _{BSUV+}	V _{DD} and V _{BS} Supply Under-Voltage Positive-Going Threshold		8.0	8.8	9.8	V
V _{DDUV-} V _{BSUV-}	V _{DD} and V _{BS} Supply Under-Voltage Negative-Going Threshold		7.4	8.3	9.0	V
V _{DDUVH} V _{BSUVH}	V _{DD} and V _{BS} Supply Under-Voltage Lockout Hysteresis Voltage			0.5		V
I _{LK}	Offset Supply Leakage Current	V _B =V _S =600 V			50	μA
I _{QBS}	Quiescent V _{BS} Supply Current	V _{IN} =0V or 5 V		45	80	μA
I_{QDD}	Quiescent V _{DD} Supply Current	V _{IN} =0V or 5 V		75	110	μΑ
I _{PBS}	Operating V _{BS} Supply Current	f _{IN} =20 kHz, rms value		530	640	μΑ
I _{PDD}	Operating V _{DD} Supply Current	f _{IN} =20 kHz, rms value		530	640	μΑ
LOGIC IN	IPUT SECTION (HIN, LIN)			•		
V_{IH}	Logic "1" Input Voltage		2.5			V
V_{IL}	Logic "0" Input Voltage				1.2	V
I _{IN+}	Logic "1" Input Bias Current	V _{IN} =5 V		25	50	μΑ
I _{IN-}	Logic "0" Input Bias Current	V _{IN} =0 V		1.0	2.0	μA
R _{IN}	Input Pull-Down Resistance		100	200		ΚΩ
GATE DR	RIVER OUTPUT SECTION (HO, LO)					
V _{OH}	High-Level Output Voltage, V _{BIAS} -V _O	No Load			1.0	V
V _{OL}	Low-Level Output Voltage, VO	No Load			35	mV
I _{O+}	Output High, Short-Circuit Pulsed Current ⁽⁴⁾	$V_O=0$ V, $V_{IN}=5$ V with PW<10 μ s	1.8	2.5		А
I _{O-}	Output Low, Short-Circuit Pulsed Current ⁽⁴⁾	V_{O} =15 V, V_{IN} =0 V with PW<10 μ s	1.8	2.5		Α
V _S	Allowable Negative V _S Pin Voltage for HIN Signal Propagation to HO		1	-9.8	-7.0	V

Note:

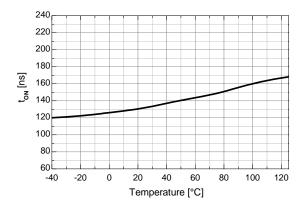
4. This parameter guaranteed by design.

Dynamic Electrical Characteristics

 V_{BIAS} (V_{DD} , V_{BS})=15.0 V, V_{S} =COM=0 V, C_{L} =1000 pF and T_{A} =25°C unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
t _{on}	Turn-on Propagation Delay	V _S =0 V		140	200	ns
t _{off}	Turn-off Propagation Delay	V _S =0 V		140	200	ns
MT	Delay Matching, HS & LS Turn-on/off			0	50	ns
t _r	Turn-on Rise Time			25	50	ns
t _f	Turn-off Fall Time			20	45	ns

Typical Characteristics



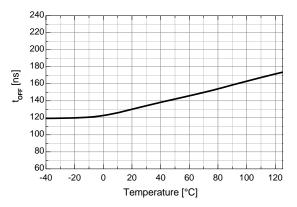
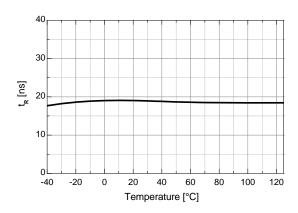


Figure 4. Turn-on Propagation Delay vs. Temperature

Figure 5. Turn-off Propagation Delay vs. Temperature



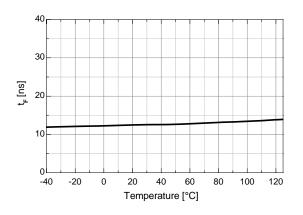
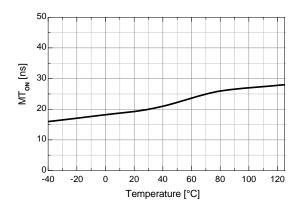


Figure 6. Turn-on Rise Time vs. Temperature

Figure 7. Turn-off Fall Time vs. Temperature



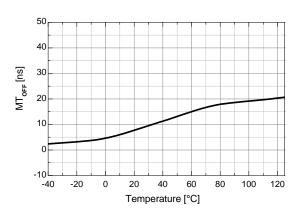
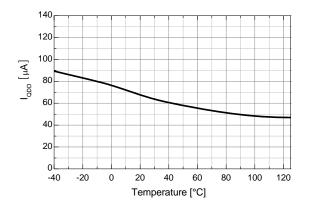


Figure 8. Turn-on Delay Matching vs. Temperature

Figure 9. Turn-off Delay Matching vs. Temperature

Typical Characteristics (Continued)



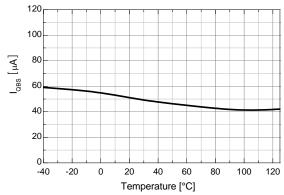
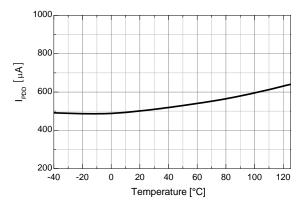


Figure 10. Quiescent V_{DD} Supply Current vs. Temperature

Figure 11. Quiescent V_{BS} Supply Current vs. Temperature



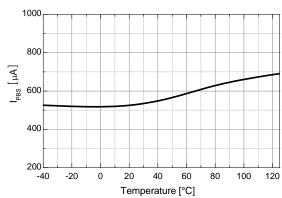
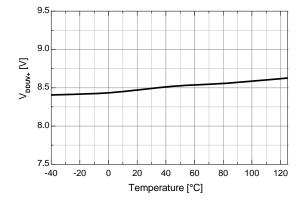


Figure 12. Operating V_{DD} Supply Current vs. Temperature

Figure 13. Operating V_{BS} Supply Current vs. Temperature



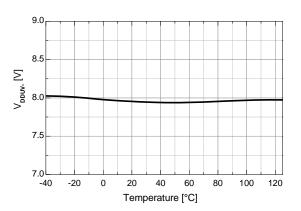
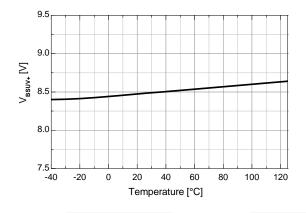


Figure 14. V_{DD} UVLO+ vs. Temperature

Figure 15. V_{DD} UVLO- vs. Temperature

Typical Characteristics (Continued)



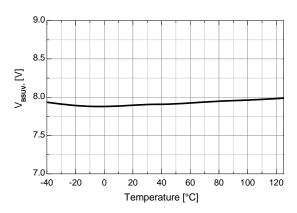
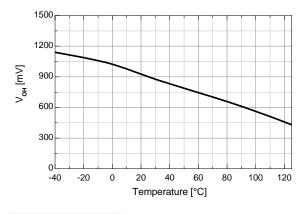


Figure 16. V_{BS} UVLO+ vs. Temperature

Figure 17. V_{BS} UVLO- vs. Temperature



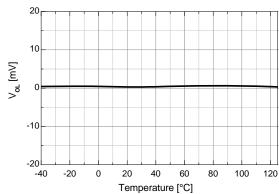
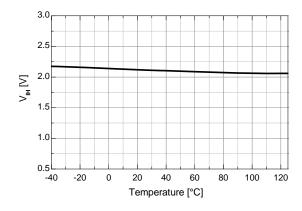


Figure 18. High-Level Output Voltage vs. Temperature

Figure 19. Low-Level Output Voltage vs. Temperature



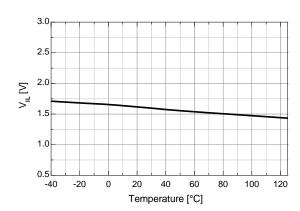
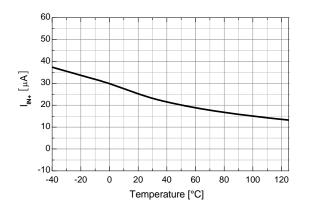


Figure 20. Logic High Input Voltage vs. Temperature

Figure 21. Logic Low Input Voltage vs. Temperature

Typical Characteristics (Continued)



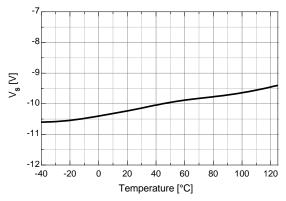


Figure 22. Logic Input High Bias Current vs. Temperature

Figure 23. Allowable Negative V_S Voltage vs. Temperature

Switching Time Definitions

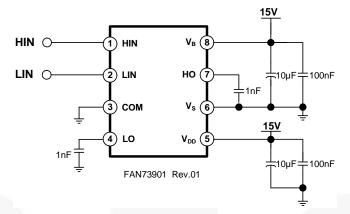


Figure 24. Switching Time Test Circuit

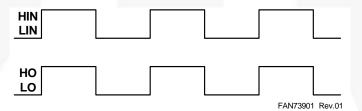


Figure 25. Input / Output Timing Diagram

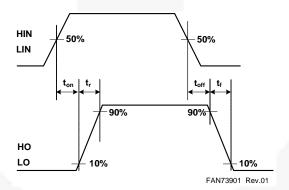


Figure 26. Switching Time Waveform Definitions

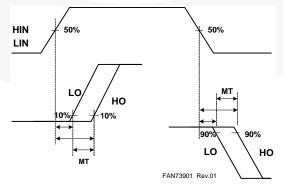


Figure 27. Delay Matching Waveform Definitions

Mechanical Dimensions 1.27 0.65 Α В 1.75 5.60 6.30 4.15 5.70 3 75 **PIN #1 ID** 1.27 \oplus 0.25 M C B A (0.35)LAND PATTERN RECOMMENDATION **TOP VIEW** 1.80 1.35 1.75 1.25 С 0.51 0.31 0.25 (8X) OPTION A - BEVEL EDGE ○ 0.10 C **FRONT VIEW** C 0.25 **OPTION B - NON BEVEL EDGE** NOTES: UNLESS OTHERWISE SPECIFIED BEVEL THIS PACKAGE CONFORMS TO JEDEC MS-012 VARIATION A EXCEPT WHERE NOTED. **GAUGE** R0.10 PLANE B. ALL DIMENSIONS ARE IN MILLIMETERS. 0.25 SEATING OUT OF JEDEC STANDARD VALUE. PLANE D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS. E. LAND PATTERN AS PER IPC SOIC127P600X175-8M 4°-8 F. FILE NAME: MKT-M08B REV1 0.80 0.30 (1.04) DETAIL "B' SCALE 2:1

Figure 28. 8-Lead Small Outline Package (SOP)

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