Adjustable Low Dropout 700mA Linear Regulator

Features

- **Input Voltage Range: 1.42V~3.47V**
- **Low Supply Current: 100μA (Max.)**
- **Low Dropout Voltage: Typically 280mV at 700mA**
- **Adjustable Output Voltage**
- **Output Accuracy: ±1% Over Line, Load, and Temperature Range**
- **Guaranteed 700mA Output Current**
- **Internal Soft start: 0.6ms**
- **Curent Limit and Short Current Limit Protections**
- **Over-Temperature Protection**
- **Open Drain VOUT Voltage Indicator (POK)**
- **Shutdown/Enable Control Function**
- **Stable with MLCC**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APL5701/2 is a P-channel low dropout linear regulator which needs only one input voltage from 1.42V to 3.47V, and delivers current up to 700mA to set output voltage. It also can work with low ESR ceramic capacitors and is ideal for using in the battery-powered applications such as notebook computers and cellular phones. Typical dropout voltage is only 75mV at 700mA loading.

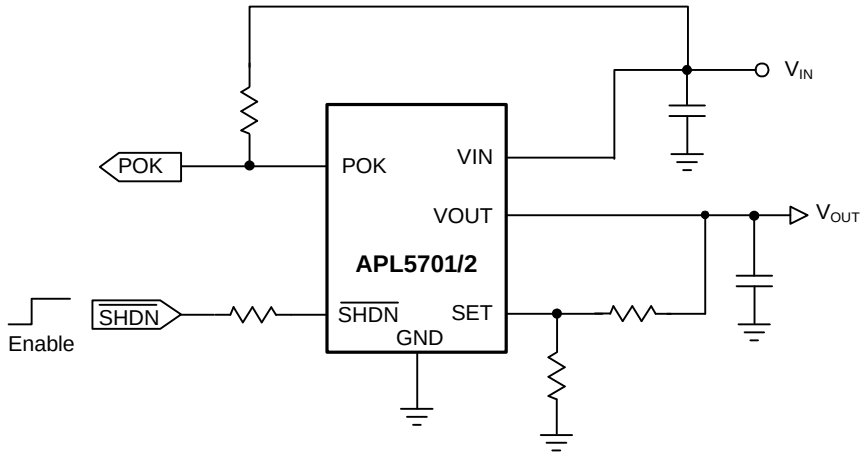
The APL5701/2 integrates many functions. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5701/2 can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V shuts off the output. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads.

The APL5701/2 is available in a SOT-23-5, SOT-23-6, SOP-8P, TDFN3x3-10 and TDFN2x2-8 packages.

Applications

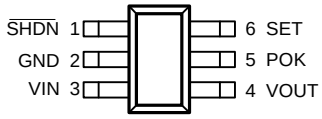
- **Cellular Phones**
- **Portable and Battery-Powered Equipments**
- **Notebook and Personal Computers**

Simplified Application Circuit



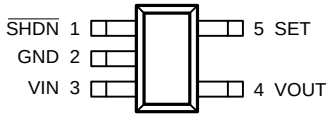
Pin Configuration

APL5701/A



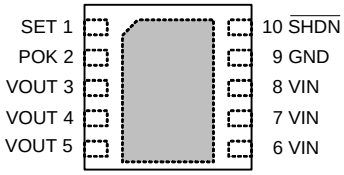
SOT23-6
(Top View)

APL5701/A



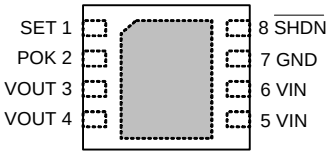
SOT23-5
(Top View)

APL5701/A



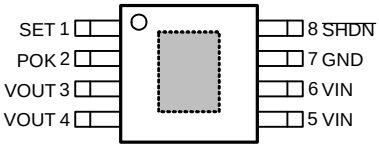
TDFN3X3-10
(Top View)

APL5702/A



TDFN2X2-8
(Top View)

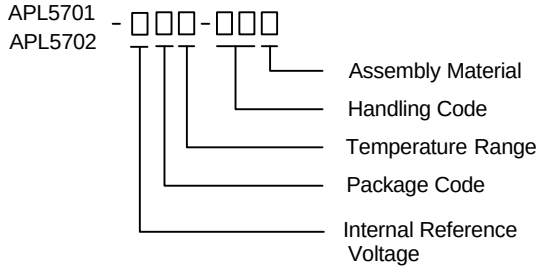
APL5701/A



SOP-8P
(Top View)

= Exposed Pad (connected to ground plane for better heat dissipation)

Ordering and Marking Information



Internal Reference Voltage
Blank : 0.8V A : 0.6V
Package Code
B : SOT-23-5 QB : TDFN 2X2-8 TDFN 3X3-10
C : SOT-23-6 KA : SOP-8P
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
L : Lead Free Device G : Halogen and Lead Free Device

APL5701	QB:	APL 5701 XXXXX XXXXX - Date Code	APL5701A	QB:	APL 5701A XXXXX XXXXX - Date Code
APL5701	B:	701X X - Date Code	APL5701A	B:	01AX X - Date Code
APL5701	KA:	APL5701 XXXXX X - Date Code	APL5701A	KA:	L5701A XXXXX X - Date Code
APL5702	QB:	5702 X X - Date Code	APL5702A	QB:	702A X X - Date Code
APL5701	C:	701X X - Date Code	APL5701A	C:	01AX X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 to 4	V
V_{OUT}	VOUT to GND Voltage	-0.3 to V_{IN}+0.3	V
$V_{/SHDN}$, V_{SET}, V_{POK}	/SHDN, SET, POK to GND Voltage	-0.3 to 4	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	SOT-23-5 Junction-to-Ambient Resistance in free air	240	°C/W
	SOT-23-6 Junction-to-Ambient Resistance in free air	250	
	SOP-8P Junction-to-Ambient Resistance in free air	55	
	TDFN2x2-8 Junction-to-Ambient Resistance in free air	75	
	TDFN3x3-10 Junction-to-Ambient Resistance in free air	55	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter		Range	Unit
V_{IN}	VIN Supply Voltage		1.42 to 3.47	V
V_{OUT}	VOUT Output Voltage	APL5701, APL5702	0.8 ~ V_{IN} – V_{DROP}	V
		APL5701A, APL5702A	0.6 ~ V_{IN} – V_{DROP}	
$V_{/SHDN}$	/SHDN to GND Voltage		0 to 3.47	V
I_{OUT}	VOUT Output Current		0 to 700	mA
R_2	SET to GND Resistance		1 ~ 100	kΩ
C_{IN}	VIN Input Capacitor		1 ~ 100	µF
C_{OUT}	VOUT Output Capacitor		6.8 ~ 33	µF
T_A	Ambient Temperature		-40 to 85	°C
T_J	Junction Temperature		-40 to 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

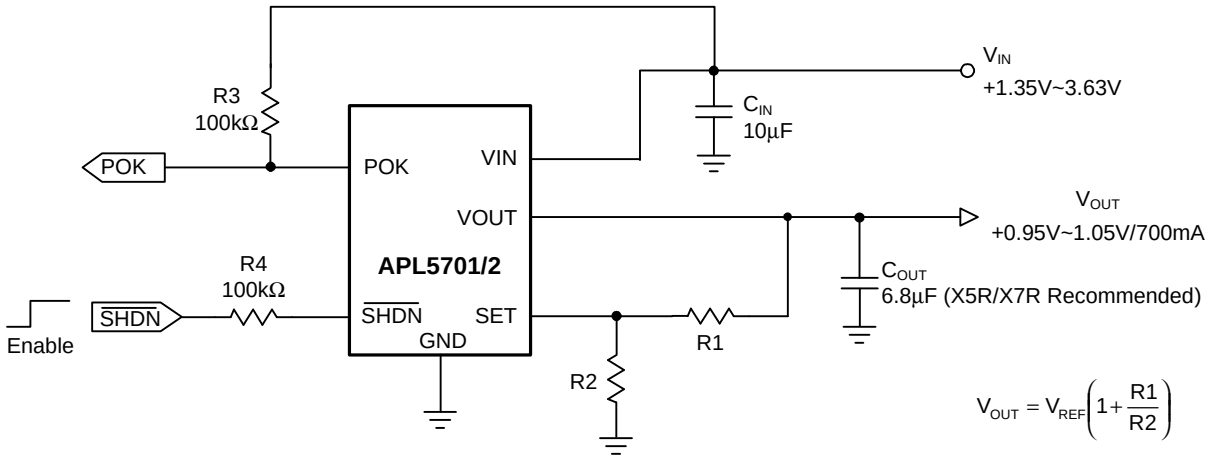
Unless otherwise specified, these specifications apply over V_{IN}=V_{OUT}+0.5V or 1.5V, $V_{/SHDN}$=V_{IN} and T_A= -40°C to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL5701/2			Unit
			Min	Typ	Max	
UNDER-VOLTAGE LOCKOUT (UVLO) AND SUPPLY CURRENT						
	VIN UVLO Threshold Voltage	V_{IN} rising	1.1	1.25	1.4	V
	VIN UVLO Hysteresis		-	50	-	mV
I_{VIN}	VIN Supply Current	No load, $V_{/SHDN}$=3.3V	-	50	100	µA
I_{SD}	VIN Supply Current at Shutdown	No load, $V_{/SHDH}$=0V, V_{IN}=3.63V	-	-	1	µA
OUTPUT VOLTAGE						
V_{REF}	Reference Voltage	APL5701, APL5702	-	0.8	-	V
		APL5701A, APL5702A	-	0.6	-	V
V_{REF}	Reference Voltage Accuracy	I_{OUT}=10mA, T_J=25°C	-0.5	-	+0.5	%
	Line Regulation	I_{OUT}=10mA, V_{IN}=V_{OUT}+0.5V to 3.3V	-0.15	-	+0.15	%/V
	Load Regulation	I_{OUT}=1mA to 700mA	-0.15	0.06	+0.15	%
	Output Accuracy	Over Line, Load, and Temperature Range	-1	-	+1	%
V_{DROP}	Dropout Voltage	V_{IN} =1.5V, I_{OUT} =700mA, T_J= 25°C	-	75	100	mV
		V_{IN} =1.5V, I_{OUT} =700mA, T_J=-40°C to 125°C	-	-	135	mV
PSRR	Power Supply Rejection Ratio	f=10kHz, C_{OUT}=6.8µF, I_{OUT}=700mA,	-	50	-	dB
	VOUT Discharge Resistance	V_{IN}=1.5V, $V_{/SHDN}$=0V, V_{OUT}=0.5V	-	50	-	Ω
	SET Input Current	V_{SET}=0.8V	-100	-	100	nA
POWER OK AND DELAY						
V_{POK}	Rising POK Threshold Voltage	V_{SET} rising	90	92	94	%V_{REF}
	POK Threshold Hysteresis		-	8	-	%V_{REF}
	POK Pull-Low Voltage	POK sinks 5mA	-	0.25	0.4	V
	POK Debounce Interval	V_{SET} < V_{PNOK}	-	10	-	µs
t_{POK}	POK Delay Time	From V_{SET} =V_{POK} to rising edge of the V_{POK}	0.3	0.6	1	ms
/SHDN AND SOFT-START						
$V_{/SHDN}$	/SHDN Logic High Threshold Voltage	$V_{/SHDN}$ rising	0.4	-	1.5	V
	/SHDN Hysteresis		-	0.1	-	V
	/SHDN Pull Low Resistance		-	3	-	MΩ
$t_{D(ON)}$	Turn On Delay Time	From /SHDN high engaged to the beginning of V_{OUT} soft start, T_J=25°C	-	200	300	µs
t_{SS}	Soft-Start Time	V_{OUT} rising 10% to 90%	0.3	0.6	1	ms
PROTECTIONS						
I_{LIMIT}	Current Limit Threshold	T_J=25°C	900	1125	1350	mA
		T_J=-40°C to 125°C	750	-	-	mA
I_{SHORT}	Short-Circuit Output Current	V_{SET} < 50%V_{REF}	-	280	-	mA
$t_{B(SC)}$	Short Current-Limit Blanking Time	From beginning of soft-start	0.6	1.2	-	ms
	Over-Temperature Threshold		-	150	-	°C
	Over-Temperature Hysteresis		-	50	-	°C

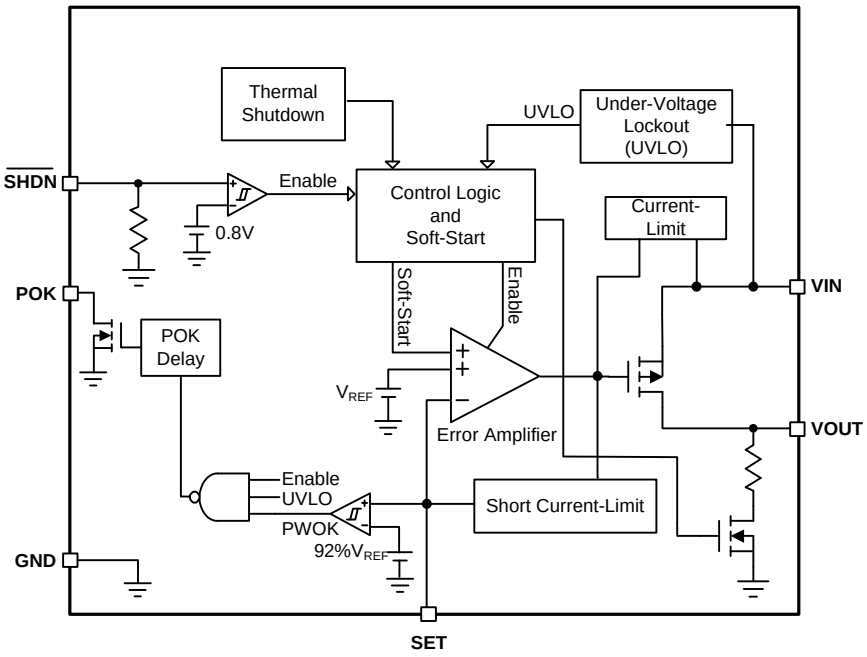
Pin Description

PIN					NAME	FUNCTION
NO.						
SOT-23-6	SOT-23-5	TDFN2x2-8	TDFN3x3-10	SOP-8P		
1	1	10	8	8	$\overline{SHDN}$	Shut Down Control Pin. pulling $V_{/SHDN}$ below 0.3V will disable the output.
2	2	9	7	7	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
3	3	6, 7, 8	5, 6	5, 6	VIN	Main supply input pin for voltage conversions. A decoupling capacitor (10µF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose.
4	4	3, 4, 5	3, 4	3, 4	VOUT	Regulator Output. Sources up to 700mA. Bypass with at least a 6.8µF MLCC capacitor to GND.
5	-	2	2	2	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing SET voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
6	5	1	1	1	SET	Set Output Voltage Pin. Connect this pin to ground for fixed output voltage operation. Connect this pin to an external resistor divider for adjustable output voltage mode operation.
-	-	Exposed Pad	Exposed Pad	Exposed Pad	GND	Ground pin of the circuitry. Connect this pad to system ground plane for good thermal conductivity.

Typical Application Circuit



Block Diagram



Function Description

VIN Under-Voltage Lockout (UVLO)

The APL5701/2 has a built-in under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input.

Soft-Start

The APL5701/2 provides an internal soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. Approximate 200μs delay time after the V_{IN} is over the UVLO threshold; the output voltage starts the soft-start. The typical soft-start interval is about 600μs.

Current Limit Protection

The APL5701/2 provides a current limit protection function. During current limit, the device limits output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Short Circuit Current Limit Protection

When the SET voltage drops below 50%V_{REF}, which is caused by the over load or short circuit, the device limits the output current down to a safe level. The short circuit current limit is used to reduce the power dissipation during short circuit conditions. If the junction temperature is over the over-temperature threshold the device will enter the thermal shutdown. The short current-limit function is disabled for successful start-up during soft-start interval.

Shutdown Control

Pulling the $V_{\overline{SHDN}}$ above 1.5V will enable the LDO output, and pulling $V_{\overline{SHDN}}$ below 0.3V will disable the LDO output. When the LDO output is disabled the supply current is reduced to less than 1μA. $\overline{SHDN}$ pin are internally pulled low by a resistor. If shutdown function is not used, connect $\overline{SHDN}$ to VIN for normal operation. The shutdown input is compatible with both TTL and CMOS logic levels.

Over-Temperature Protection

An over-temperature protection circuitry limits the junction temperature of APL5701/2. When the junction temperature exceeds +150°C, the over-temperature protection circuitry disables the LDO outputs, allowing the device to cool down. The LDO outputs are enabled again after the junction temperature cools down by 50°C, resulting in a pulsed output during continuous thermal overload conditions. Over-temperature protection is designed to protect the IC in the event of over temperature conditions. For reliable operation, the junction temperature cannot exceed T_J=+125°C.

Power-OK and Delay

The APL5701/2 indicates the status of the output voltage by monitoring the feedback voltage (V_{SET}) on SET pin. As the V_{SET} rises and reaches the rising Power-OK voltage threshold, an internal delay function starts to work. At the end of the delay time, the IC turns of the internal NMOS of the POK to indicate the output is ok. As the V_{SET} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK.

Application Information

Output Capacitor

The APL5701/2 requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon ESR (equivalent series resistance) and capacitance of the output capacitor over the operating temperature.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as output capacitors.

During load transients, the output capacitors, depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the APL5701/2 and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

Input Capacitor

The APL5701/2 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance. Ultra-low-ESR capacitors (such as ceramic chip capaci- tors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an input capacitor of VIN. For most applications, the recommended input capacitance of VIN is 10μF.

However, if the drop of the input voltage is not cared, the input capacitance can be less than 10μF. More capacitance reduces the variations of the supply voltage on VIN pin.

Setting Output Voltage

The output voltage is programmed by the resistor divider connected to SET pin. The preset output voltage is calculated by the following equation :

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) \quad \text{..... (V)}$$

Where R1 is the resistor connected from VOUT to SET with Kelvin sensing connection and R2 is the resistor connected from SET to GND.

Layout Consideration

1. Please solder the Exposed Pad on the ground pad on the top-layer of PCBs. The ground pad must have wide size to conduct heat into the ambient air through the ground plane and PCB as a heat sink.
2. Please place the input capacitors for VIN pins near the pin as close as possible for decoupling high-frequency ripples.
3. Ceramic decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
4. To place APL5701/2 and output capacitors near the load reduces parasitic resistance and inductance for excellent load transient response.
5. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
6. Large current paths, shown by bold lines on the figure 1, must have wide tracks.
7. Place the R1 and R2 near the APL5701/2 as close as possible to avoid noise coupling.
8. Connect the ground of the R2 to the GND pin by using a dedicated track.
9. Connect the one pin of the R1 to the load for Kelvin sensing.

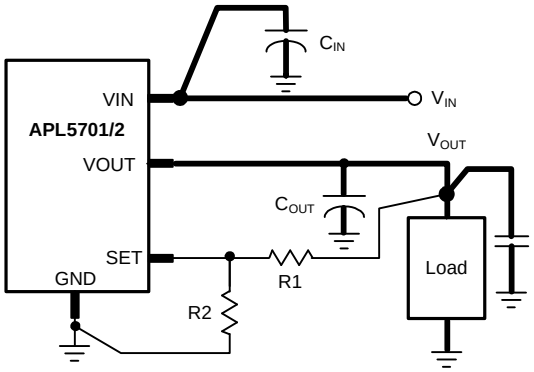
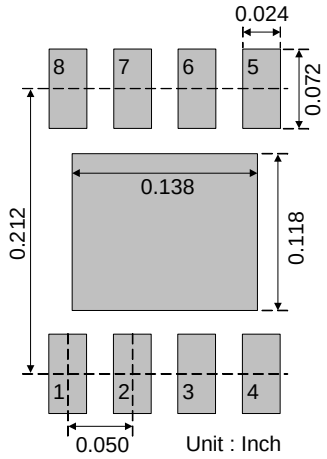
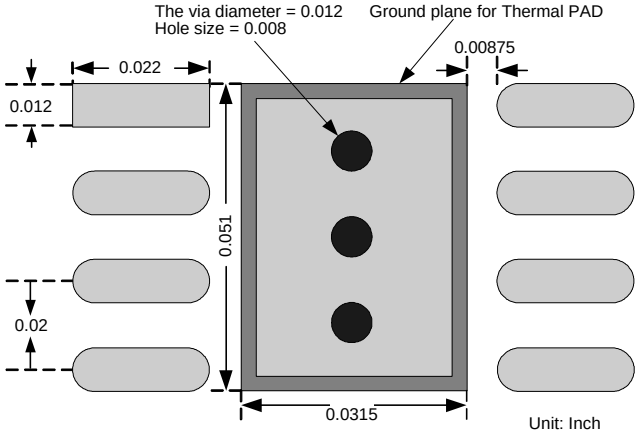


Figure 1

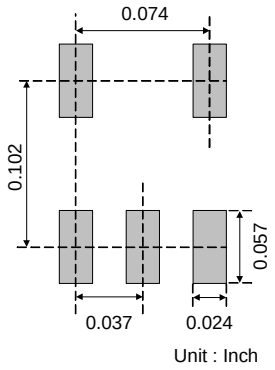
Recommended Minimum Footprint



SOP-8P

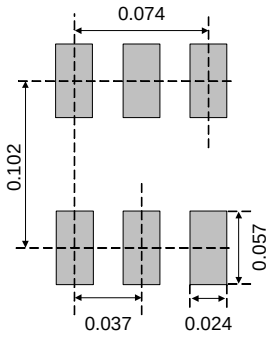


TDFN2x2-8



SOT-23-5

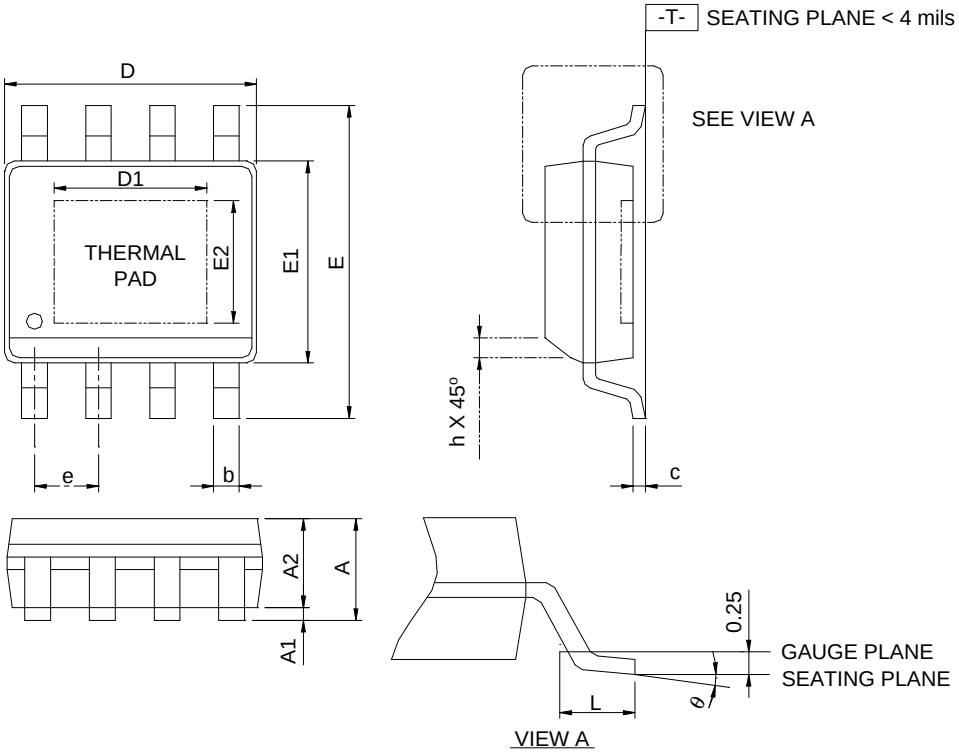
Layout Consideration



SOT-23-6

Package Information

SOP-8P

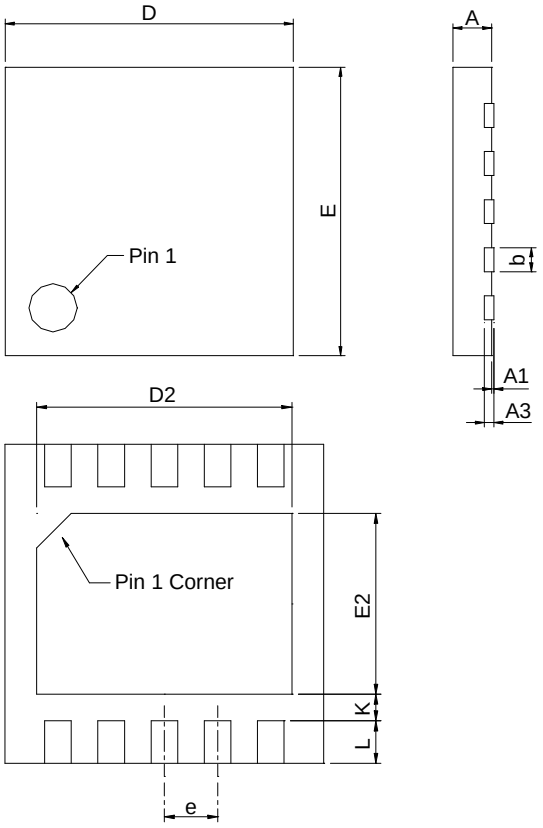


SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

TDFN3x3-10

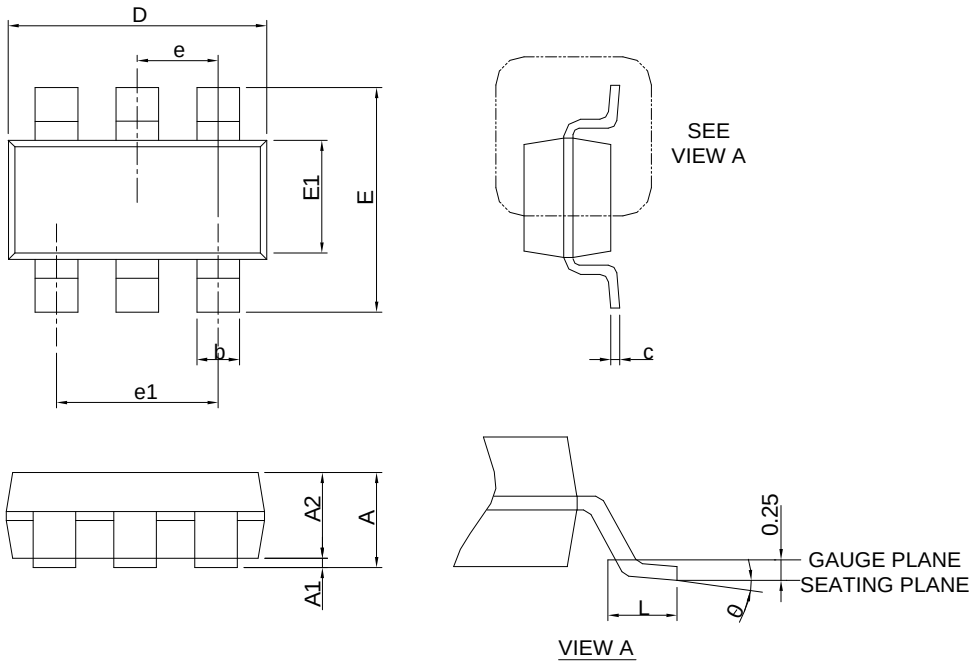


SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Package Information

SOT-23-6

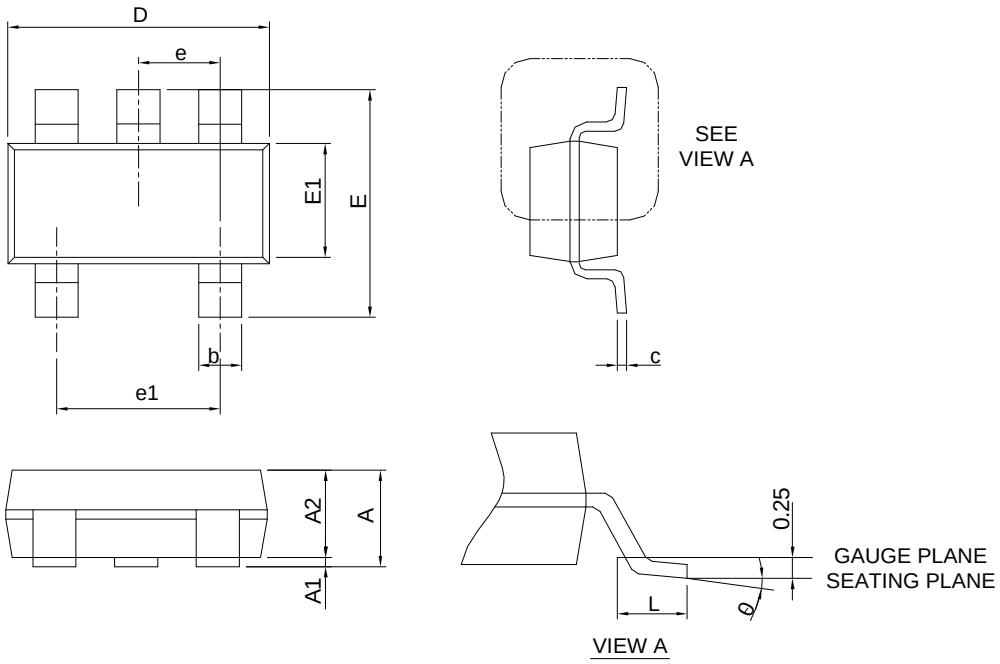


SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOT-23-5

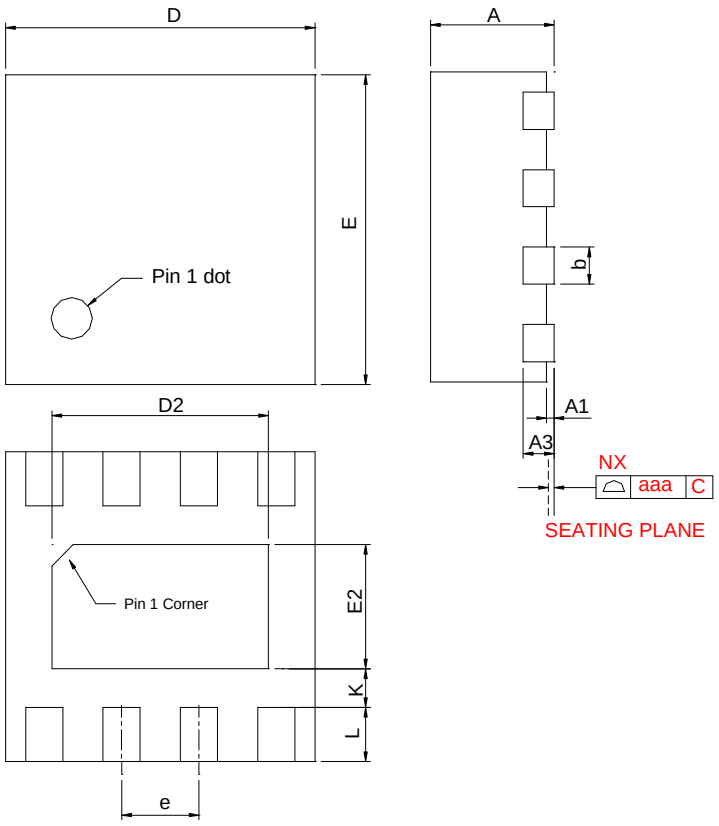


SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

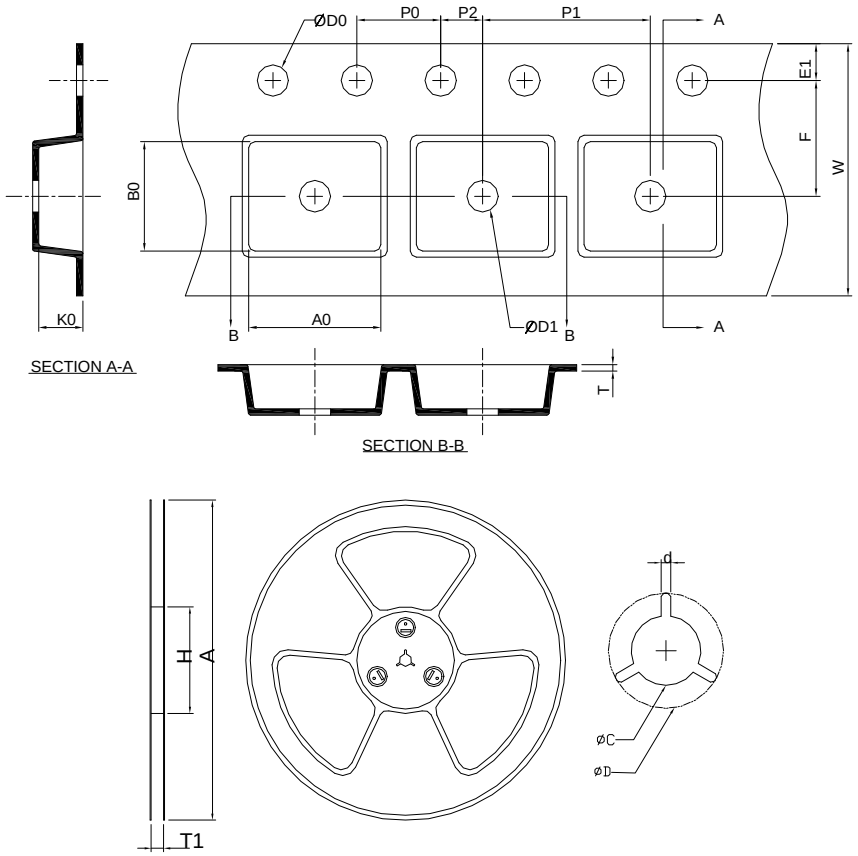
TDFN2x2-8



SYMBOL	TDFN2*2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Follow from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	2.35±0.20	2.35±0.20	1.00±0.20

(mm)

Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

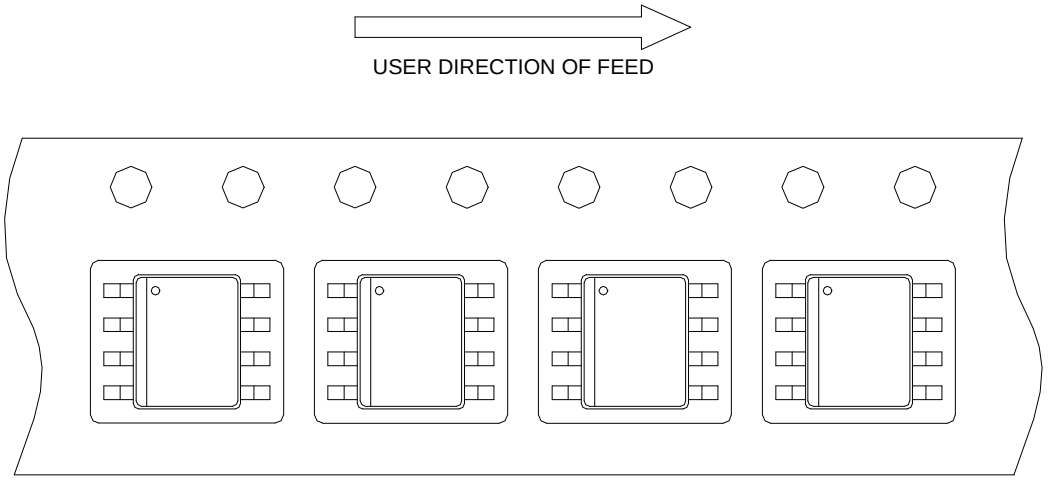
(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP- 8P	Tape & Reel	2500
TDFN-3x3-10	Tape & Reel	3000
TDFN2x2-8	Tape & Reel	3000
SOT-23-5	Tape & Reel	3000
SOT-23-6	Tape & Reel	3000

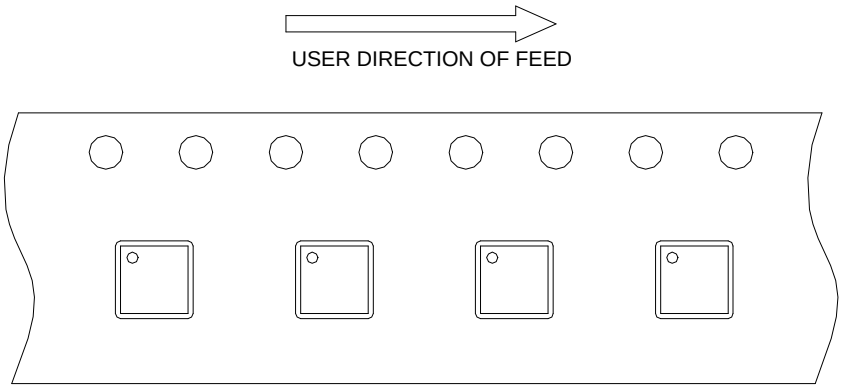
Taping Direction Information

SOP-8P

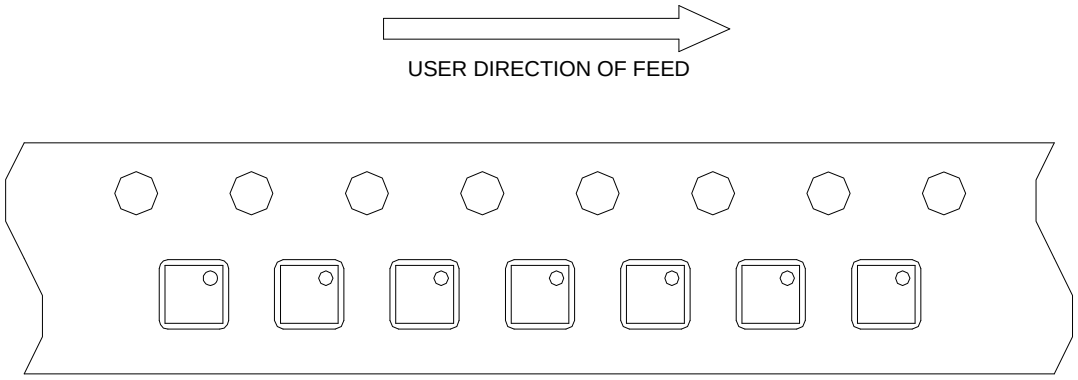


Taping Direction Information

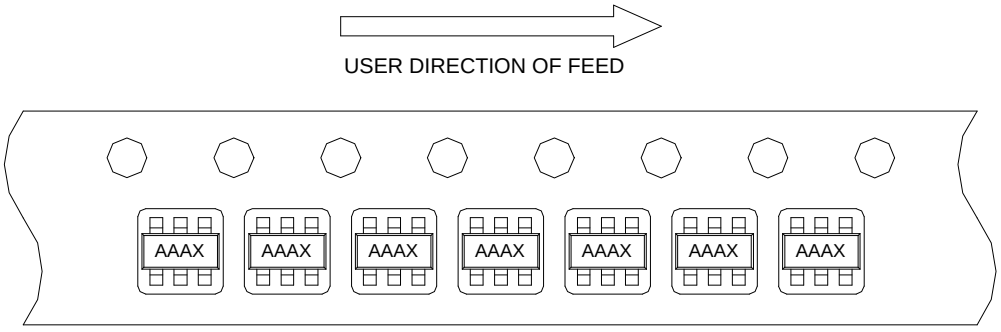
TDFN3x3-10



TDFN2x2-8

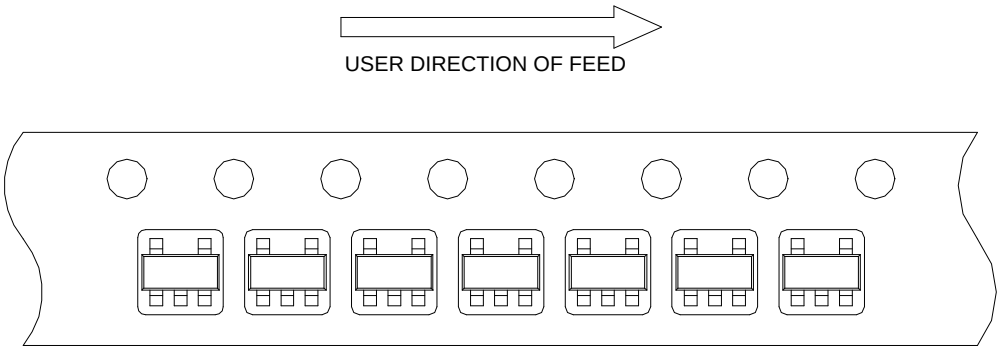


SOT-23-6

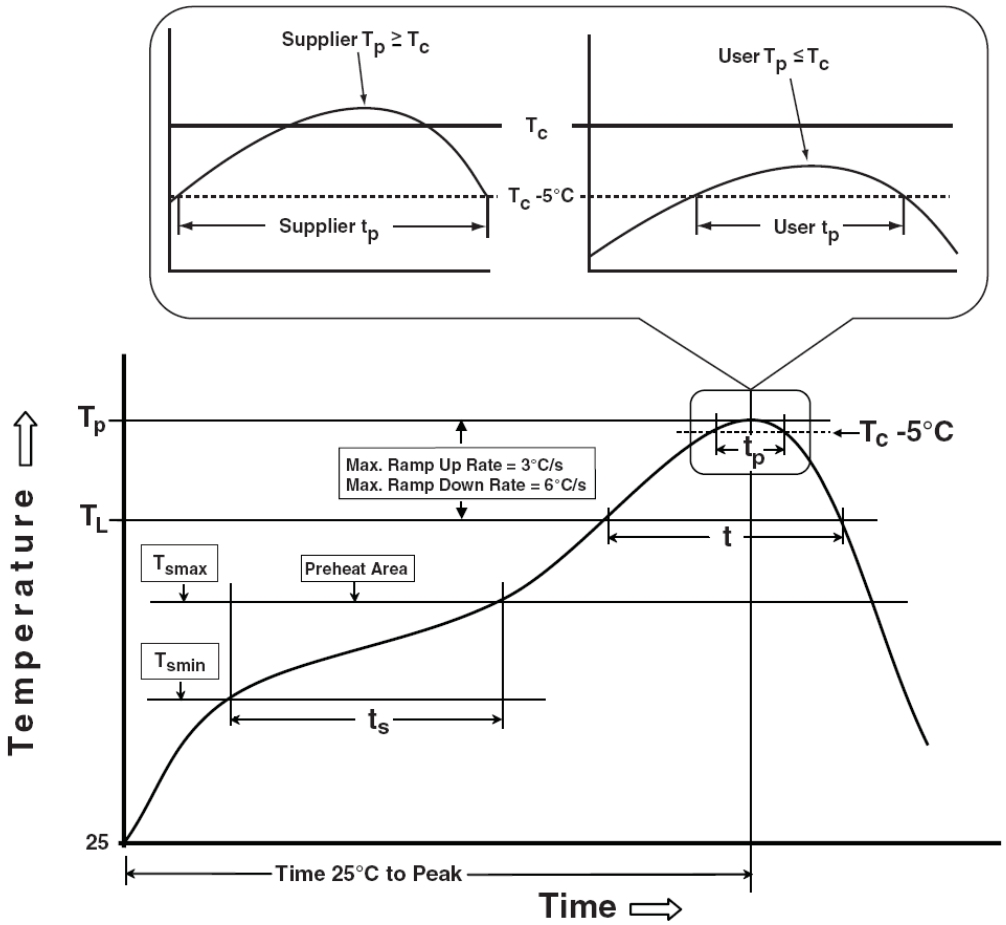


Taping Direction Information

SOT-23-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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