CDCLVP111 Low-Voltage 1:10 LVPECL With Selectable Input Clock Driver

1 Features

- Distributes One Differential Clock Input Pair LVPECL to 10 Differential LVPECL
- Fully Compatible With LVECL and LVPECL
- Supports a Wide Supply Voltage Range from 2.375 V to 3.8 V
- Selectable Clock Input Through CLK_SEL
- Low-Output Skew (Typical 15 ps) for Clock-Distribution Applications
  - Additive Jitter Less Than 1 ps
  - Propagation Delay Less Than 350 ps
  - Open Input Default State
  - LVDS, CML, SSTL Input Compatible
- V_{BB} Reference Voltage Output for Single-Ended Clocking
- Available in a 32-Pin LQFP and QFN Package
- Frequency Range From DC to 3.5 GHz
- Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111

2 Applications

- Designed for Driving 50-Ω Transmission Lines
- High Performance Clock Distribution

3 Description

The CDCLVP111 clock driver distributes one differential clock pair of LVPECL input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP111 can accept two clock sources into an input multiplexer. The CDCLVP111 is specifically designed for driving 50-Ω transmission lines. When an output pin is not used, leaving it open is recommended to reduce power consumption. If only one of the output pins from a differential pair is used, the other output pin must be identically terminated to 50 Ω.

The V_{BB} reference voltage output is used if single-ended input operation is required. In this case, the V_{BB} pin should be connected to $\overline{CLK0}$ and bypassed to GND through a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

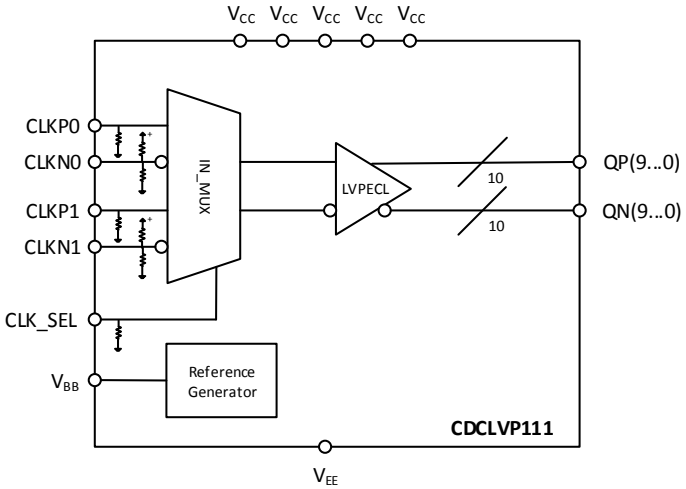
The CDCLVP111 device is characterized for operation from –40°C to 85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCLVP111	VQFN (32)	5.00 mm × 5.00 mm
	LQFP (32)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (July 2011) to Revision F — **Page**

- Added *Device Information* Table, *Pin Configuration and Functions*; *Specifications*; *Applications and Implementation*; *Detailed Description*; *Layout*;*Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* 1
- Added extended frequency range from 1GHz down to 100MHz 8

Changes from Revision D (March 2010) to Revision E — **Page**

- Changed the PowerPAD Pin Function Description 4

Changes from Revision C (November 2009) to Revision D — **Page**

- Deleted duplicate information covering the PowerPAD from Note 1 of the Pin Functions table. 4
- Changed the PowerPAD description in the PIN FUNCTIONS table to include the LQFP package information. 5
- Added "NOTE" at the beginning of "Applications and Implementation" section. 13
- Changed JEDEC symbol to $R_{\theta JA}$ 19

Changes from Revision B (April 2009) to Revision C — **Page**

- Changed PowerPAD information to the Pinout Package 4
- Added PowerPAD information to the Pin Functions table 4

Changes from Revision A (March 2009) to Revision B — **Page**

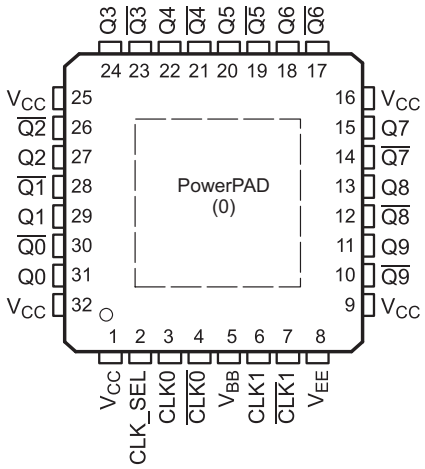
- Added LVTTL/LVCMOS functionality compatible. 4
- Changed recommended resistor values in 16

Changes from Original (January 2009) to Revision A **Page**

- Changed note refernece within the AC ELECTRICAL CHARACTERISTICS table 7
- Added a Typ value of 0.04ps to the Additive phase jitter in the AC ELECTRICAL CHARACTERISTICS 7

5 Pin Configuration and Functions

RHB, VF, or VFP Package
32-Pin VQFN, LQFP, or HLQFP
Top View



Pin Functions[1]

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLK_SEL	2	Input	Clock select. Used to select between CLK0 and CLK1 input pairs. LVTTL/LVCMOS functionality compatible.
CLK0, $\overline{\text{CLK0}}$	3	Input	Differential LVECL/LVPECL input pair
	4		
CLK1, $\overline{\text{CLK1}}$	6		
	7		
Q [9:0]	11	Output	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
	13		
	15		
	18		
	20		
	22		
	24		
	27		
	29		
	31		
$\overline{\text{Q}}$[9:0]	10	Output	LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{\text{CLKn}}$.
	12		
	14		
	17		
	19		
	21		
	23		
	26		
	28		
	30		
V_{BB}	5	—	Reference voltage output for single-ended input operation

(1) CLKn, CLK_SEL pulldown resistor = 75 kΩ; $\overline{\text{CLKn}}$ pullup resistor = 37.5 kΩ; $\overline{\text{CLKn}}$ pulldown resistor = 50 kΩ.

Pin Functions(1) (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{CC}	1	Power	Supply voltage
	9		
	16		
	25		
	32		
V_{EE}	8	Ground	Device ground or negative supply voltage in ECL mode
PowerPAD™	0	Ground	The PowerPAD of the QFN32 is thermally connected to the die to improve the heat transfer out of the package. The pad of the QFN32 with PowerPAD must be connected to V_{EE}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage (Relative to V_{EE})	–0.3	4.6	V
V_I	Input voltage	–0.3	V_{CC} + 0.5	V
V_O	Output voltage	–0.3	V_{CC} + 0.5	V
I_{IN}	Input current		±20	mA
V_{EE}	Negative supply voltage (Relative to V_{CC})	–4.6	0.3	V
I_{BB}	Sink/source current	–1	1	mA
I_O	DC output current		–50	mA
T_J	Maximum operating junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (relative to V_{EE})	2.375	2.5/3.3	3.8	V
T_A	Operating free-air temperature	–40		85	°C/W
T_J	Operating junction temperature			110	°C

6.4 Thermal Information

THERMAL METRIC[1]		CDCLVP111		UNIT
		RHB (VQFN)	VF (LQFP)	
		32 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.2	85.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.5	23.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	49.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.9	48.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.7	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics, LVECL

Vsupply: V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85°C	40		85	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} – 2 V	–40°C			354	mA
			25°C			380	
			85°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors, $V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 2 V	–40°C, 25°C, 85°C	–150		150	µA
V_{BB}	Internally generated bias voltage	For V_{EE} = –3 to –3.8 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.45	–1.3	–1.15	V
		V_{EE} = –2.375 to –2.75 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.4	–1.25	–1.1	
V_{IH}	High-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	–1.165		–0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	–1.81		–1.475	V
V_{ID}	Input amplitude (CLKn, $\overline{CLKn}$)	Difference of input, see [1] $\lvert V_{IH} - V_{IL} \rvert$	–40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, $\overline{CLKn}$)	DC offset relative to V_{EE}	–40°C, 25°C, 85°C	V_{EE} + 1		–0.3	V
V_{OH}	High-level output voltage	I_{OH} = –21 mA	–40°C	–1.26		–0.85	V
			25°C	–1.2		–0.85	
			85°C	–1.15		–0.85	
V_{OL}	Low-level output voltage	I_{OL} = –5 mA	–40°C	–1.85		–1.5	V
			25°C	–1.85		–1.45	
			85°C	–1.85		–1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} –2 V, see Figure 5	–40°C, 25°C, 85°C	600			mV

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

6.6 DC Electrical Characteristics, LVPECL

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85°C	40		85	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} – 2 V	-40°C			354	mA
			25°C			380	
			85°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors V_{IH}=V_{CC}, V_{IL}= V_{CC}–2V	–40°C, 25°C, 85°C	–150		150	µA
V_{BB}	Internally generated bias voltage	V_{CC} = 3 to 3.8 V, I_{BB}= –0.2 mA	–40°C, 25°C, 85°C	V_{CC} – 1.45	V_{CC} – 1.3	V_{CC} – 1.15	V
		V_{CC} = 2.375 to 2.75 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	V_{CC} – 1.4	V_{CC} – 1.25	V_{CC} – 1.1	
V_{IH}	High-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	V_{CC} – 1.165		V_{CC} – 0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	V_{CC} – 1.81		V_{CC} – 1.475	V
V_{ID}	Input amplitude (CLKn, $\overline{CLKn}$)	Difference of inpu, see (1), $\lvert V_{IH} - V_{IL} \rvert$	–40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, $\overline{CLKn}$)	DC offset relative to V_{EE}	–40°C, 25°C, 85°C	1		V_{CC} – 0.3	V
V_{OH}	High-level output voltage	I_{OH} = –21 mA	–40°C	V_{CC} – 1.26		V_{CC} – 0.85	V
			25°C	V_{CC} – 1.2		V_{CC} – 0.85	
			85°C	V_{CC} – 1.15		V_{CC} – 0.85	
V_{OL}	Low-level output voltage	I_{OL} = –5 mA	–40°C	V_{CC} – 1.85		V_{CC} – 1.5	V
			25°C	V_{CC} – 1.85		V_{CC} – 1.45	
			85°C	V_{CC} – 1.85		V_{CC} – 1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} - 2 V, see Figure 5	–40°C, 25°C, 85°C	600			mV

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

6.7 AC Electrical Characteristics

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V or LVECL/LVPECL input V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Differential propagation delay CLKn, $\overline{CLKn}$ to all Q0, $\overline{Q0}$… Q9, $\overline{Q9}$	See Note D in Figure 2	200		350	ps
$t_{sk(o)}$	Output-to-output skew	See Note A in Figure 2		15	30	ps
$t_{sk(pp)}$	Part-to-part skew	See Note B in Figure 2			70	ps
t_{aj}	Additive phase jitter	Integration bandwidth of 20 kHz to 20 MHz, fout = 125 MHz at 25°C		0.04	< 0.8	ps
$f_{(max)}$	Maximum frequency	Functional up to 3.5 GHz			3500	MHz
t_r/t_f	Output rise and fall time (20%, 80%)	See Note D in Figure 2	90		200	ps

6.8 Typical Characteristics

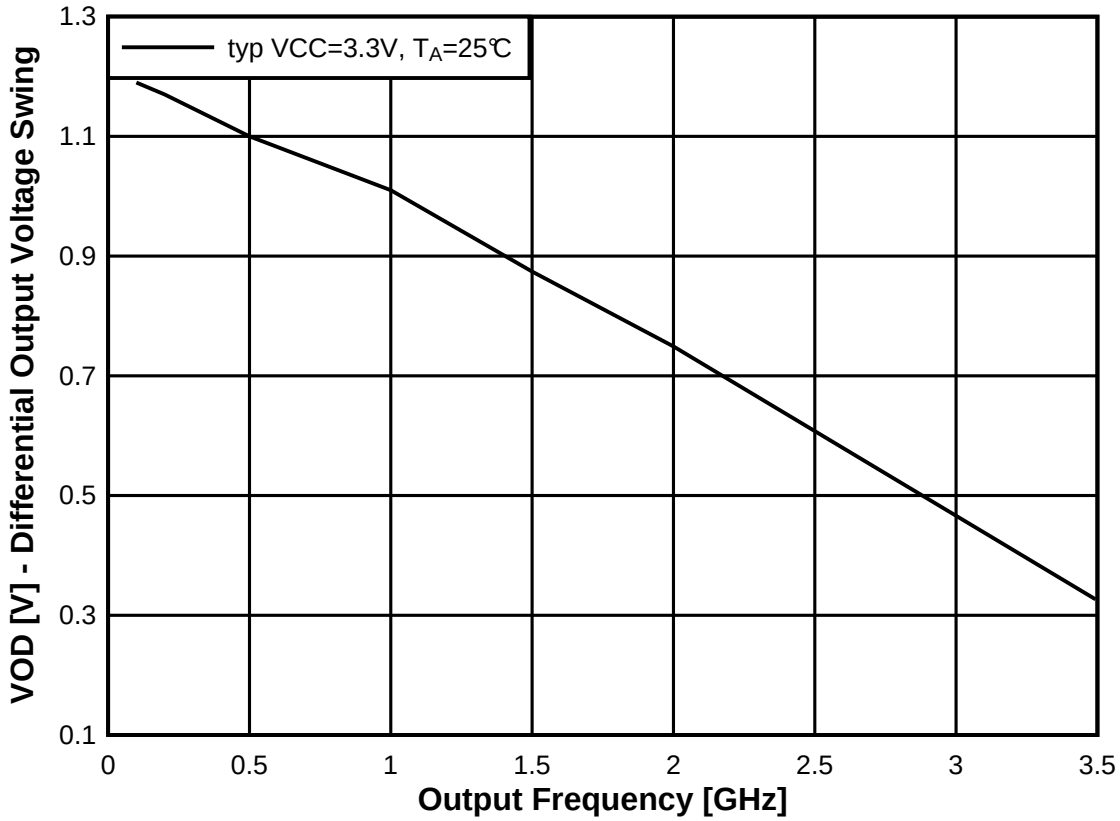
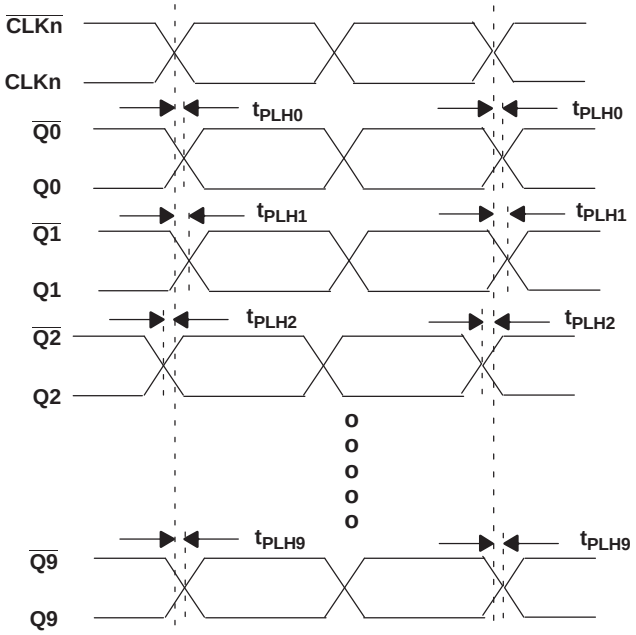


Figure 1. LVPECL Input Using CLK0 Pair, V_{CM} = 1 V, V_{ID} = 0.5 V

7 Parameter Measurement Information

7.1 Test Configurations



A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9).

B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) across multiple devices or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9) across multiple devices.

C. Typical value measured at ambient when clock input is 155.52 MHz for an integration bandwidth of 20 kHz to 5 MHz.

D. Input conditions: V_{CM} = 1 V, V_{ID} = 0.5 V and F_{IN} = 1 GHz.

Figure 2. Waveform for Calculating Both Output and Part-to-Part Skew

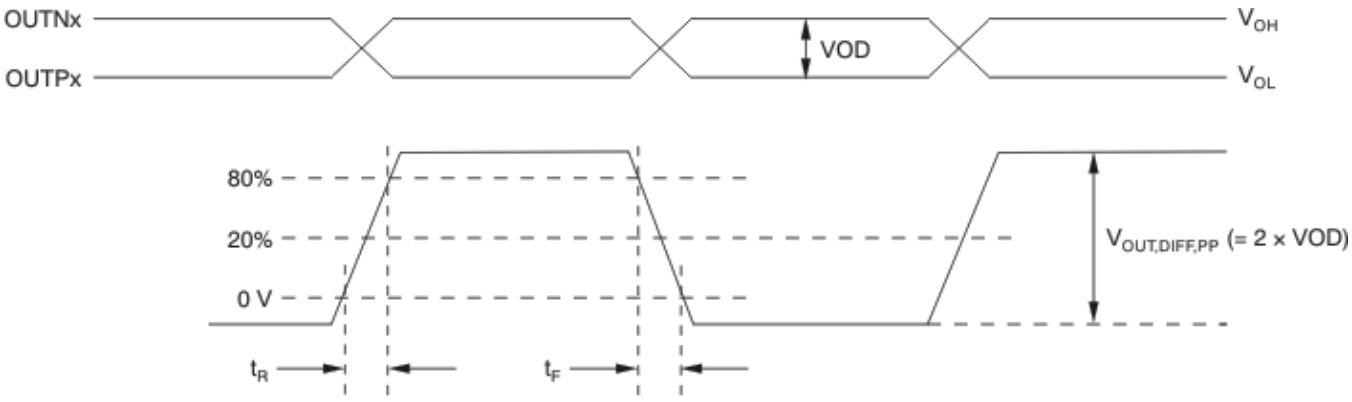


Figure 3. Output Voltage and Rise and Fall Time

Test Configurations (continued)

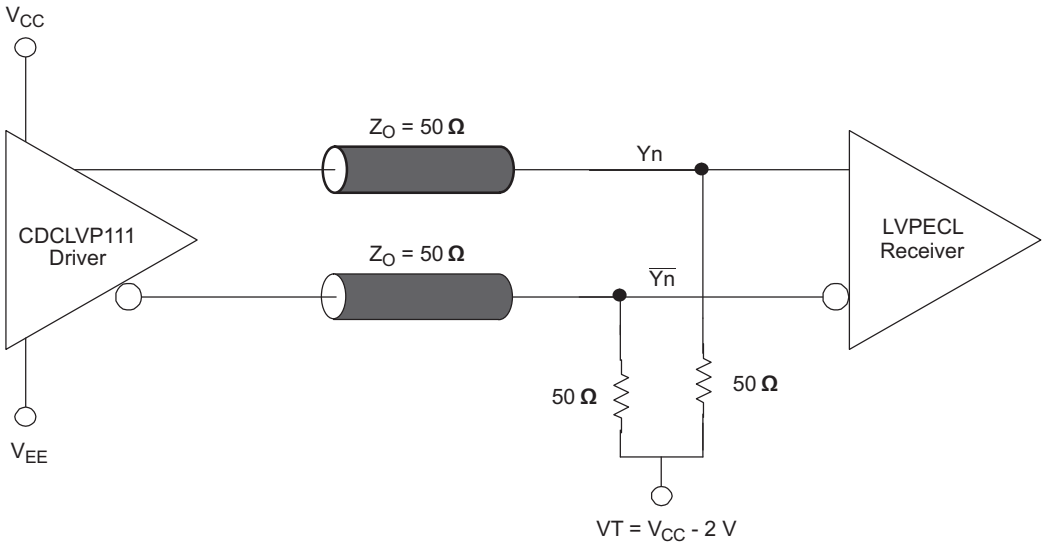


Figure 4. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, SCAA056)

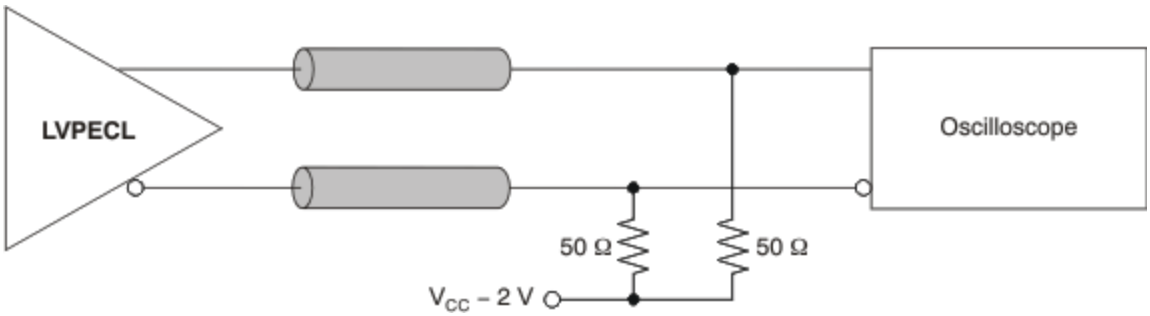


Figure 5. LVPECL Output DC Configuration During Device Test

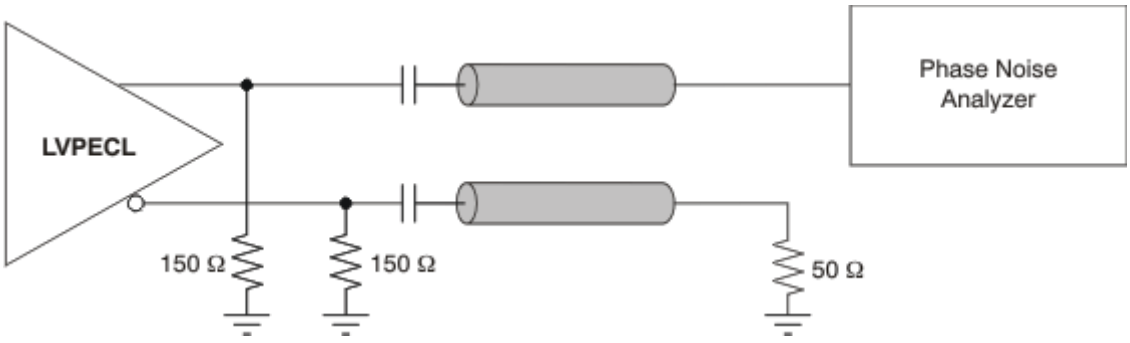


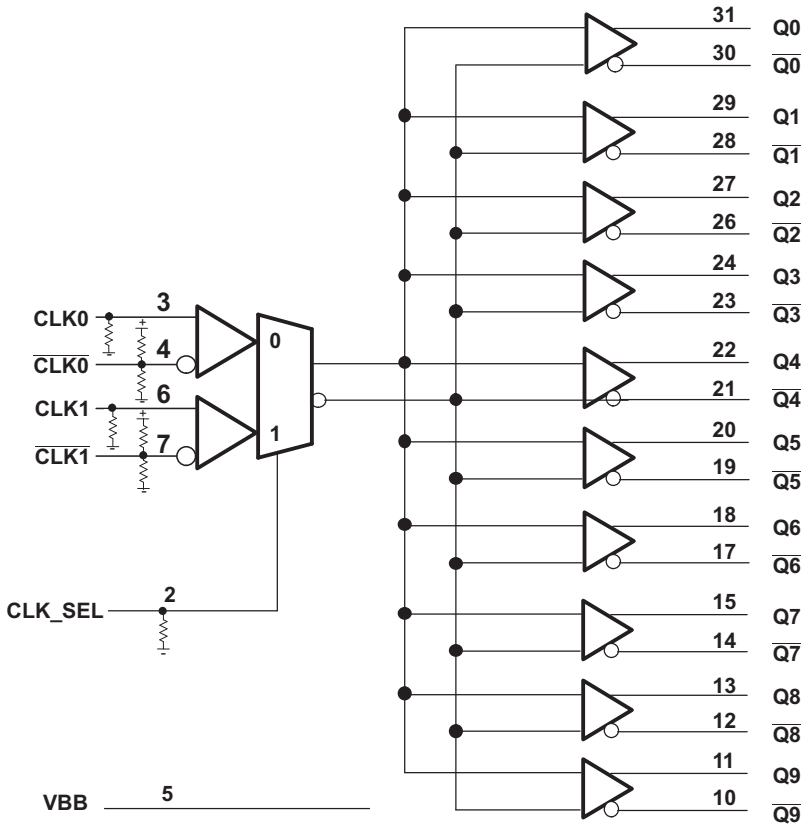
Figure 6. LVPECL Output AC Configuration During Device Test

8 Detailed Description

8.1 Overview

The CDCLVP111 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is a 50 Ω to (V_{CC} –2) V, but this DC voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (DC) and AC-coupled configurations. These configurations are shown in Figure 8 (a and b) for V_{CC} = 2.5 V and Figure 9 (a and b) for V_{CC} = 3.3 V, respectively. TI recommends to place all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, AC coupling is required.

8.2 Functional Block Diagram



8.3 Feature Description

The CDCLVP111 is a low-additive jitter universal to LVPECL fan out buffer with 2 selectable inputs. The small package, low-output skew, and low-additive jitter make for a flexible device in demanding applications.

8.4 Device Functional Modes

Select Input Terminal By CLK_SEL Pin

Table 1. Function Table

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

The two inputs of the CDCLVP111 are internally mixed together and can be selected through the control pin. Unused inputs and outputs can be left floating to reduce overall component cost. Both AC and DC coupling schemes can be used with the CDCLVP111 to provide greater system flexibility.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCLVP111 is a low-additive jitter LVPECL fanout buffer that can generate 5 copies of 2 selectable LVDS, CML or SSTL inputs. The CDCLVP111 can accept reference clock frequencies up to 3.5 GHz while providing low-output skew.

9.2 Typical Application

9.2.1 Fanout Buffer for Line Card Application

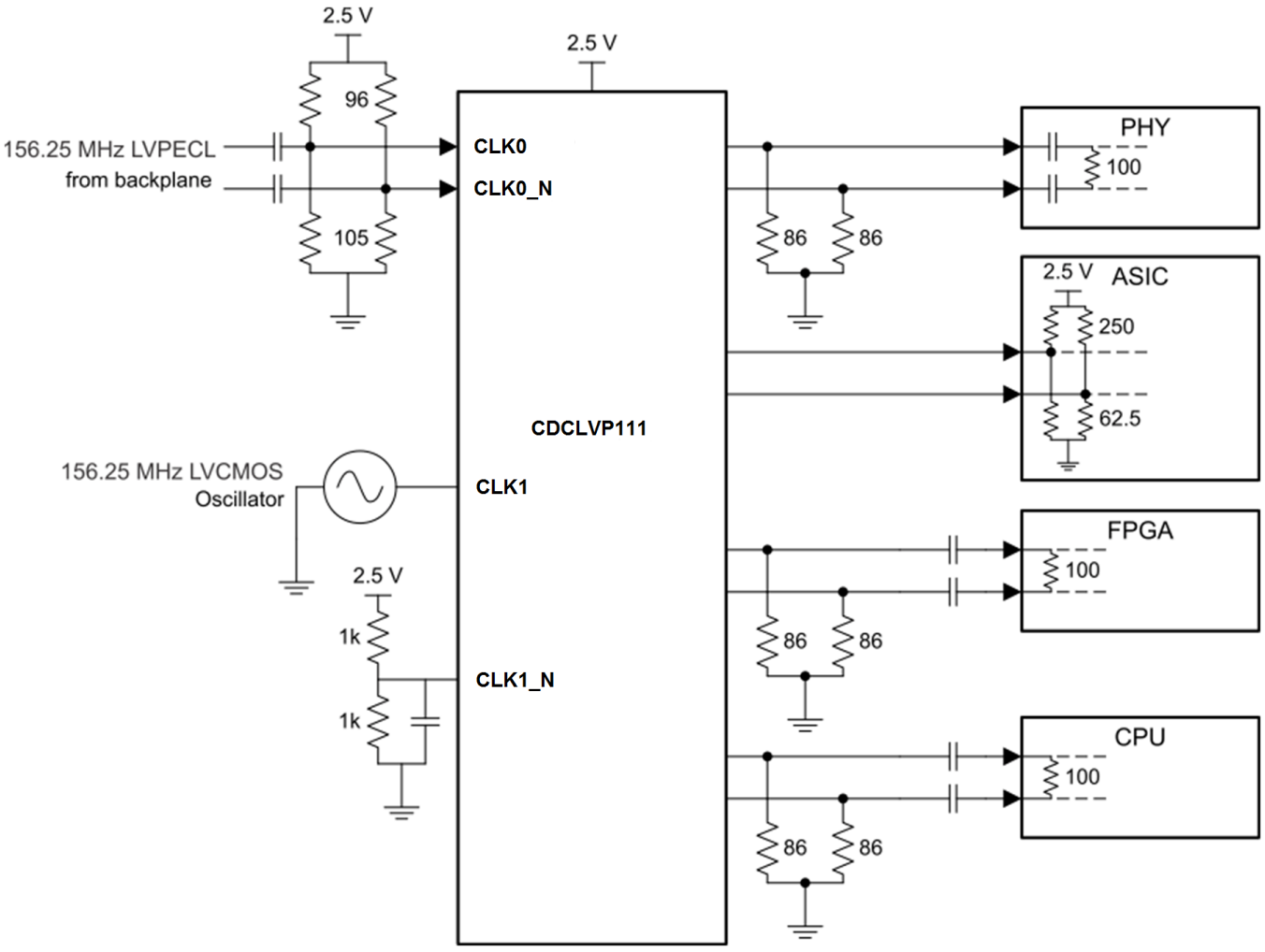


Figure 7. CDCLVP111 Block Diagram

Typical Application (continued)

9.2.1.1 Design Requirements

The CDCLVP111 shown in Figure 7 is configured to be able to select 2 inputs, a 156.25-MHz LVPECL clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. Either signal can be then fanned out to desired devices, as shown.

The configuration example is driving 4 LVPECL receivers in a line card application with the following properties:

- The PHY device has internal AC coupling and appropriate termination and biasing. The CDCLVP111 will need to be provided with 86-Ω emitter resistors near the driver for proper operation.
- The ASIC is capable of DC coupling with a 2.5-V LVPECL driver such as the CDCLVP111. This ASIC features internal termination so no additional components are needed.
- The FPGA requires external AC coupling but has internal termination. Again, 86-Ω emitter resistors are placed near the CDCLVP111 and a 0.1-uF are placed to provide AC coupling. Similarly, the CPU is internally terminated and requires external AC coupling capacitors.

9.2.1.2 Detailed Design Procedure

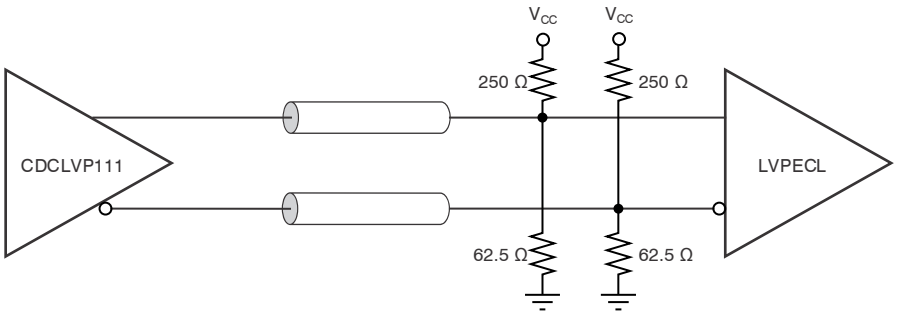
Unused outputs can be left floating.

In this example, the PHY, ASIC, and FPGA/CPU require different schemes. Power-supply filtering and bypassing is critical for low-noise applications.

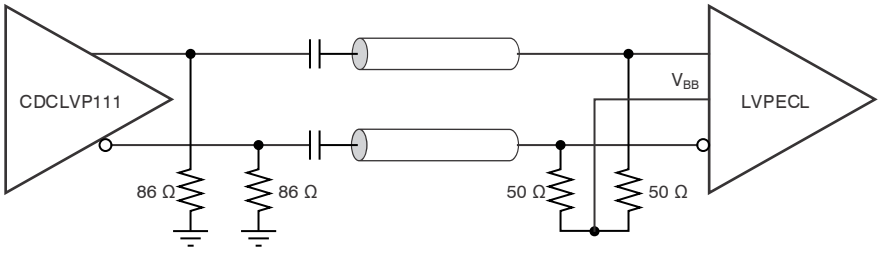
See Figure 18 for recommended filtering techniques.

9.2.1.2.1 LVPECL Output Termination

Refer to Figure 8 for output termination schemes depending on the receiver application.



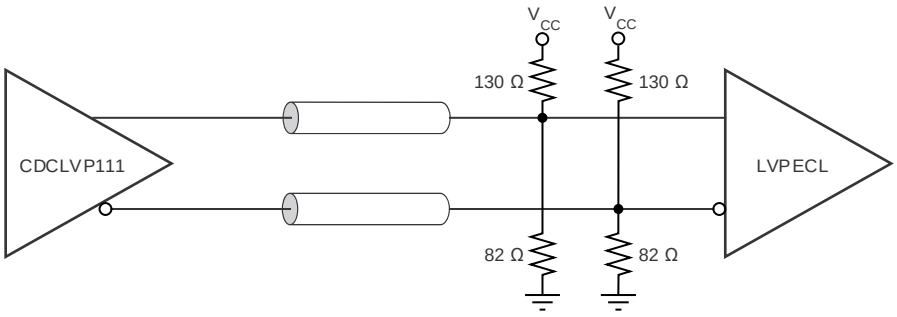
(a) Output DC Termination



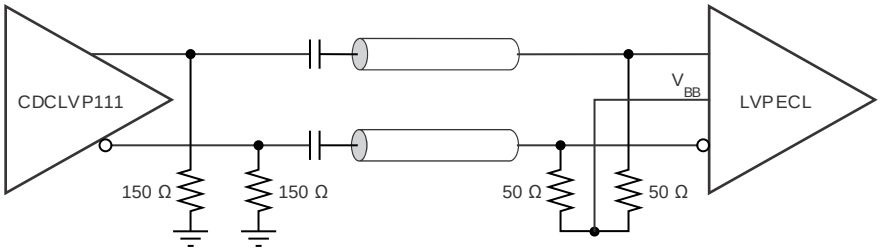
(b) Output AC Termination

Figure 8. LVPECL Output DC and AC Termination for V_{CC} = 2.5 V

Typical Application (continued)



(a) Output DC Termination



(b) Output AC Termination

Figure 9. LVPECL Output DC and AC Termination for V_{CC} = 3.3 V

9.2.1.2.2 Input Termination

The CDCLVP111 inputs can be interfaced with LVPECL, LVDS, or LVCMOS drivers. Figure 10 illustrates how to DC couple an LVCMOS input to the CDCLVP111. The series resistance (R_S) should be placed close to the LVCMOS driver; the value is calculated as the difference between the transmission line impedance and the driver output impedance.

Refer to Figure 10 for proper input terminations, dependent on single ended or differential inputs.

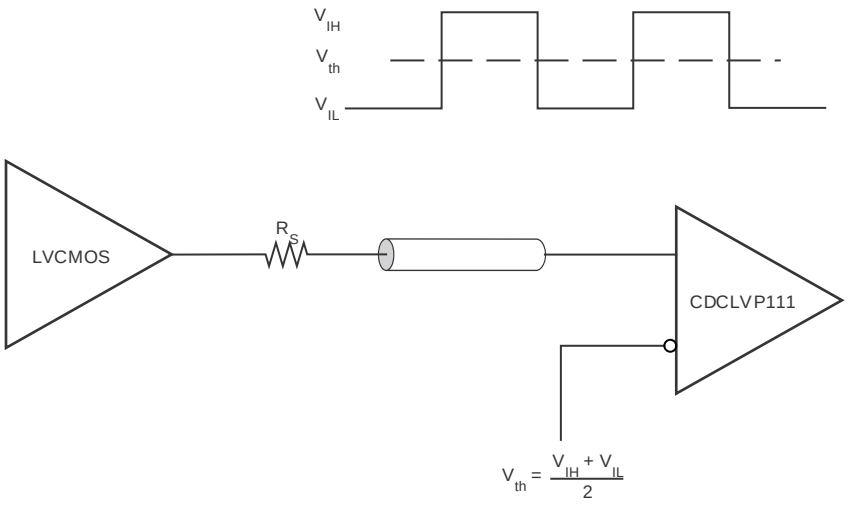


Figure 10. DC-Coupled LVCMOS Input to CDCLVP111

Typical Application (continued)

Figure 11 shows how to DC couple LVDS inputs to the CDCLVP111. Figure 12 and Figure 13 describe the method of DC coupling LVPECL inputs to the CDCLVP111 for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively.

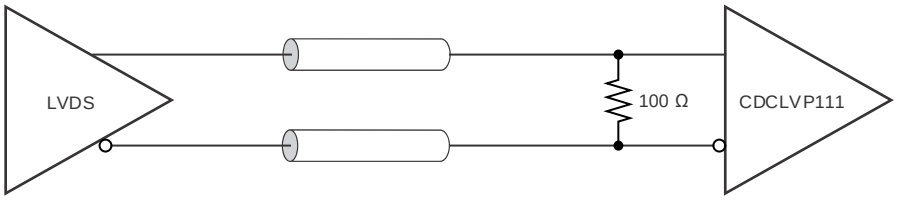


Figure 11. DC-Coupled LVDS Inputs to CDCLVP111

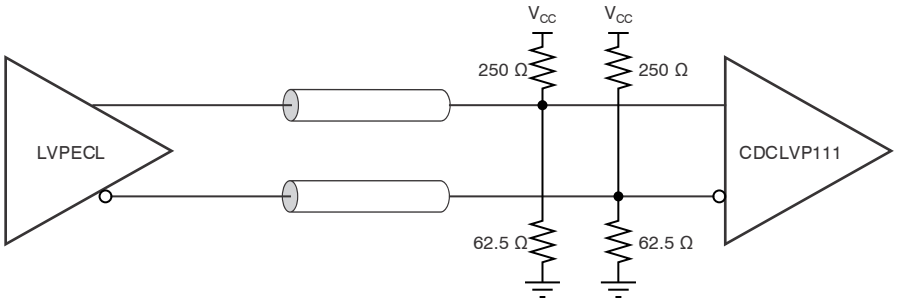


Figure 12. DC-Coupled LVPECL Inputs to CDCLVP111 (V_{CC} = 2.5 V)

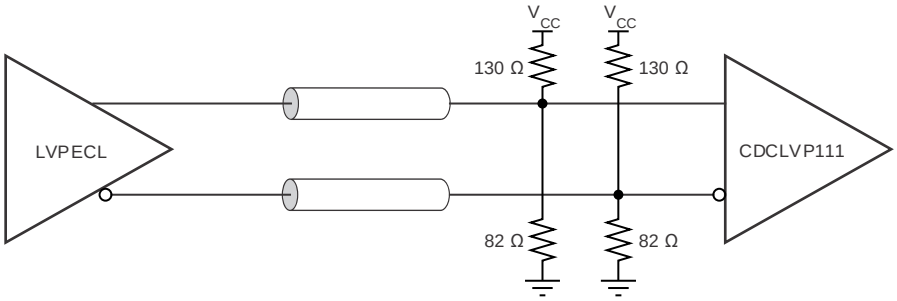


Figure 13. DC-Coupled LVPECL Inputs to CDCLVP111 (V_{CC} = 3.3 V)

Typical Application (continued)

Figure 14 and Figure 15 show the technique of AC coupling differential inputs to the CDCLVP111 for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively. TI recommends to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, AC coupling is required.

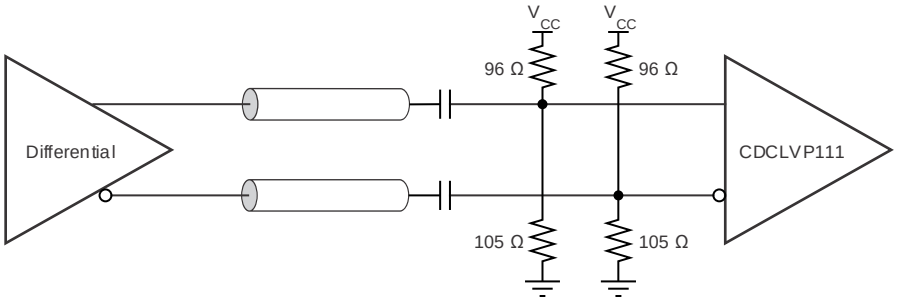


Figure 14. AC-Coupled Differential Inputs to CDCLVP111 (V_{CC} = 2.5 V)

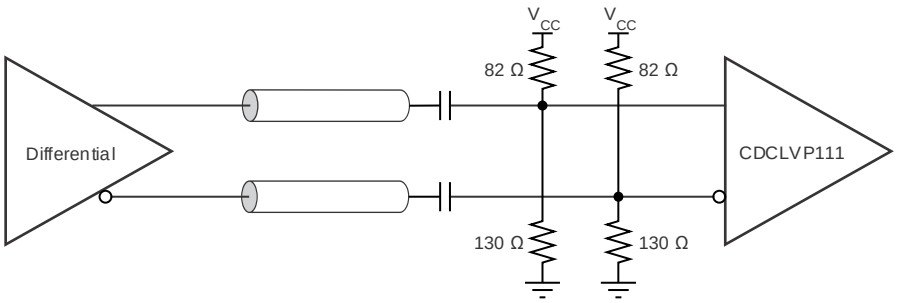
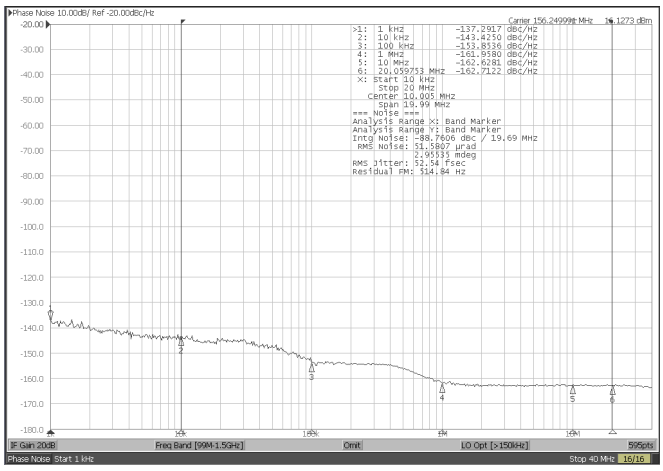


Figure 15. AC-Coupled Differential Inputs to CDCLVP111 (V_{CC} = 3.3 V)

9.2.1.3 Application Curves

The CDCLVP111 low-additive noise can be shown in this line card application. The low-noise, 156.25-MHz signal with 53-fs RMS jitter drives the CDCLVP111, resulting in 86-fs RMS when integrated from 10 kHz to 20 MHz. The resultant-additive jitter is a low 68-fs RMS for this configuration.



Reference signal is low noise signal generator

Figure 16. CDCLVP111 Reference Phase Noise 32 fs rms (10 kHz to 20 MHz)

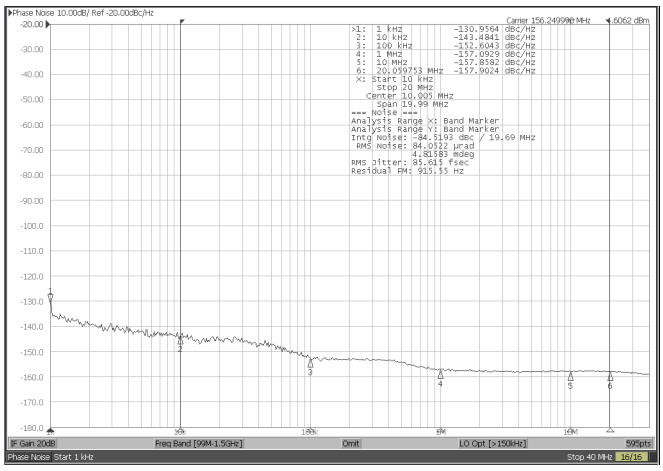


Figure 17. CDCLVP111 Output Phase Noise 57 fs rms (10 kHz to 20 MHz)

10 Power Supply Recommendations

10.1 Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter and phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. TI recommends to add as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply terminals in the package. TI recommends, but does not require, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low dc resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 18 illustrates this recommended power-supply decoupling method.

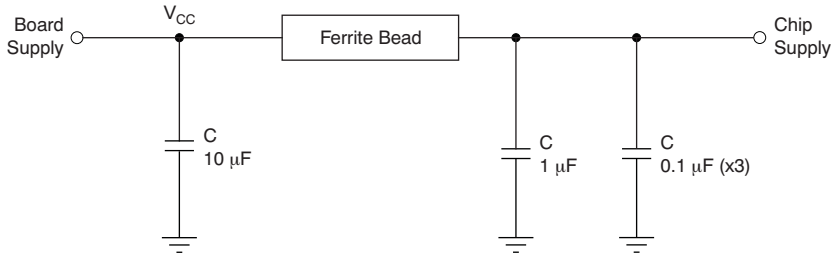


Figure 18. Power-Supply Decoupling

11 Layout

11.1 Layout Guidelines

Power consumption of the CDCLVP111 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +110°C. That is, as an estimate, ambient temperature (TA) plus device power consumption times $R_{\theta JA}$ should not exceed +110°C.

The device package has an exposed pad that provides the primary heat removal path to the printed-circuit-board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 19 shows a recommended land and via pattern.

11.2 Layout Example

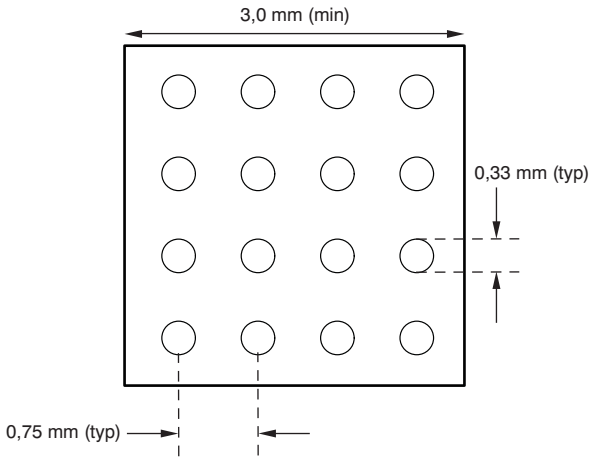


Figure 19. Recommended PCB Layout

11.3 Thermal Management

Power consumption of the CDCLVP111 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +110°C. That is, as an estimate, ambient temperature (T_A) plus device power consumption times $R_{\theta JA}$ should not exceed +110°C.

The device package has an exposed pad that provides the primary heat removal path to the printed-circuit-board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 19 shows a recommended land and via pattern.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Interfacing Between LVPECL, LVDS, and CML Application Note, SCAA056

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVP111RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVP111	Samples
CDCLVP111RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVP111	Samples
CDCLVP111VF	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP111	Samples
CDCLVP111VFR	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP111	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CDCLVP111 :

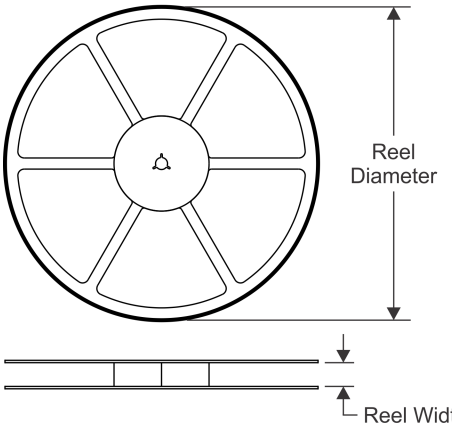
- Enhanced Product: CDCLVP111-EP

NOTE: Qualified Version Definitions:

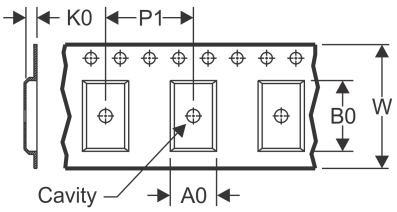
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

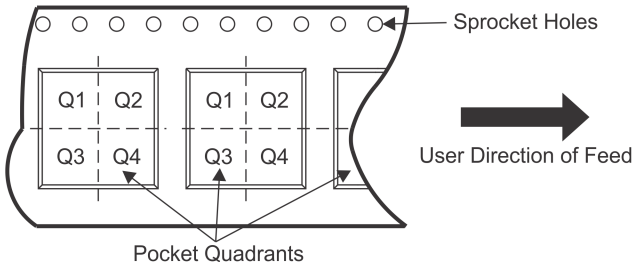


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

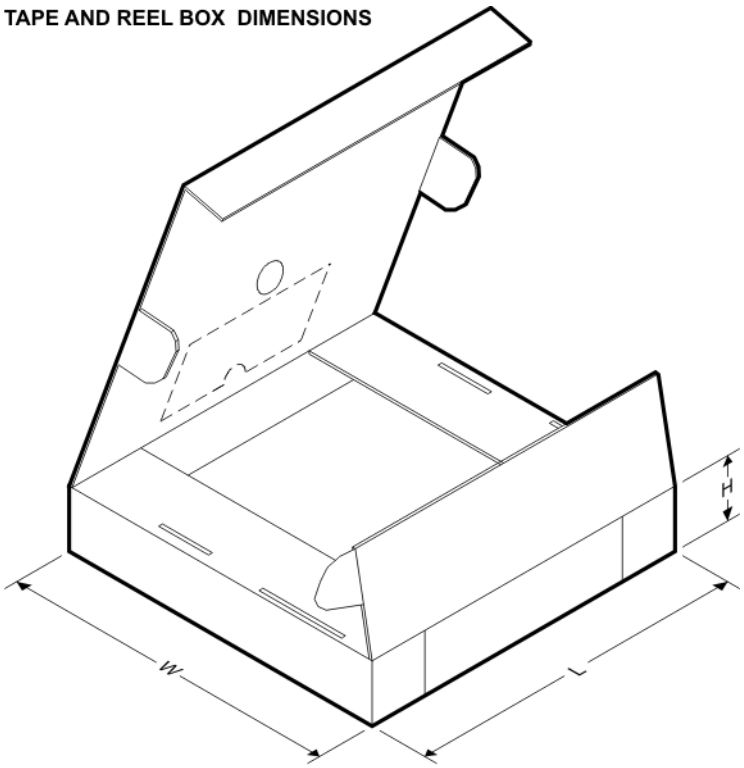
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP111VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

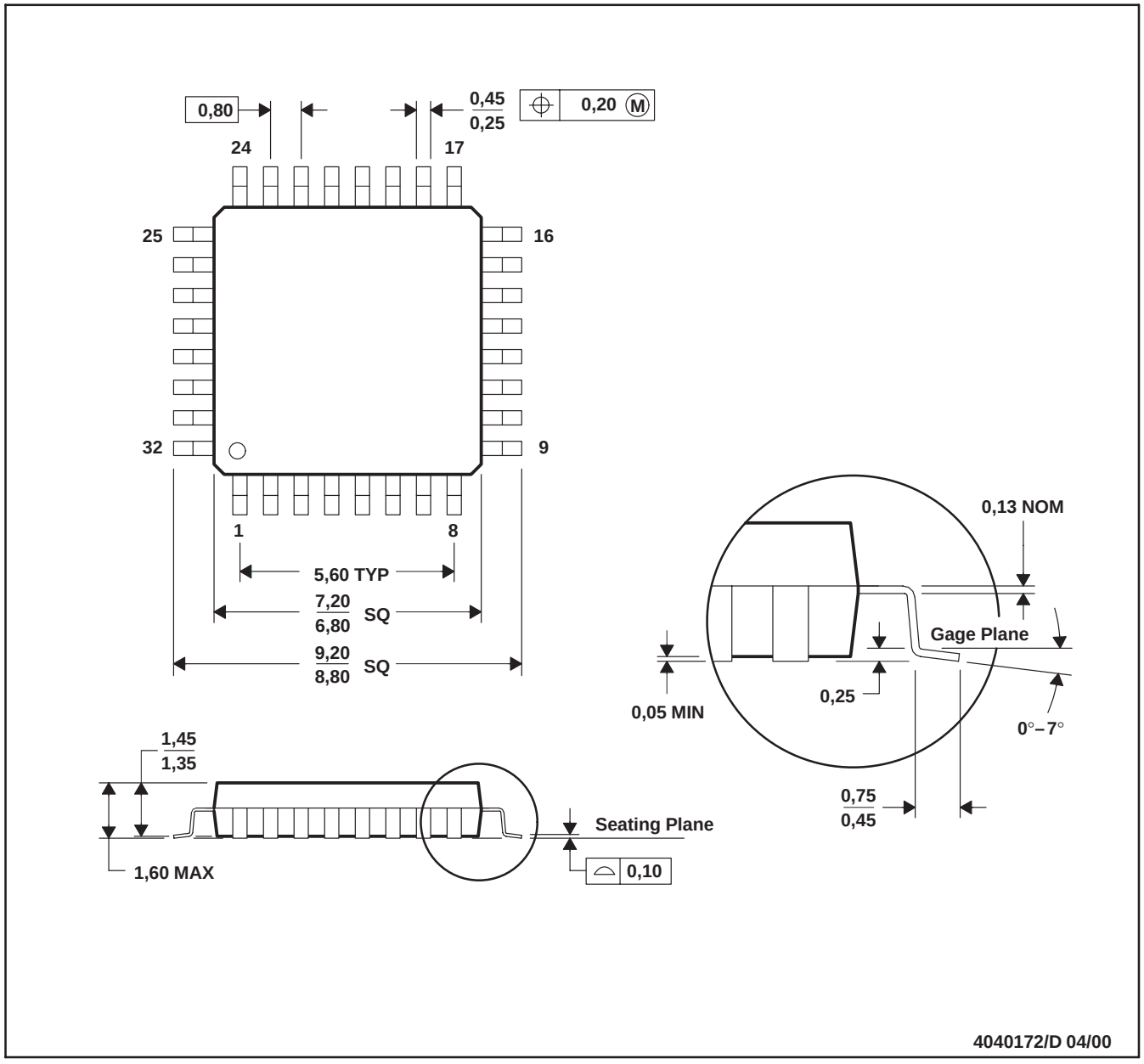


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP111VFR	LQFP	VF	32	1000	367.0	367.0	38.0

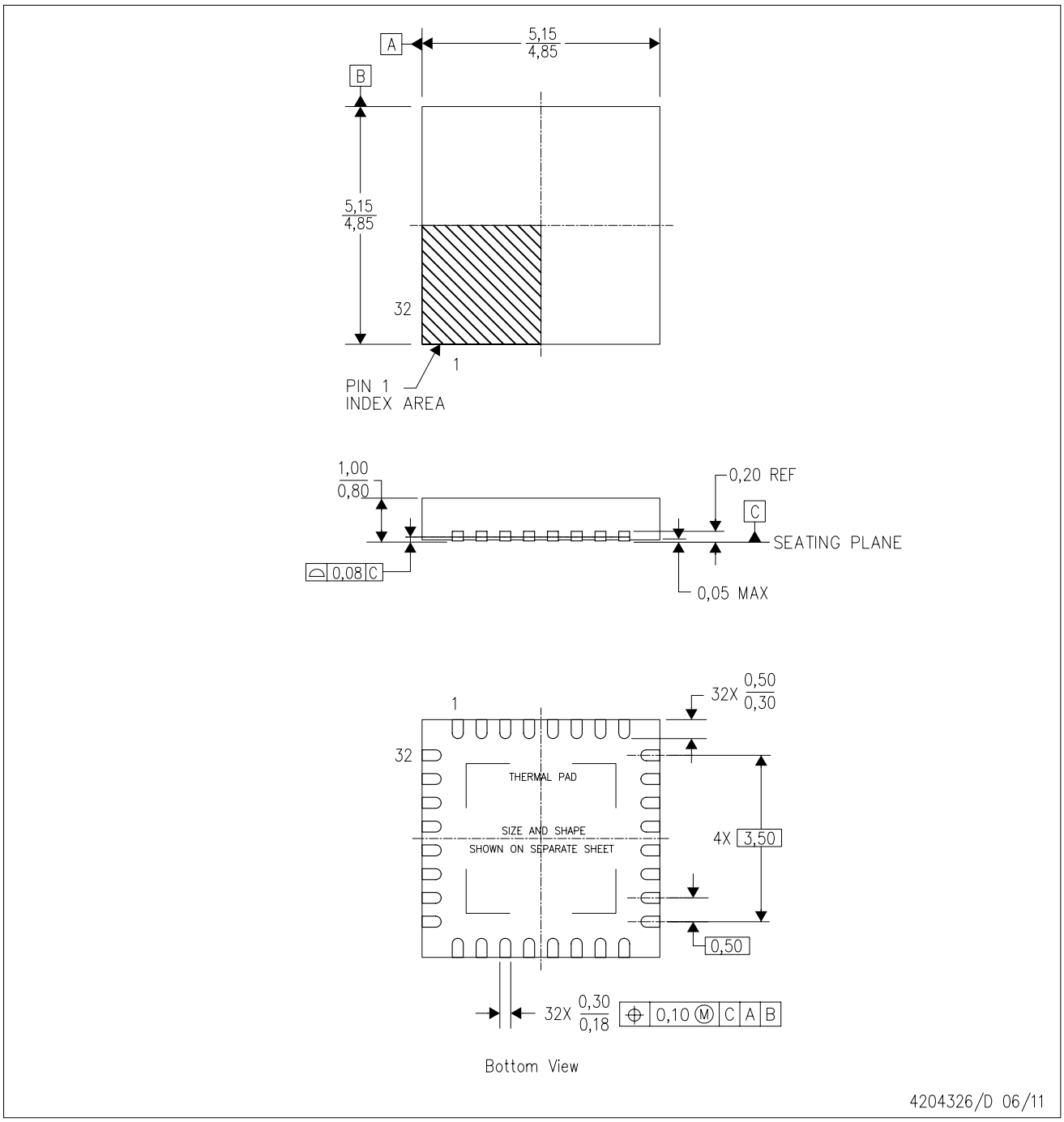
MTQF002B – JANUARY 1995 – REVISED MAY 2000

VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

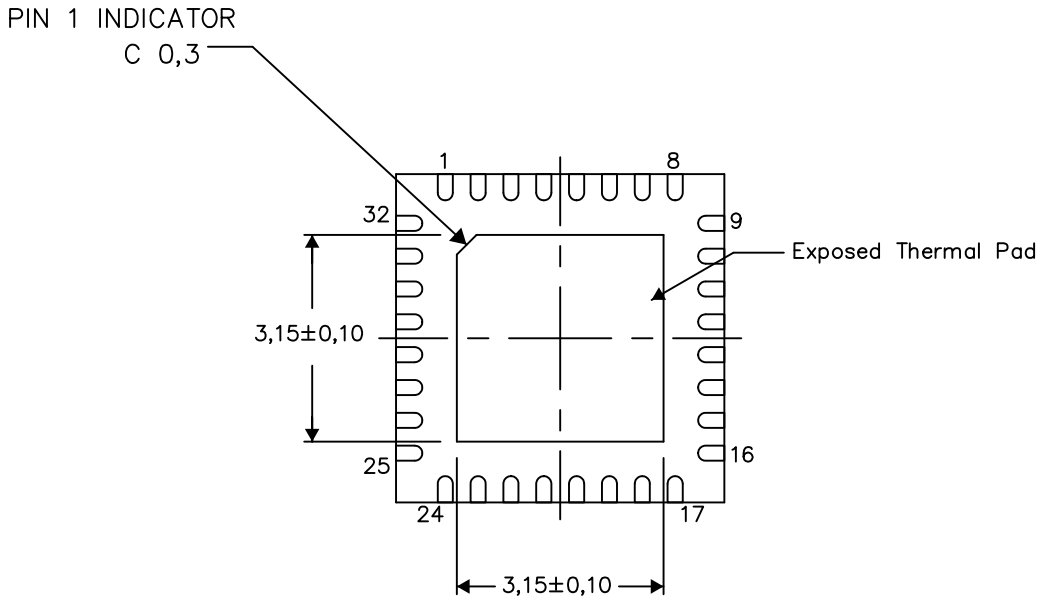
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



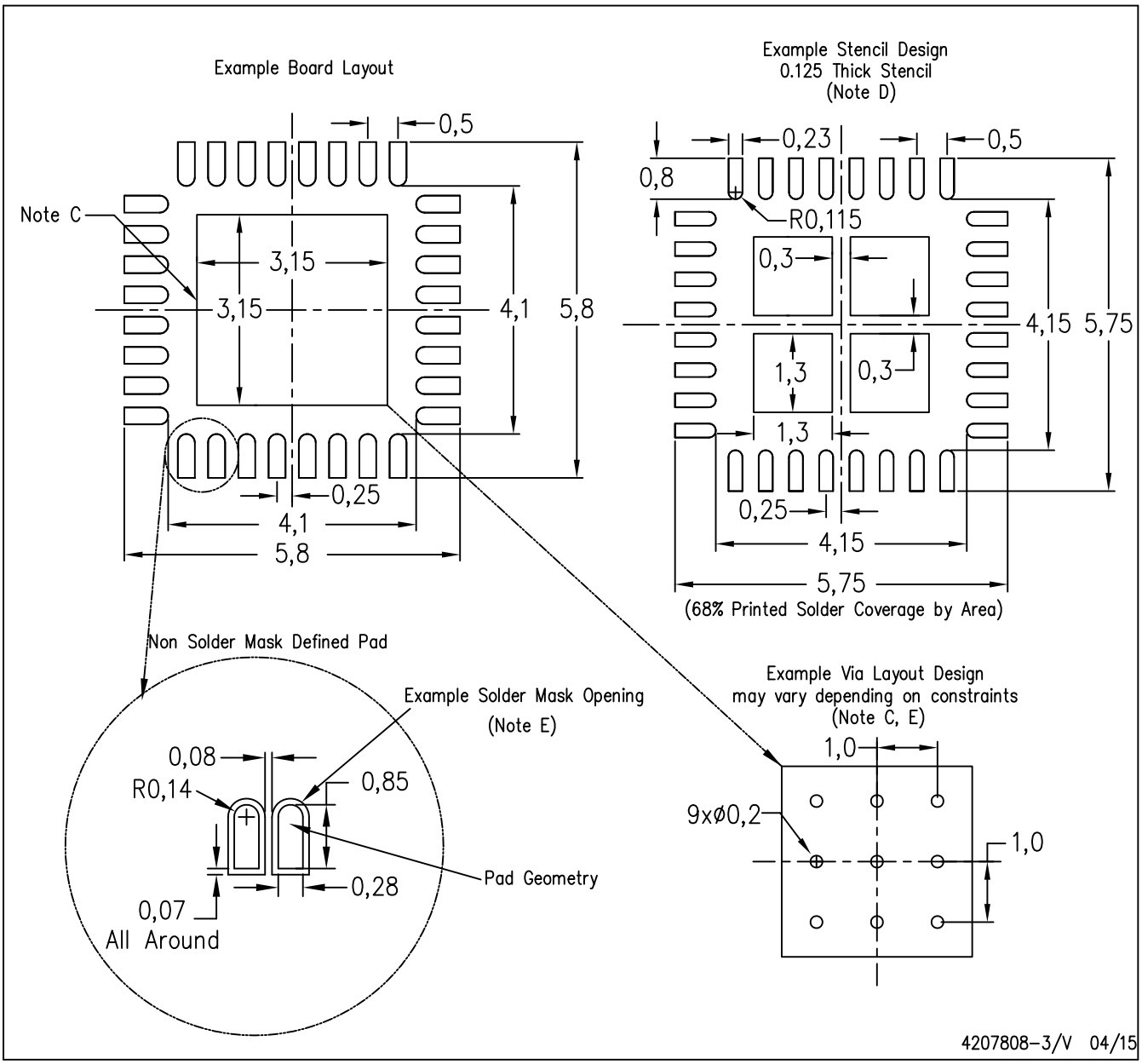
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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