Dual-Ouputs 6-A Buck Converter with Integrated DCP Scheme

1 Description

The SC8102A is a synchronous dual-output ports buck converter with a wide input voltage from 5V to 36V. The SC8102A regulates the output voltage at a fixed 5V or customized voltage by setting the divider resistor. It also provides high accurate output current limit. The converter enters Constant Current (CC) Mode in case any of the two output channels reaches the setting current limit. The total output power can be programmed by a resistor, which makes it easy for constant power control.

The SC8102A adopts fixed line drop compensation, programmable frequency setting and PWM/PFM mode operation. It also integrates automatic DCP mode and Type-C current mode, so that a USB controller can be saved. With minimum external components, maximum functions can be achieved for user's different applications.

The SC8102A also supports full protections including under voltage protection, over voltage protection, short current protection and auto-restart, over temperature protection.

The SC8102A adopts 32 pin QFN 5x5 package.

2 Features

- Wide input operating voltage from 5V to 36V
- 11mΩ/27mΩ Low Rdson Internal Power MOSFETs
- Max output capacity with 5V/6A
- 100% duty cycle operation
- Low quiescent current
- Programmable output power limit
- Build-in DP/DM for USB DCP modes:
  - BC1.2 DCP Mode
  - Divider Mode
  - 1.2V/1.2V Mode
- Build-in USB Type-C 3A current mode
- Integrated NMOS gate driver
- Build-in line drop compensation
- PFM/PWM mode selection
- Adjustable frequency 80kHz to 600kHz
- Hiccup and auto-restart
- Full protection of UVLO, OVP, OCP, OTP

3 Applications

- Car Charger
- Multi-Ports Wall Charger
- Hub
- Industrial applications

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8102AQDJR	32 pin QFN	5 mm x 5 mm x 0.75 mm

5 Typical Application Circuit

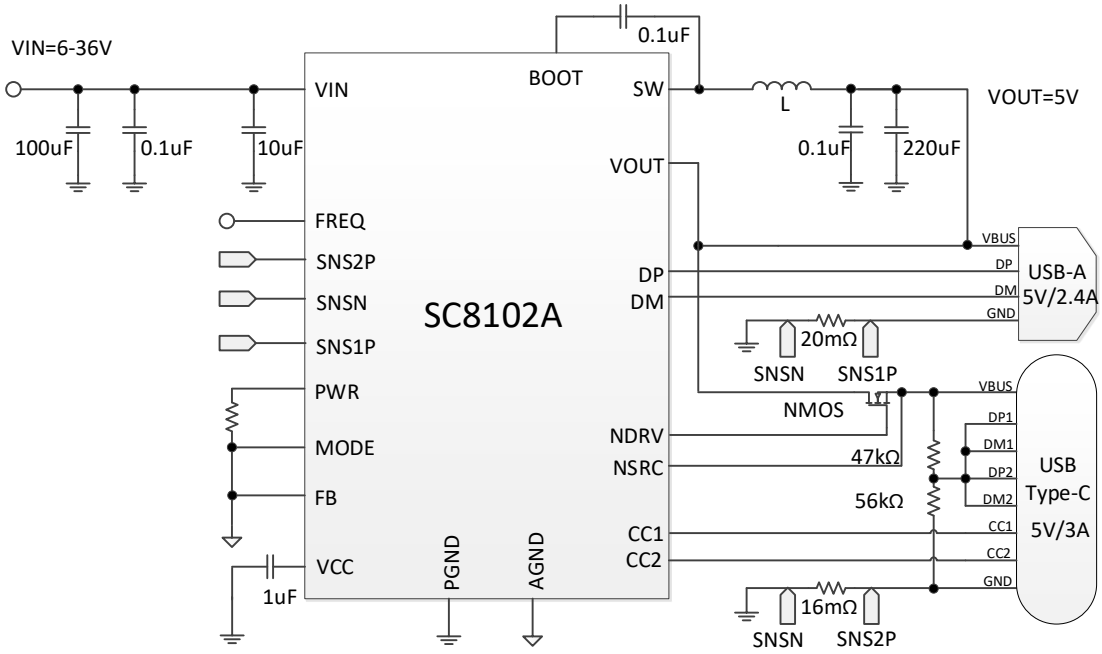


Figure.1 Typical Application Circuit with Dual-Outputs and Isolated NMOS

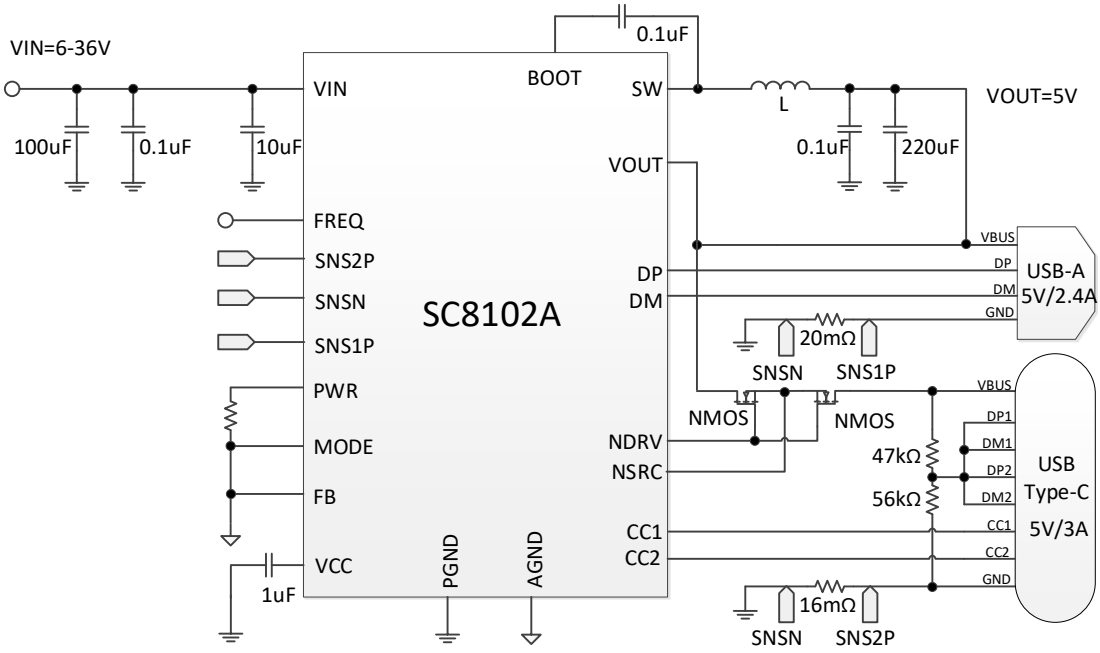
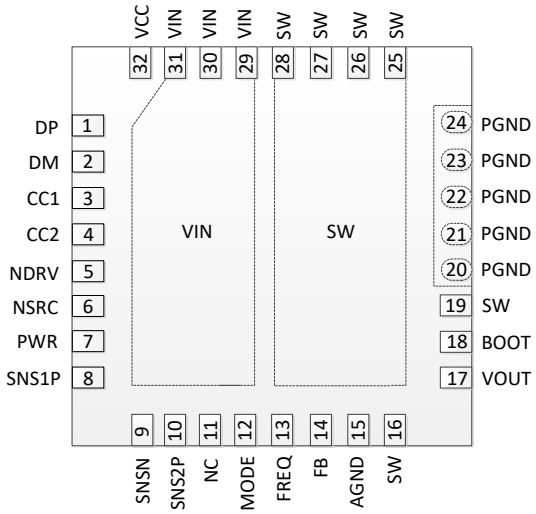


Figure.2 Typical Application Circuit with Dual-Outputs and Back-to-Back Isolated NMOS

6 Terminal Configuration and Functions



QFN 32 Package Reference

(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	DP	I/O	D+ data line to USB connector 2, used for hand-shaking with portable devices.
2	DM	I/O	D- data line to USB connector 2, used for hand-shaking with portable devices.
3	CC1	I/O	Configuration Channel 1 to USB Type-C connector.
4	CC2	I/O	Configuration Channel 2 to USB Type-C connector.
5	NDRV	O	Gate signal for isolated Type-C NMOS
6	NSRC	O	Source signal for isolated Type-C NMOS
7	PWR	I	Output power limit pin. Setting the output power limit by connecting a resistor to GND
8	SNS1P	I	Positive end of output 1 current sense amplifier.
9	SNSN	I	Negative end of output current sense amplifier.
10	SNS2P	I	Positive end of output 2 current sense amplifier.
11	NC		Floating.
12	MODE	I	Mode selection pin. Logic high level sets the device working in PWM mode; logic low level or floating sets the device working in PFM mode.
13	FREQ	I	The operation frequency is programmed by a resistor between this pin and AGND. Leaving this pin floating sets the device working in 120kHz.

14	FB	I	Output voltage feedback. Connect the center of two divider resistor to program the output voltage. Output voltage be configured for fixed 5.1V with FB pin connected to GND.
15	AGND	I/O	Analog Ground.
17	VOUT	I	Output node of the Buck.
18	BOOT	PWR	Connect a capacitor between BT and SW to bootstrap a voltage to provide the bias for high side MOSFET driver.
16, 19, 25, 26, 27, 28	SW	PWR	Switching node.
20~24	PGND	PWR	Power ground.
29, 30, 31	VIN	I	Input node of Buck. Connect a 10 µF ceramic capacitor from VIN to PGND pin.
32	VCC	PWR	Output of internal regulator to provide 5.2V voltage for the bias voltage of internal gate drivers. Connect a 1 µF ceramic capacitor from VCC to PGND pin.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, VOUT, SNS1P, SNSN, SNS2P,	-0.3	42	V
	SW	-1	42	V
	NDRV	-1	10	V
	FB, DP, DM, CC1, CC2, VCC, FREQ, MODE, NSRC, PWR	-0.3	6.5	V
	BOOT	-0.3	50	V
Temperature Range	Operating Junction, T_J	-40	150	°C
	Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2) for DP/DM pin	-8	8	kV
	Human body model (HBM) ESD stress voltage(2) for CC1/CC2 pin	-8	8	kV
	Human body model (HBM) ESD stress voltage for other pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage (3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	6		36	V
V_{OUT}	Output voltage range		5		V
C_{IN}	Input Capacitance	30	100		µF
C_{OUT}	Output capacitance	80	220	680	µF
L	Inductance	6.8	10	22	µH
$R_{SNS1/2}$	Current Sensing Resistor		16		mΩ
f_{SW}	Operating frequency range	80	120	600	kHz
T_J	Operating junction temperature	-40		125	°C

(1) The recommend operation conditions are based on 5V3A dual outputs application.

7.4 Electrical Characteristic

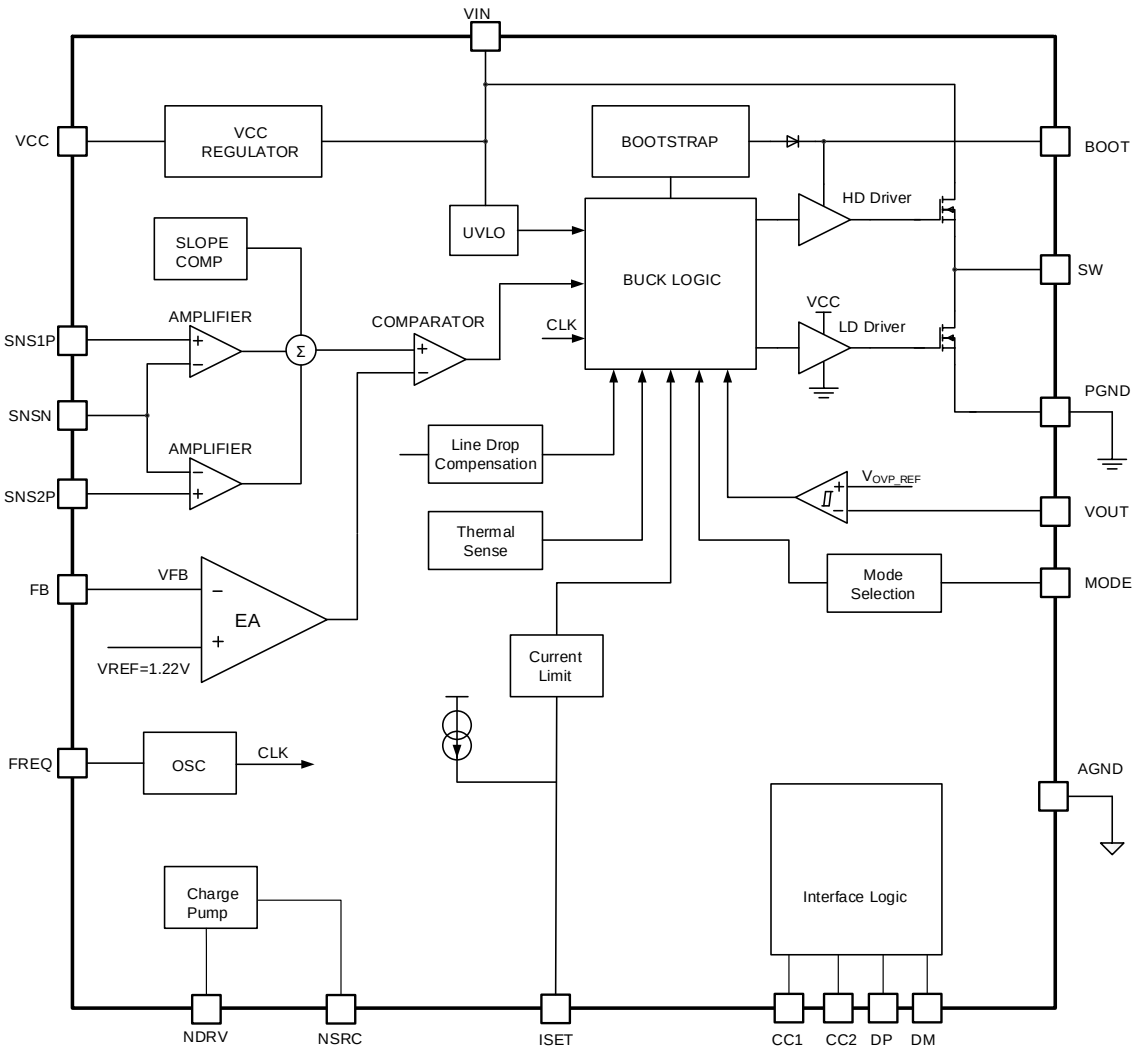
T_J= 25°C and V_{IN} = 12V, V_{OUT} = 5.05V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Operating voltage		4.6		36	V
V_{IN_UVLO}	Under voltage lockout threshold	Rising edge			4.2	V
		Falling edge		4.0	4.1	V
I_Q	Quiescent current into VIN	EN= high, no switching		100		μA
I_{SD}	Shutdown current into VIN	EN = low		3	5	μA
OUTPUT						
V_{OUT}	Operating voltage		3		36	V
		FB connected to GND	5.05	5.10	5.15	V
V_{FB_REF}	FB reference voltage		1.208	1.22	1.232	V
V_{Line_Drop}	Line drop compensation	I_{OUT} = 2.4A, RSNS=20mΩ		120	140	mV
VCC AND DRIVER						
V_{CC}	VCC clamp voltage		4.9	5.2	5.5	V
I_{VCC_LIM}	VCC current limit	V_{CC} = 5.2V	100			mA
R_{HD_pu}	High side driver pull up resistor			10.0		Ω
R_{HD_pd}	High side driver pull down resistor			2.0		Ω
R_{LD_pu}	Low side driver pull up resistor			5.0		Ω
R_{LD_pd}	Low side driver pull down resistor			1.5		Ω
DT1	Dead time for HD off to LD on	V_{CC} = 5.2V		25		ns
DT2	Dead time for LD off to HD on	V_{CC} = 5.2V		25		ns
$I_{NMOS(ON)}$	Isolated NMOS on state current		10			μA
$I_{NMOS(OFF)}$	Isolated NMOS off state current		10			μA
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	VCC=5.2V		27		mΩ
	Low-side MOSFET on-resistance	VCC=5.2V		11		mΩ
CURRENT LIMIT						
I_{LIM_Peak}	Internal peak current limit		10			A
V_{LIM_OUT}	Output current limit threshold	RSNS=20mΩ	54.4	56	58.6	mV
SWITCHING FREQUENCY						
f_{SW}	Switching frequency		80		600	kHz
		R_{FREQ} = Floating		120		kHz
SOFT START						
t_{SS}	Internal soft-start time	VOUT from 10% to 90%		5	8	ms
BC1.2 DCP MODE						
R_{DPM_short}	DP/DM short resistor		5	10	20	Ω
R_{DCHG_PM}	DP/DM discharge resistor to GND		350	650	1100	kΩ
DIVIDER MODE						
$V_{DP\_divider}$	DP output voltage		2.7	2.75	2.8	V
$V_{DM\_divider}$	DM output voltage		1.9	2.05	2.1	V

$Z_{DP\_divider}$	DP output impedance		24	30	36	kΩ
$Z_{DM\_divider}$	DM output impedance		24	30	36	kΩ
1.2V/1.2V MODE						
$V_{DPM\_1.2V}$	DP/DM output voltage		1.1	1.2	1.3	V
$Z_{DP\_1.2V}$	DP output impedance		70	100	130	kΩ
$Z_{DM\_1.2V}$	DM output impedance		70	100	130	kΩ
TYPE-C CC CURRENT MODE						
I_{CCx_Source}	CCx pin 3A mode pull up current		303.6	330	356.4	μA
t_{DB_attach}	CCx pin attach debounce time		100		200	ms
t_{DB_detach}	CCx pin detach debounce time		10		20	ms
t_{VOUT_ON}	The time from CC attached to VOUT reaches 5V				275	ms
t_{VOUT_OFF}	The time from CC detached to VOUT reaches 0V				650	ms
R_{DISC}	Type-C port discharge resistor	VOUT=5V		1.5		kΩ
LOGIC CONTROL						
V_{MODE_L}	MODE logic low voltage		0.4			V
V_{MODE_H}	MODE logic high voltage				1.2	V
PROTECTION						
OVP	Output over voltage protection	FB connected to feedback network	109%	110%	111%	
		FB connected to GND	5.5	5.55	5.61	V
V_{HICP}	Hiccup trigger threshold voltage			2.0		V
T_{HICP_ON}	On time of Hiccup Mode	VOUT<2.0V	15	20	25	ms
T_{HICP_OFF}	Off time of Hiccup Mode	VOUT<2.0V	400	500	600	ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature (1)			165		°C
	Thermal shutdown hysteresis (1)			15		°C

(1) Guarantee by design

8 Functional Block Diagram



9 Detailed Description

The SC8102A is a dual-output synchronous buck converter with a wide input voltage range. The SC8102A is configured to provide a fixed 5-V or customized output voltage programmed by FB pin. Each channel offers max 3A continuous output capacity with ±5% current limit accuracy.

The SC8102A operates in a fixed frequency current mode control to regulate the output voltage in Constant Voltage (CV) mode. If output current reaches its limit, the SC8102A enters Constant Current (CC) mode while output voltage drops. If the output current still goes larger, SC8102A enters hiccup as short circuit protection when output voltage is lower than 2V. The SC8102A adopts fixed line compensation and programmable operating frequency for different user's application. The internal loop compensation simplifies the design process and save the external components. The SC8102A works in PFM mode. In this operation mode, high efficiency can be achieved in light load condition.

The SC8102A works in two different modes: PFM and PWM mode. In PFM mode, high efficiency can be achieved in light load condition. In PWM mode, the switching frequency is same both for light load and heavy load conditions and output ripple can be reduced.

For the Type-C output port, SC8102A integrates the isolated NMOS gate driver, which can provide less power loss on the path and lower price for MOSFET selection.

9.1 Feature Description

9.1.1 Enable and Startup

The SC8102A integrates an internal circuit that controls the ramp up of output voltage during start-up and prevents the converter from the large inrush current. During the startup phase, the internal soft-start circuit increases the voltage on FB pin gradually so that the output voltage slope follows the FB pin voltage slope until the target voltage is reached.

9.1.2 Mode Selection

The SC8102 integrates two different operating modes: PWM mode and PFM mode.

In PWM mode, SC8102 always works in constant frequency for the whole load range, which can achieve the best output voltage performance. The efficiency is low since negative inductor current appears at light load condition.

In power save mode with pulse frequency modulation (PFM), the efficiency can be improved at light load condition while output voltage ripple can be a little larger compared with PWM operation.

9.1.3 Output Voltage Setting

The SC8102A can be configured for two fixed 5.05V output ports with FB pin connected to GND. The output voltage can also be configured for customized values by using external feedback resistors. The FB status is only detected when IC is powered up, so the FB configuration setting is latched and cannot be changed until SC8102A is powered down and restart again.

If alternative output voltage is required, the following equation can be used to calculate the divider resistor.

$$VOUT = V_{FB\_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

Where:

V_{FB_REF} = Internal reference voltage 1.22V

R_{UP} and R_{DWON} = Resistor divider at FB connected to VOUT and AGND.

9.1.4 Line Drop Compensation

The SC8102A is capable of compensating the output voltage drop, caused by a long trace, to keep a fairly constant 5V load-side voltage. The internal comparator compares the voltages across the two sense resistors and selects the larger one to compensate the line drop. This function is enabled when FB pin is connected to AGND

When using default 20mΩ output sensing resistor, the SC8102 provides 44mV/A fixed line drop compensation rate for long cables, as shown in Figure 4. The line drop compensation amplitude increases linearly as the load current increasing.

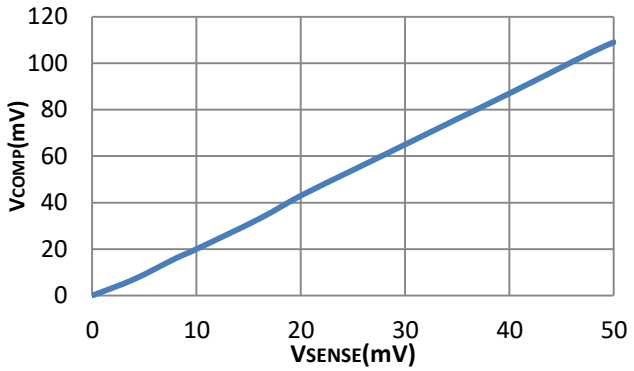


Figure.3 Line Drop Compensation vs. Sensing Voltage

9.1.5 Switching Frequency

he switching frequency can be set by a resistor between FREQ pin and GND. Figure.5 shows the relationship between operating frequency and resistor value.

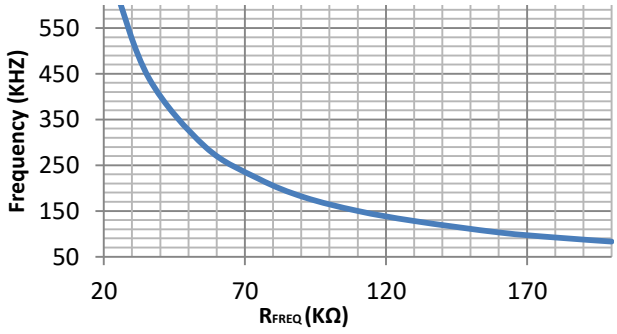


Figure.4 Switching Frequency vs. Setting Resistor

For minimal external components and simplifying the design process, the SC8102A also supports 120-kHz operating frequency if FREQ pin is floating.

9.1.6 Output Power Limit

The output power limit can be set by connecting a resistor between PWR pin and GND. The following table shows the relationship between output power limit and the resistor.

Table.1 Relationship between R-PWR and power limit

R-PWR	56 KΩ	68 KΩ	82 KΩ	100 KΩ	120 KΩ
Pout(typ.)	41W	34W	28W	24W	20W

* The R_PWR must be close to PWR pin to avoid switching noise

The output power limit function helps customer to control the total power delivery of the system. Especially in the application of Quick Charge, the total power delivery should be same even though the VOUT is different. Due to this function, the output current limit can be different according to different output voltage.

9.1.7 Constant Voltage / Constant Current Mode

SC8102A operates either in CV (constant voltage) mode or CC (constant current) mode and automatically changes from CV to CC smoothly. In CV mode, SC8102A regulates the output voltage. As long as output current limit threshold is reached, SC8102A enters CC mode and the output voltage drops while output current is clamped at the setting values.

SC8102A both monitors the two output ports current limit. In case either of the two outputs current reaches setting current limit, SC8102A enters CC mode.

The current limit can be set by the current sensing resistors by the following equation.

$$I_{LIM\_OUT} = \frac{56mV}{RSNS}$$

Where RSNS is the value of current sense resistor.

Usually, the BC1.2 mode limit is set at 2.8A by default with an external sensing resistor RSNS=20mΩ.When the voltage drop cross the sensing resistor gets higher than 56mV , the driver is turned off and in this way, the output current is limited. Table.2 shows some typical RSNS value and output current limit relationship.

RSNS	Output Current Limit
16mΩ	3.5A
20mΩ	2.8A
24mΩ	2.33A
30mΩ	1.87A

Table.2 Relationship between RSNS and current limit

9.1.8 Under-Voltage Lockout (UVLO)

The UVLO function protects the chip from operating at insufficient power supply. The chip disables all the function if input voltage in lower than 4.0V and it doesn't start up again until input voltage is higher than 4.2V.

9.1.9 Output Over-Voltage Protection

SC8102A adopts an output over-voltage protection (OVP) with ±1% accuracy. When FB pin is connected to GND, in case the output voltage is higher than 5.55V, the buck converter stops switching until OVP status is removed. When FB is connected with two divider resistors, OVP is triggered in case the FB voltage is higher than 110% normal reference voltage.

9.1.10 Short Circuit Protection and Hiccup

The SC8102A integrates a hiccup mode which is triggered once the output voltage is lower than 2V. In hiccup mode, SC8102A periodically stops switching for 500ms and then tries to restart with output current increasing to current limit for 20ms. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit condition is removed, SC8102A exits hiccup mode and goes back to normal operation.

9.1.11 Over Temperature Protection

The over temperature protection (OTP) prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165 ℃, SC8102A is shut down. When the temperature drops below threshold (typically 150℃), the chip is enabled again.

10 Application Information

10.1 Input and Output Capacitor Selection

The input current to the Buck converter is discontinuous, therefore the input capacitor should be carefully selected. At least 30μF input capacitor is required for small input voltage ripple and stability. The input capacitor can be electrolytic, tantalum or ceramic. MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60 μF X5R or X7R capacitors with higher voltage rating than operating voltage with margin is recommended. For example, if the highest operating input voltage is 12V, select at least 16V capacitor and to secure enough margin, 25V voltage rating capacitor is recommended. If electrolytic or tantalum capacitor is used, at least 1μF ceramic capacitor must be placed close to IC's VIN pin, to improve the high frequency performance. The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The output capacitor is recommended to be larger than 80μF. The output voltage ripple is estimated as the following equation

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

If electrolytic or tantalum capacitor is used, low ESR capacitor is recommended and 10μF ceramic capacitor is needed in parallel.

10.2 Inductor Selection

For better power limit regulation, a larger inductance is recommend to make sure the system operates in CCM mode at the max load, especially the max VIN and the max VOUT. The min inductance is calculated as follows:

$$L \geq \frac{V_{OUT}}{2I_{OUT} \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so around 10mΩ n DCR is recommended for the first selection. If the current is relatively small, high DCR inductor can be selected. But if switch current is high, just like around 10A, then select the lowest DCR inductor as much as possible because 10mΩ DCR also causes 1W power loss.

The inductor saturation current I_{SAT} should be higher than input / output current with sufficient margin.

10.3 PCB Layout Guide

For best performance, PCB layout should be carefully designed to avoid instability, noise and EMI. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI. For a BUCK converter, the critical loop area is showed in figure 6:

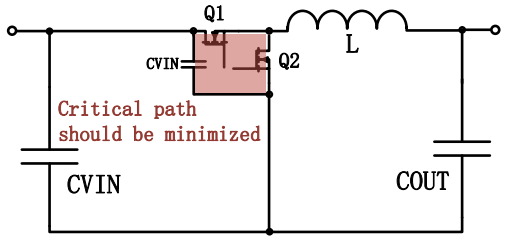


Figure.5 Minimizing the critical path helps mitigate EMI

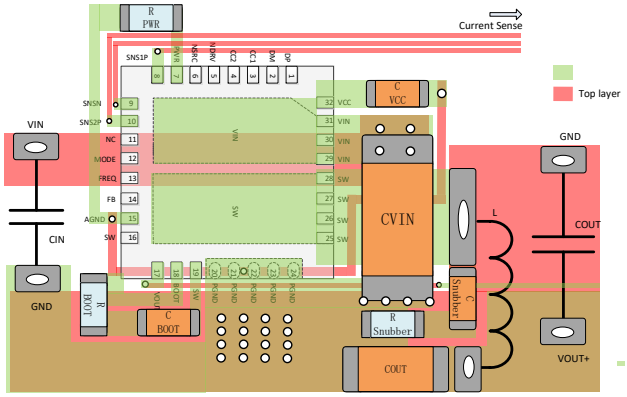


Figure.6 A layout example of SC8102A

Here shows some guidelines for reference:

1) The input capacitor (CVIN, 10uF, MLCC) should be close to IC to minimize the critical path area and make sure the current flows through the CVIN first, then VIN pin.

2) The VCC capacitor (CVCC, 1uF, MLCC) should be close to VCC pin and connected to PGND pin directly, to avoid noise and instability.

3) The power limit resistor and line drop compensation resistor (R-PWR) are sensitive, it should be close to the corresponding pin (keep away from switching node) and connected to AGND pin directly.

4) The FB feedback resistor should be close to FB pin and be away from switching node. A feed-forward capacitor is highly recommended to prevent instability.

5) The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing)

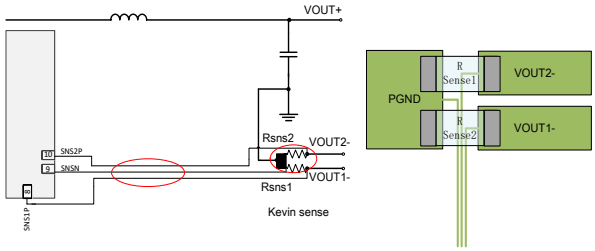


Figure.7 Current sense

6) The RC snubber is connected between SW and PGND to absorb switching noise. The snubber should be close to SW and GND pin and minimize the loop area to optimize EMI.

7) The boot capacitor should be close to SW and BOOT pin

8) The SNSN, AGND and PGND are in the same physical net, be careful when using copper pour.

Here is a reference design:

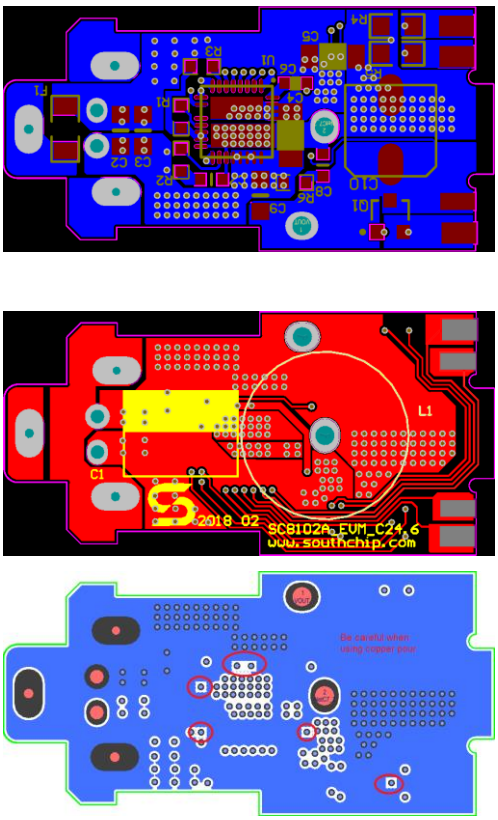
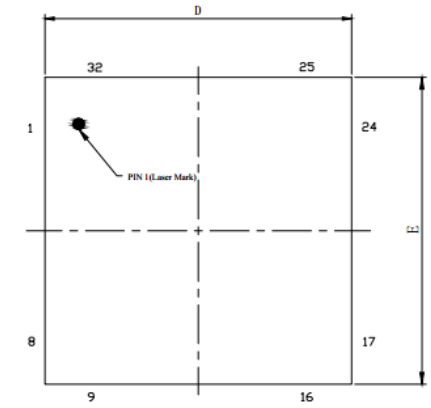


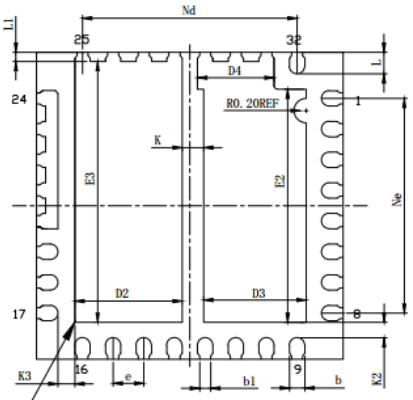
Figure.8 Reference design

Packaging Information

QFN32L(0505x0.75-0.50)

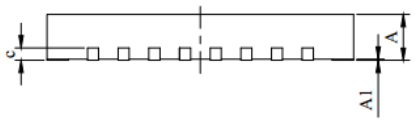


TOP VIEW



BOTTOM VIEW

EXPOSED THERMAL
PAD ZONE



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	4.90	5.00	5.10
D2	1.65	1.75	1.85
D3	1.575	1.675	1.775
D4	1.15	1.25	1.35
e		0.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
E3	4.15	4.25	4.35
Ne		3.50BSC	
L	0.30	0.35	0.40
K	0.30	0.35	0.40
K2	0.20	0.25	0.30
K3	0.225	0.275	0.325
R		0.02REF	