TPS342x 具有可配置延迟的低功耗按钮控制器

1 特性

- 超小型封装：1.45mm x 1.00mm 小外形尺寸无引线 (SON) 封装
- 工作电压范围：1.6V 至 6.5V
- 单 (TPS3422) 或双（TPS3420 和 TPS3421）按钮输入
- 低电源电流： 250nA（典型值）
- 双态逻辑，用户可选输入延迟：
  - 例如：7.5s 和 0s
  - 多个定时选项可用
- $\overline{RST}$ 的固定超时脉冲（TPS3421 和 TPS3422）：400ms（典型值）
  - 按要求可提供其它定时选项
- 低电平有效，开漏输出

2 应用范围

- 智能电话
- 平板电脑, Ultrabooks™
- 游戏控制台
- 便携式消费类产品
- 导航器件
- 消费类医疗产品
- 玩具

3 说明

TPS3420、TPS3421 和 TPS3422 (TPS342x) 是低电流、超小型、按钮式复位定时器。 这些器件使用一个长定时设置延迟来提供所需的系统复位并且避免由短时按钮关闭或按键按压而造成的复位。 这个复位配置还可区分软件终端和硬件系统复位。

TPS3420 和 TPS3421 监控两个输入（PB1 和 PB2）并且在两个输入在所选的时间延迟内都为低电平时输出一个低电平有效复位脉冲信号 ($\overline{RST}$)。 对于 TPS3421，$\overline{RST}$在一个厂家设定的固定时间内保持低电平。 对于 TPS3420，$\overline{RST}$在其中一个 PBx 输入被释放前保持低电平。 由于两个输入被用来确保复位，也就无需一个专用复位按钮了。 TPS3422 监控一个输入 (PB1) 并且在 PB1 在所选的时间延迟内为低电平时输出一个低电平有效复位脉冲信号 ($\overline{RST}$)。

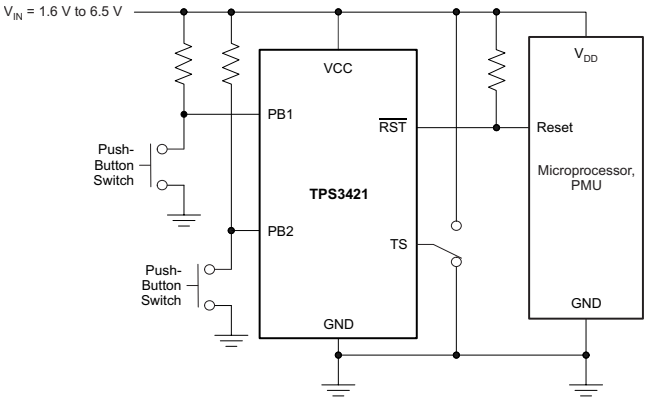
TPS342x 具有一个开漏输出，可与其他开漏器件进行线或连接。 TPS342x 的工作电压范围为 1.6V 至 6.5V，工作温度范围为 -40°C 至 +125°C，并且可提供精准而节省空间的微功耗解决方案以满足系统复位需求。

器件信息(1)

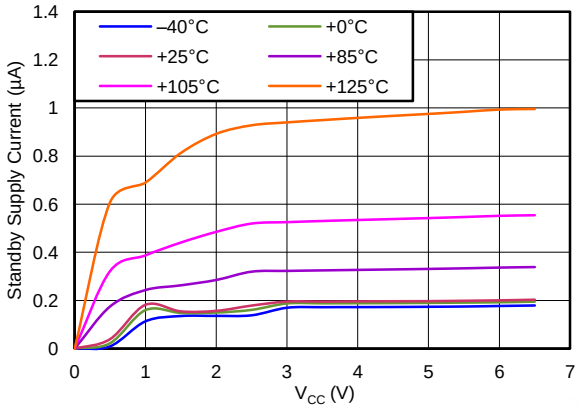
器件型号	封装	封装尺寸（标称值）
TPS342x	USON (6)	1.45mm x 1.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

TPS3421 典型应用图



待机电源电流与电源电压间的关系



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4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B **Page**

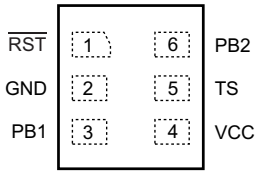
- 已添加 *典型值*至*特性*列表中的*低电源电流*要点 ... 1
- 已添加 *典型值*到*特性*列表中的*固定超时脉冲*要点 ... 1
- Changed *Pin Configuration and Functions* section; updated table format ... 3
- Changed Absolute Maximum Ratings table; added storage temperature range (T_{stg}) specification ... 4
- Changed *Start-up time* to *start-up delay*, added parametric symbol ... 5

Changes from Original (August 2012) to Revision A **Page**

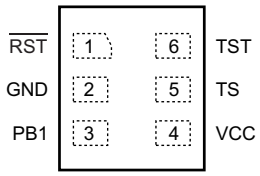
- 已添加 *ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已将数据表从产品预览更改为量产数据 ... 1

5 Pin Configuration and Functions

TPS3420, TPS3421: DRY Package
6-Pin USON
Top View



TPS3422: DRY Package
6-Pin USON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS3420/21	TPS3422		
GND	2	2	—	Ground.
PB1	3	3	I	Push-button input. PB1 and PB2 must be held low for greater than t_{TIMER} time to assert the reset output.
PB2	6	—	I	Second push-button input. PB1 and PB2 must be held low for greater than t_{TIMER} time to assert the reset output.
$\overline{RST}$	1	1	O	Active low, open-drain output. Reset is asserted (goes low) when both PB1 and PB2 are held low for longer than t_{TIMER} time (only PB1 for TPS3422). For TPS3420: Reset is deasserted when either PBx input goes high. For TPS3421,TPS3422: Reset is deasserted after fixed time of t_{RST}.
TS	5	5	I	Time delay selection input. Connect to VCC or GND for different t_{TIMER} selections. In normal operation, the TS pin state should not be changed because it is intended to be permanently connected to either GND or VCC. If switching the TS pin is required, it should be done during power off, or when either PBx input is high.
TST	—	6	—	Connect this pin to GND or VCC during normal device operation.
VCC	4	4	I	Supply voltage input. Connect a 1.6-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VCC	–0.3	7	V
	$\overline{RST}$	–0.3	7	
	PB1, PB2	–0.3	7	
	TS	–0.3	V_{CC} + 0.3	
Current	$\overline{RST}$ pin	–20	20	mA
Temperature (2)	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input supply voltage	1.6		6.5	V
V_{TS}	TS pin voltage	0		V_{CC}	V
V_{PB1}, V_{PB2}	PB1 and PB2 pin voltage	0		6.5	V
V_{RST}	RST pin voltage	0		6.5	V
I_{RST}	RST pin current	0.00035		8	mA

6.4 Thermal Information

THERMAL METRIC (1)		TPS342x DRY (USON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	322	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1185.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.7	
ψ_{JT}	Junction-to-top characterization parameter	34.9	
ψ_{JB}	Junction-to-board characterization parameter	182.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	69.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All specifications are over the operating temperature range of –40°C < T_J < 125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input supply			1.6		6.5	V
I_{CC}	Supply current (standby)	TPS3421, TPS3422	V_{CC} = 3.3 V		250		nA
			V_{CC} = 6.5 V, –40°C < T_J < 85°C			1	µA
			V_{CC} = 6.5 V			3.3	µA
		TPS3420	V_{CC} = 3.3 V		350		nA
			V_{CC} = 6.5 V, –40°C < T_J < 85°C			1.2	µA
			V_{CC} = 6.5 V			3.4	µA
	Supply current (active timer)(1)	TPS3420, TPS3421	PB1, PB2 = 0 V, V_{CC} = 6.5 V		6	12	µA
		TPS3422	PB1, PB2 = 0 V, V_{CC} = 6.5 V		106	136	
V_{IH}	High-level input voltage	TPS3421, TPS3422	PB1, PB2	0.7 V_{CC}			V
		TPS3420	PB1, PB2	0.85			
V_{IL}	Low-level input voltage	TPS3421, TPS3422	PB1, PB2	0		0.3 V_{CC}	V
		TPS3420	PB1, PB2	0		0.3	
R_{PB1}	PB1 internal pullup resistance (TPS3422)				65		kΩ
I_{PB}	Input current (PB1, PB2)	TPS3420 TPS3421	PB1, PB2 = 0 V or V_{CC}	–50		50	nA
		TPS3422	PB1, PB2 = V_{CC}	–50		50	
V_{OL}	Low-level output voltage		V_{CC} ≥ 4.5 V, I_{SINK} = 8 mA			0.4	V
			V_{CC} ≥ 3.3 V, I_{SINK} = 5 mA			0.3	
			V_{CC} ≥ 1.6 V, I_{SINK} = 3 mA			0.3	
$I_{lkg(OD)}$	Open-drain output leakage current		High impedance, V $\overline{RST}$ = 6.5 V	–0.35		0.35	µA

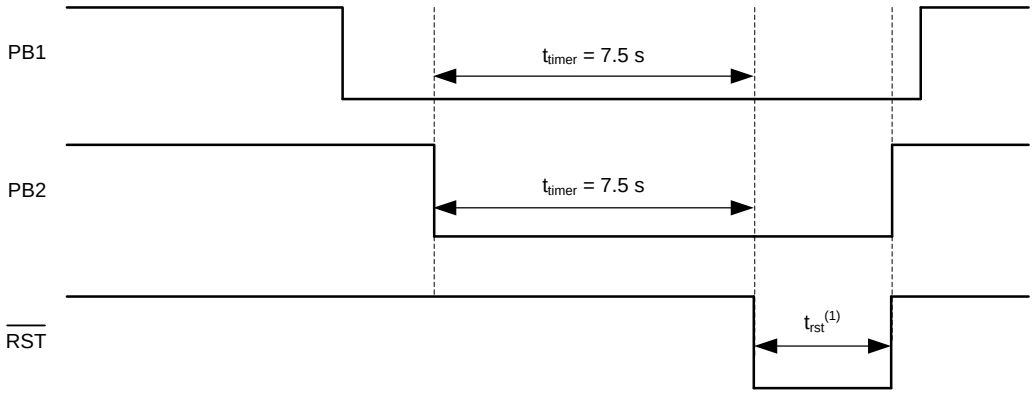
(1) Includes current through pullup resistor between input pin (PB1) and supply pin (VCC) for TPS3422.

6.6 Timing Requirements

All specifications are over the operating temperature range of –40°C < T_J < 125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3 V.

			MIN	TYP	MAX	UNIT
t_{TIMER}	Push-button timer(1)		–20%		20%	s
		TPS3420D: TS = GND	6	7.5	9	
		TPS3420D: TS = VCC	10	12.5	15	
		TPS3421Ey, TPS3422Ey: TS = GND	6	7.5	9	
		TPS3421Ey, TPS3422Ey: TS = VCC		0		
t_{RST}	Reset pulse duration		–20%		20%	ms
		TPS3421xC	64	80	96	
		TPS3421xG	320	400	480	
		TPS3422xG	320	400	480	
t_{DD}	Detection delay (from input to $\overline{RST}$)(2)	For 0-s t_{TIMER} condition		150		µs
t_{SD}	Start-up delay(2)	VCC rising		300		µs

(1) For devices with a 0-second delay while TS = VCC, this option is only for factory testing and is not intended for normal operation. In normal operation, the TS pin should be tied to GND.
(2) For devices with a 0-second delay when TS = VCC, reset asserts in t_{DD} time when both PB inputs go low in this configuration. During start-up, if the PB inputs are low, reset asserts after a start-up time delay. This value is specified by design.



(1) For the TPS3420, t_{RST} is not a fixed time, but instead depends on one of the PB pins going high.

Figure 1. TPS3420 Timing Diagram

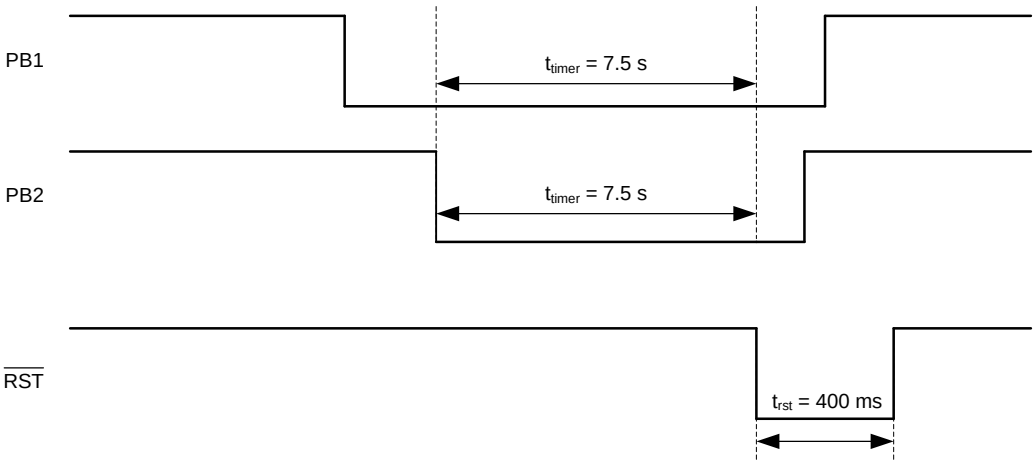


Figure 2. TPS3421 Timing Diagram

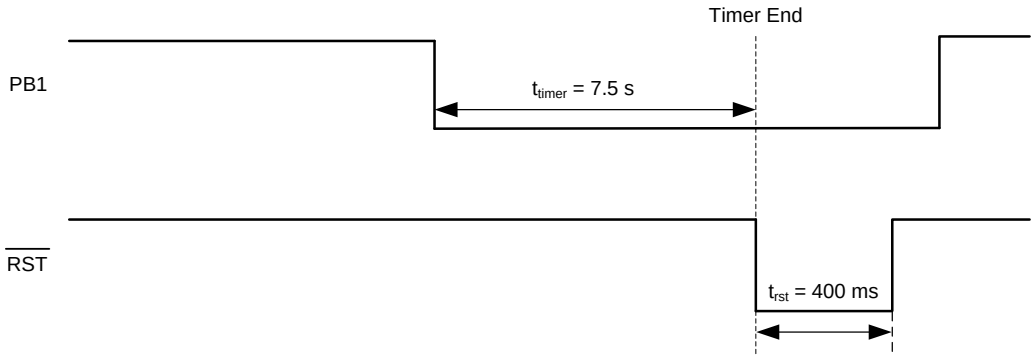


Figure 3. TPS3422 Timing Diagram

6.7 Typical Characteristics

At T_J = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

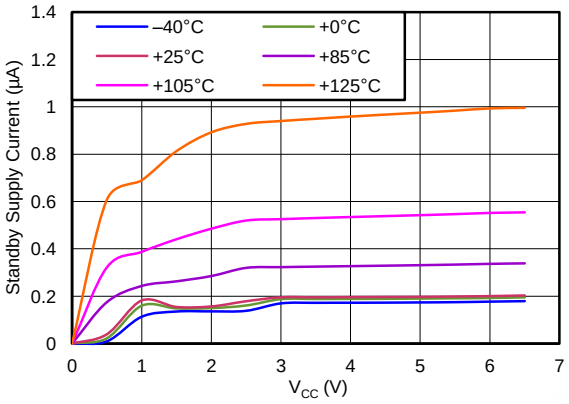


Figure 4. TPS3421: Standby Supply Current vs Supply Voltage

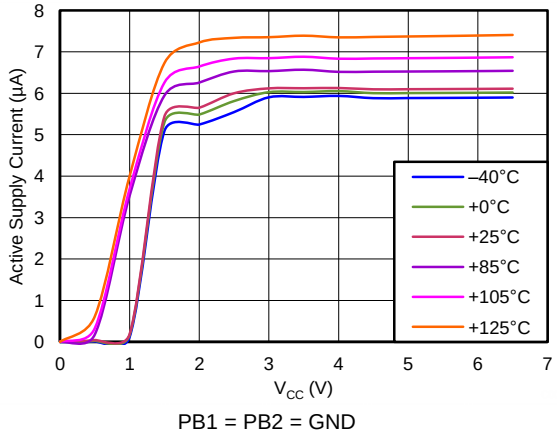


Figure 5. TPS3421: Active Supply Current vs Supply Voltage

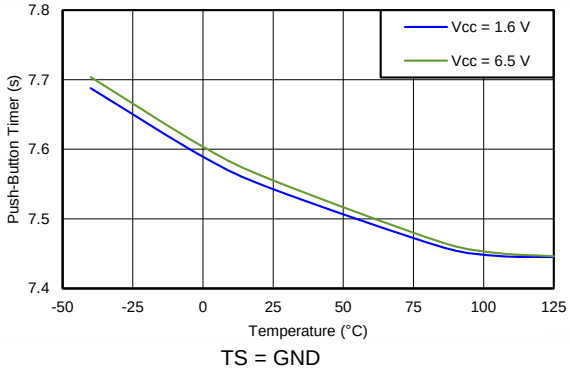


Figure 6. Push-Button Timer vs Temperature

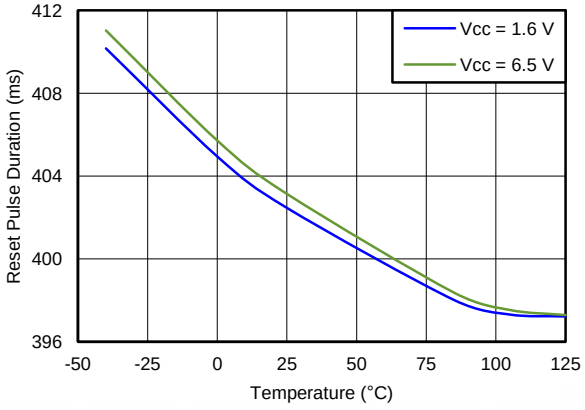


Figure 7. Reset Pulse Duration vs Temperature

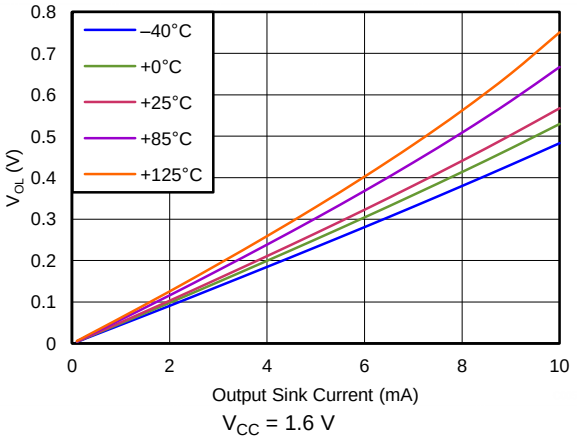


Figure 8. Output Voltage Low vs Output Sink Current

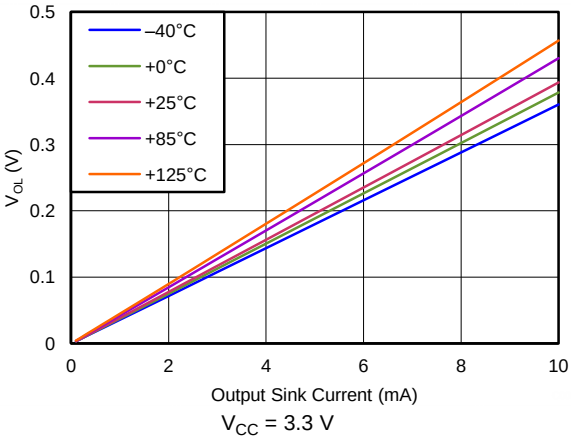


Figure 9. Output Voltage Low vs Output Sink Current

Typical Characteristics (continued)

At T_J = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

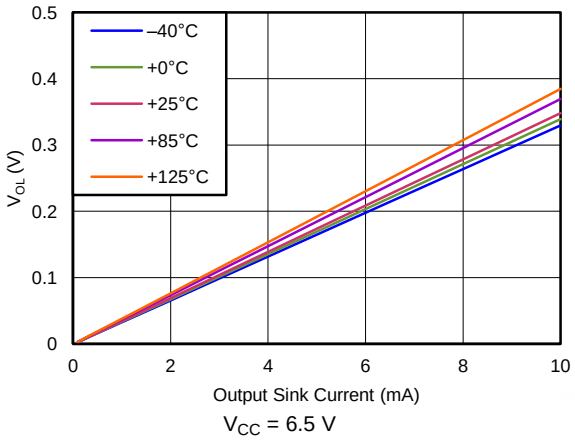


Figure 10. Output Voltage Low vs Output Sink Current

7 Detailed Description

7.1 Overview

The TPS342x are a family of push-button reset devices with an extended setup period that prevents resets from occurring as a result of short-duration switch closures. See Table 1 for details.

The TPS3420 is a dual-channel device with an output that asserts when both inputs (PB1 and PB2) are held low for the push-button timer duration, and deasserts when either input PBx is released.

The TPS3421 is a dual-channel device with an output that asserts when both inputs (PB1 and PB2) are held low for the push-button timer duration, and deasserts after the reset time-out duration.

The TPS3422 is a single-channel device with an output that asserts when the PB1 input is held low for the push-button timer duration, and deasserts after the reset time-out duration.

The TPS342x family also has a TS pin that selects between two different push-button timing options by connecting the pin to either GND or V_{CC}.

Table 1. Device Family Options

DEVICE	CHANNELS	INPUT	RESET BEHAVIOR (DEASSERTION)
TPS3420	2	NMOS-based threshold	Input (PBx) dependent
TPS3421	2	External pullup to VCC	Fixed pulse
TPS3422	1	Internal pullup	Fixed pulse

7.2 Functional Block Diagrams

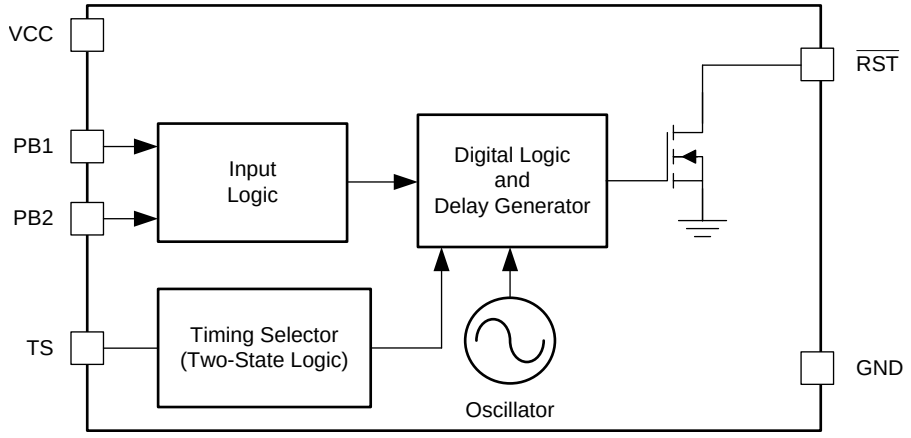


Figure 11. TPS3420 Block Diagram

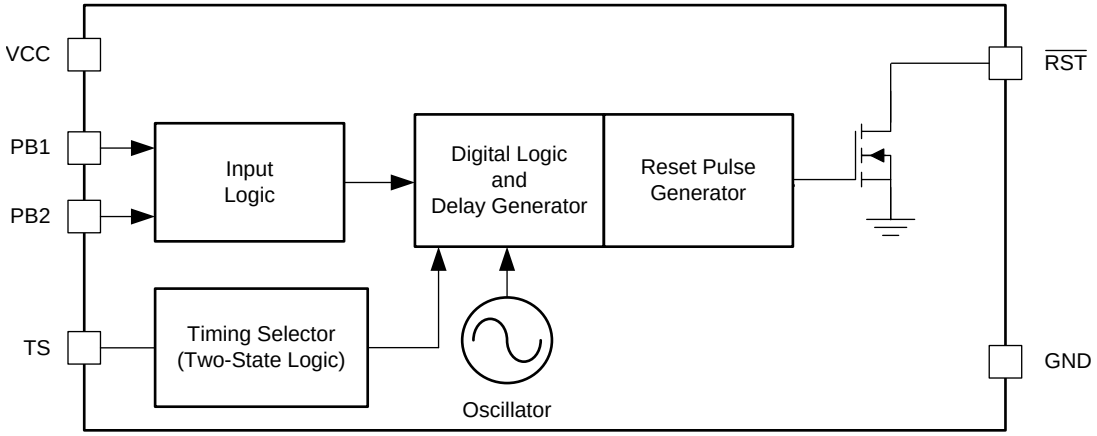


Figure 12. TPS3421 Block Diagram

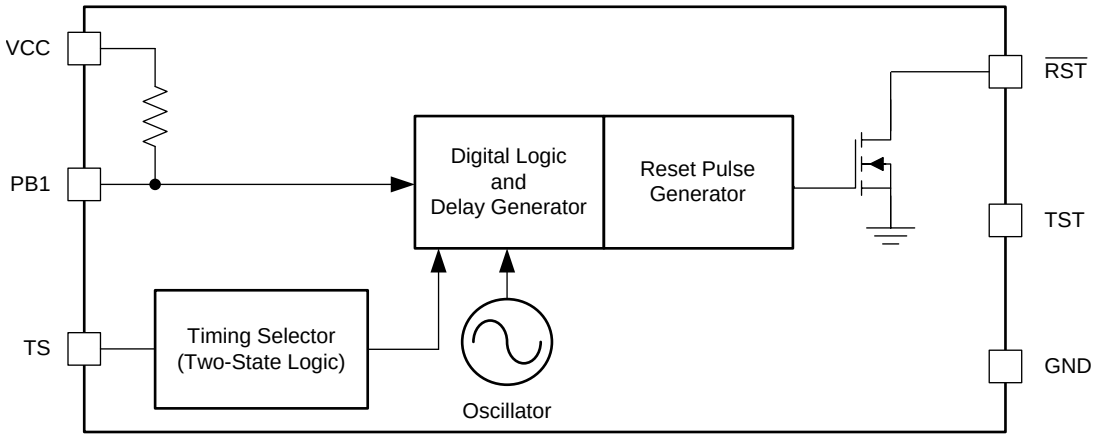


Figure 13. TPS3422 Block Diagram

7.3 Feature Description

7.3.1 Push-Button Timer Selection (TS)

The TPS342x offer two different push-button timer options (t_{TIMER}) for system flexibility with the use of the TS pin. Connect the TS pin to either GND or VCC for two different timing options, as shown in Table 2.

Table 2. Push-Button Timer Option Examples

PRODUCT	PUSH-BUTTON TIMER		RESET PULSE
	TS = VCC	TS = GND	
TPS3420DDRYR/T	12.5 s	7.5 s	N/A
TPS3421EGDRYR/T	0 s	7.5 s	400 ms
TPS3422EGDRYR/T	0 s	7.5 s	400 ms

During normal operation, the TS pin state should not be changed because TS is intended to be permanently connected to either ground or VCC. The state of the TS pin is checked during power up and when either PBx input is high. Therefore, if a different timing option is desired, the state must be changed during power off, or when either PBx input is high, to avoid false operation.

7.3.2 Inputs

This section discusses the inputs of the TPS342x devices.

7.3.2.1 TPS3420 Inputs (PB1, PB2)

The TPS3420 has two NMOS-based threshold inputs (PB1, PB2) with a $V_{IH} \geq 0.85$ V, and a $V_{IL} \leq 0.3$ V. When input conditions are met (that is, when both inputs are simultaneously held low for the push-button timer period, t_{TIMER}), the device asserts a reset low, as shown in Figure 1. Reset deassertion occurs when either input goes high. The reset pulse occurs only one time after each valid input condition. At least one input pin must be released (goes high) and then driven low for the t_{TIMER} period before $\overline{RST}$ asserts again.

7.3.2.2 TPS3421 Inputs (PB1, PB2)

The TPS3421 has two inputs: PB1 and PB2. External pullup resistors to VCC are required to pull the input pins high. When input conditions are met (that is, when both inputs are held low simultaneously for the push-button timer period, t_{TIMER}), the device asserts a single reset pulse of a fixed time (t_{RST}); see Figure 2. Reset deassertion is independent of the inputs because t_{RST} is a fixed time pulse. A reset pulse occurs only one time after each valid input condition. At least one input pin must be released (go high) and then driven low for the t_{TIMER} duration before $\overline{RST}$ asserts again.

7.3.2.3 TPS3422 Inputs (PB1)

The TPS3422 has only one input: PB1. This input has an internal pullup resistor to V_{CC}. When input conditions are met (that is, when the input is held low for the push-button timer period, t_{TIMER}), the device asserts a single reset pulse of a fixed time (t_{RST}); see Figure 3. Reset deassertion is independent of the input because t_{RST} is a fixed time pulse. A reset pulse occurs only one time after each valid input condition. The input pin must be released (go high) and then driven low for the t_{TIMER} period before $\overline{RST}$ asserts again.

7.3.3 Output ($\overline{RST}$)

The TPS342x have an open-drain output. A pullup resistor must be used to hold the line high when the output is in a high-impedance state (not asserted). By connecting a pullup resistor to the proper voltage rail, the output can be connected to other devices at correct interface voltage levels. The TPS342x output can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pullup resistor values. The pullup resistor value is determined by V_{OL}, sink current capability, and output leakage current ($I_{lkg(OD)}$). These values are specified in *Electrical Charactersitcs*.

The *Inputs (PB1, PB2)* describes how the output is asserted or deasserted. See Figure 1 (TPS3420), Figure 2 (TPS3421), or Figure 3 (TPS3422) for a timing diagram that describes the relationship between the PB1 and PB2 inputs and the output. Figure 14 shows the TPS3421 reset timing.

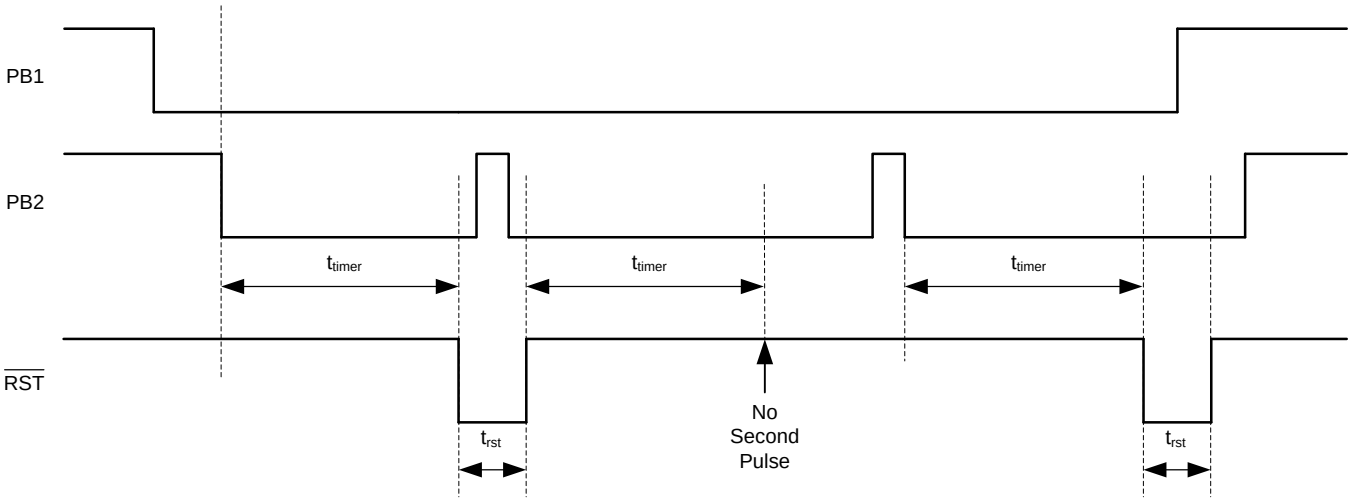


Figure 14. TPS3421 Reset Timing Diagram

Any change in input condition is detected after reset is deasserted. If input PB1 or PB2 has a pulse (low-to-high-to-low) during the t_{RST} period, the change is not recognized by the device. If input PB1 or PB2 go high during the t_{RST} period, the change is detected after reset is deasserted.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > 1.6 V)

When the voltage on VDD is greater than 1.6 V ($V_{DD(min)}$) for approximately 300 µs (t_{SD}), the $\overline{RST}$ signal corresponds to the state of the PB1 and PB2 pins; see Table 1.

7.4.2 Below $V_{DD(min)}$ (1.6 V > V_{DD} > 1.3 V)

When the voltage on VDD is less than 1.6 V but greater than 1.3 V (typical), the $\overline{RST}$ signal corresponds to the state of the PB1 and PB2 pins; however, the electrical specifications in the *Electrical Characteristics* and *Timing Requirements* tables do not apply when $V_{DD} < V_{DD(min)}$.

7.4.3 Power-On Reset (V_{DD} < 1.3 V)

When the voltage on VDD is lower than 1.3 V (typical), the $\overline{RST}$ output should be high-impedance. However, it is not ensured to be in a high impedance state under all conditions.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS342x family of devices are small, low-current, push-button reset timers. These devices use a long timing setup delay to provide the system reset signals, and avoid resets from short push-button closures. This reset configuration allows for differentiation between user inputs and hard system resets. TPS342x uses an open drain output, has an input voltage range of 1.6 V to 6.5 V, and is specified from –40°C to +125°C.

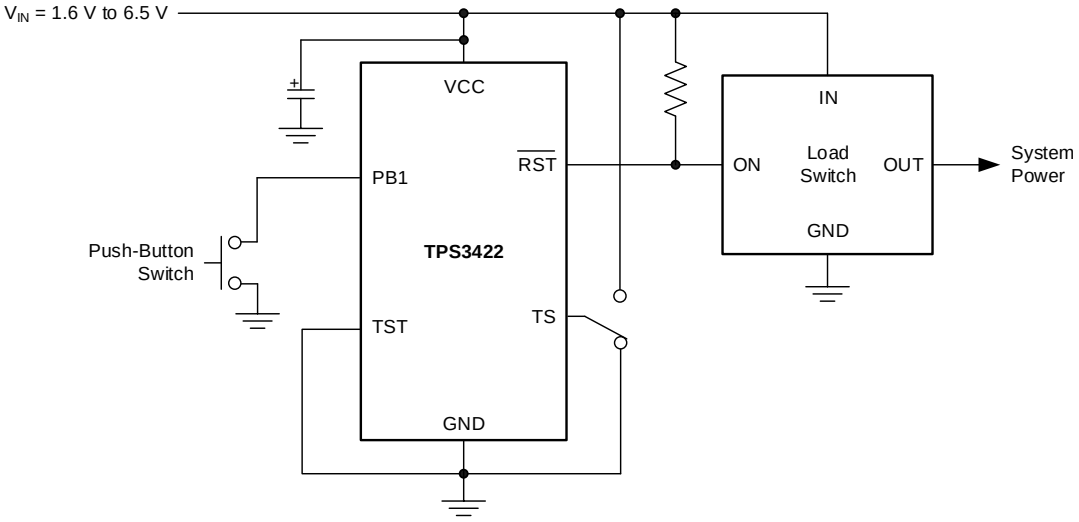
The TPS3420 and TPS3421 are used to monitor two inputs while TPS3422 is used to monitor a single input.

8.2 Typical Applications

8.2.1 Single Input With Fixed Reset Pulse Duration

If only one input must be monitored to set the state of a logic pin, such as the enable pin of a load switch, use the TPS3422. After a reset event has occurred, $\overline{RST}$ is held low for a fixed amount of time (t_{RST}) regardless of the state of the PB1 pin.

An application diagram is shown in Figure 15.



A. Connect TS to VCC or ground for different PB time delays.

Figure 15. TPS3422 Application Diagram

8.2.1.1 Design Requirements

Table 3 lists the design requirements for Figure 15.

Table 3. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT
Single input	PB1
Does not react to input signal less than 5 s	6 s (minimum)
Reset pulse greater than 240 ms	320 ms (minimum)
I_{CC} < 5 µA	3.3 µA (maximum)

8.2.1.2 Detailed Design Procedure

When the output switches to the high-*Z* state, the rise time of the $\overline{RST}$ node depends on the pullup resistance and the capacitance on that node. Choose pullup resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 1-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

8.2.1.3 Application Curve

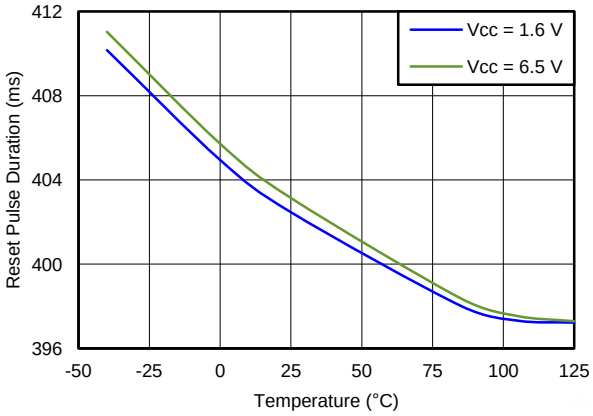
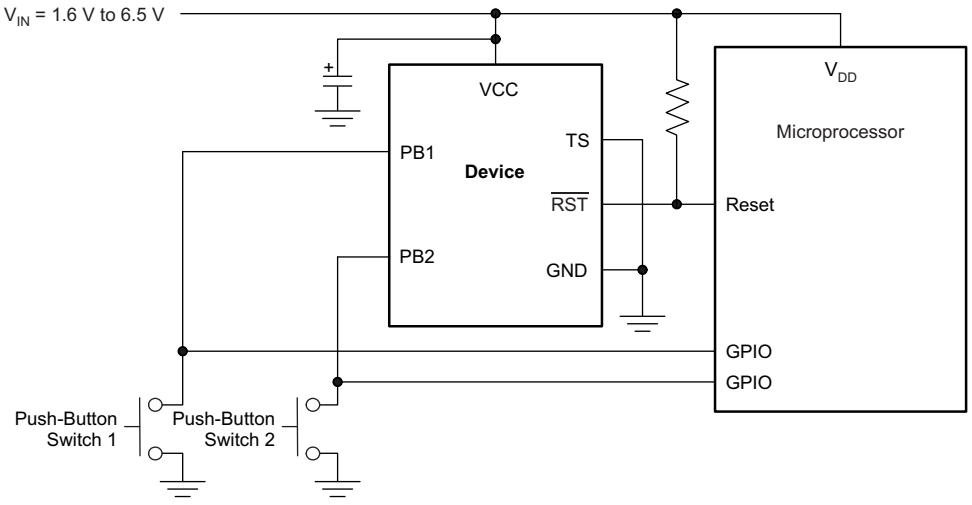


Figure 16. Reset Pulse Duration vs Temperature

8.2.2 Dual Input Applications

If two inputs must be monitored to set the state of a microprocessor reset pin, either the TPS3420 or the TPS3421 can be used. The system functionality determines which device to use. Use the TPS3420 if $\overline{RST}$ must be held low until the signal on one of the PBx pins transitions to a logic high state. Use the TPS3421 if $\overline{RST}$ should only be held low for a fixed amount of time (t_{RST}) regardless of the state of the PBx pins.

An application diagram that is suitable for either the TPS3420 and the TPS3421 is shown in Figure 17.



A. Connect TS to VCC or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

Figure 17. TPS3420 or TPS3421 Application Diagram

8.2.2.1 Design Requirements

Table 4 lists the design requirements for Figure 17.

Table 4. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT	
	TPS3420	TPS3421
Dual input	PB1 and PB2	PB1 and PB2
Does not react to input signal less than 5 s	6 s (minimum)	6 s (minimum)
Reset pulse greater than 140 ms	Depends on PBx timing	320 ms (minimum)
Reset pulse ends after at least one input goes high	True	Does not depend on PBx timing

8.2.2.2 Detailed Design Procedure

Determine which version of the TPS342x family best suits the functional performance required.

When the output switches to the high-*Z* state, the rise time of the $\overline{RST}$ node depends on the pullup resistance and the capacitance on that node. Choose pullup resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 1-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

8.2.2.3 Application Curve

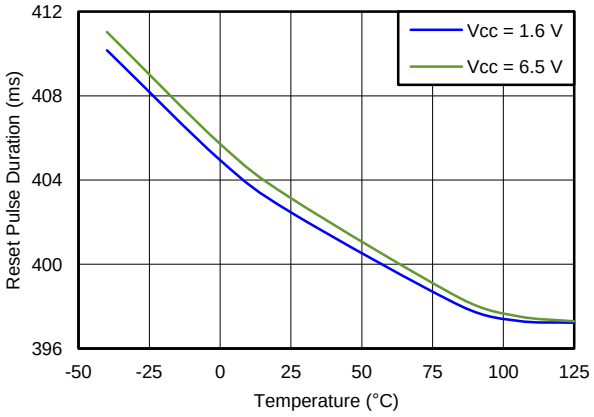


Figure 18. Reset Pulse Duration vs Temperature

8.2.3 Latched Reset Signal

Some applications require the reset signal ($\overline{RST}$) to be latched and only change state after a second low input signal is received. To achieve a latched version of the $\overline{RST}$ signal, a D-flip-flop can be used. The output of the D-flip-flop, *Q*, is then connected to the device to be reset.

See Figure 19 for an example of a latched reset signal configuration.

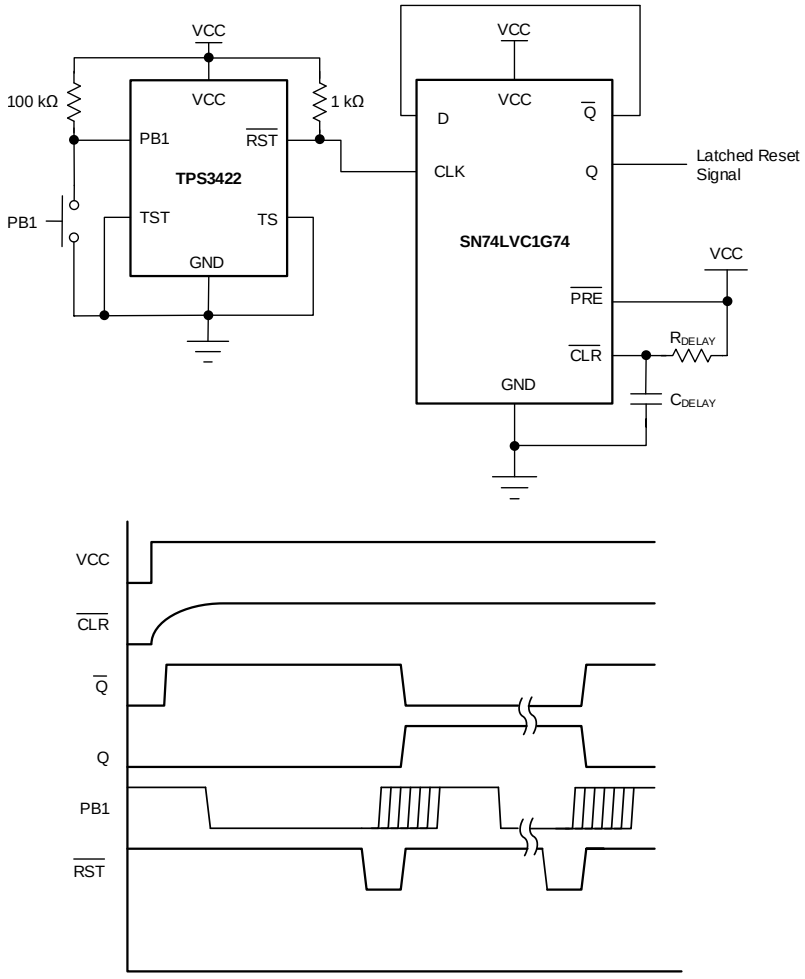


Figure 19. Latched Reset Schematic and Timing Diagram

8.2.3.1 Design Requirements

Table 5 summarizes the design requirements for Figure 19.

Table 5. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT
Single input	PB1
Latched output	Q
Does not react to input signal less than 5 s	6 s (minimum)
Reset pulse greater than 200 ms	320 ms (minimum)
I_{CC} < 20 µA	13.3 µA (maximum)

8.2.3.2 Detailed Design Procedure

Once a positive-edge triggered D-flip-flop is chosen, make sure the slew rate of the $\overline{RST}$ signal is fast enough to trigger the flip-flop. For the SN74LVC1G74 shown in Figure 19, TI recommends a 1-kΩ pullup resistor. The RC time constant of the delay cap (C_{DELAY}) and delay resistor (R_{DELAY})should be 10 times the rise time of the input voltage to VCC so that a clear signal is sent to the D-flip-flop, to initialize it into a known state.

8.2.3.3 Application Curve

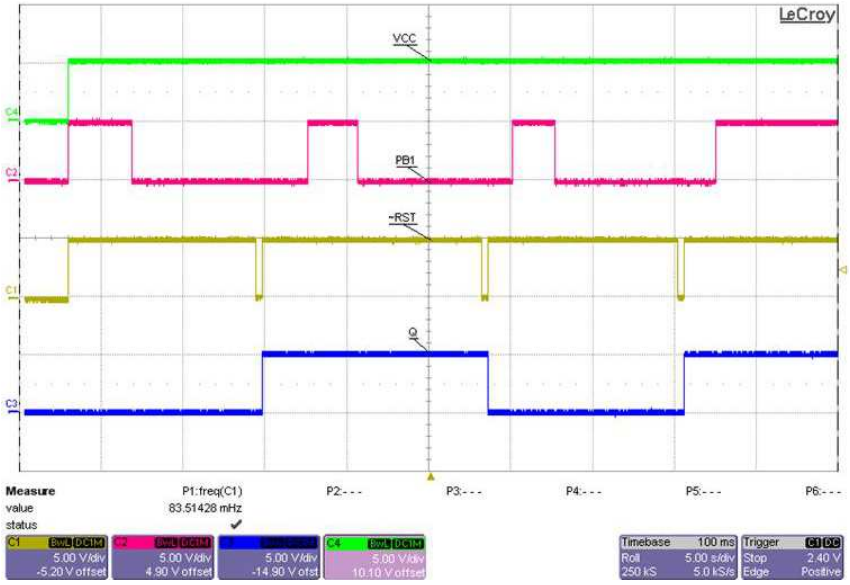


Figure 20. Latched Reset Waveforms Using SN74LVC1G74

9 Power Supply Recommendations

The input power supply should range from 1.6 V to 6.5 V and should be well regulated. Though not required, it is good analog design practice to place a 0.1-µF ceramic capacitor close to the VCC pin.

10 Layout

10.1 Layout Guidelines

Follow these guidelines for laying out the printed circuit board (PCB) that is used for the TPS342x.

- Place the VCC decoupling capacitor close to the device.
- Avoid using long traces for the VCC supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VCC voltage.

10.2 Layout Example

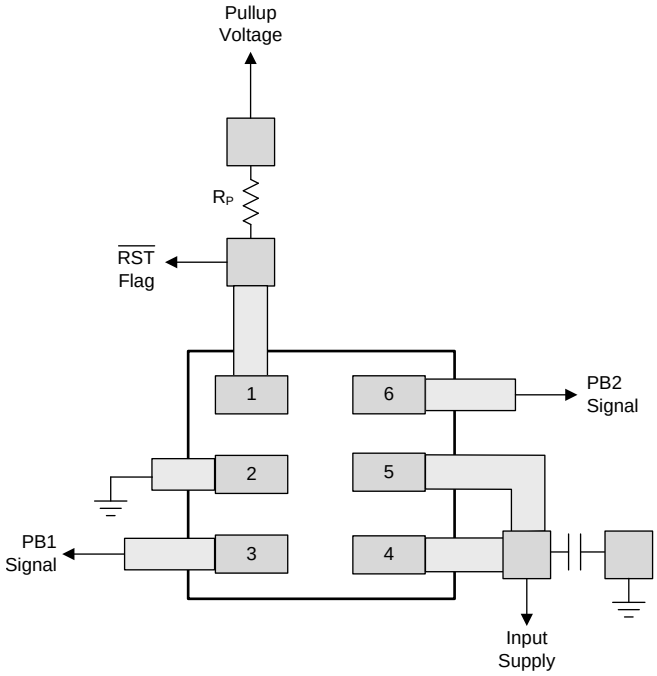


Figure 21. Layout Example (DRY Package)

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS3421EG 配套使用，帮助评估初始电路性能。 TPS3421EGEVM-156 评估模块（和相关的用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。 您可以从产品文件夹中的*工具和软件*下获取 TPS3421EG 的 SPICE 模型。

11.1.2 器件命名规则

表 **6.** 器件命名规则

产品	说明
TPS3420**xzzza** TPS3421**xyzzza** TPS3422**xyzzza**	**x** 为按钮式定时器选项。 **y** 为不同的复位超时脉冲选项。 **zzz** 为封装标识符。 **a** 为卷带数量。

11.2 文档支持

11.2.1 相关文档

- *《TPS3421EGEVM-156 用户指南》*，SLVU781

11.3 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **7.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS3420	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3421	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3422	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 商标

Ultrabooks is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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DLP® 产品	www.dlp.com	能源	www.ti.com/energy
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RFID 系统	www.ti.com.cn/rfidsys		
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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3420DDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3420DDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3421ECDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3421ECDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3421EGDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3421EGDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3422EGDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE	Samples
TPS3422EGDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

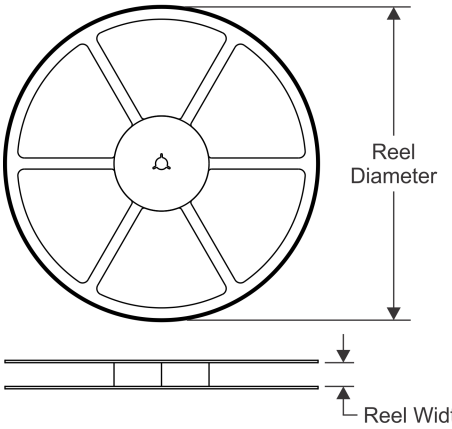
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

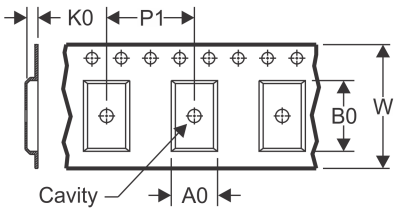
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

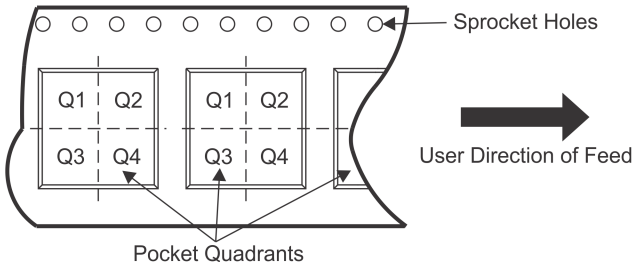


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

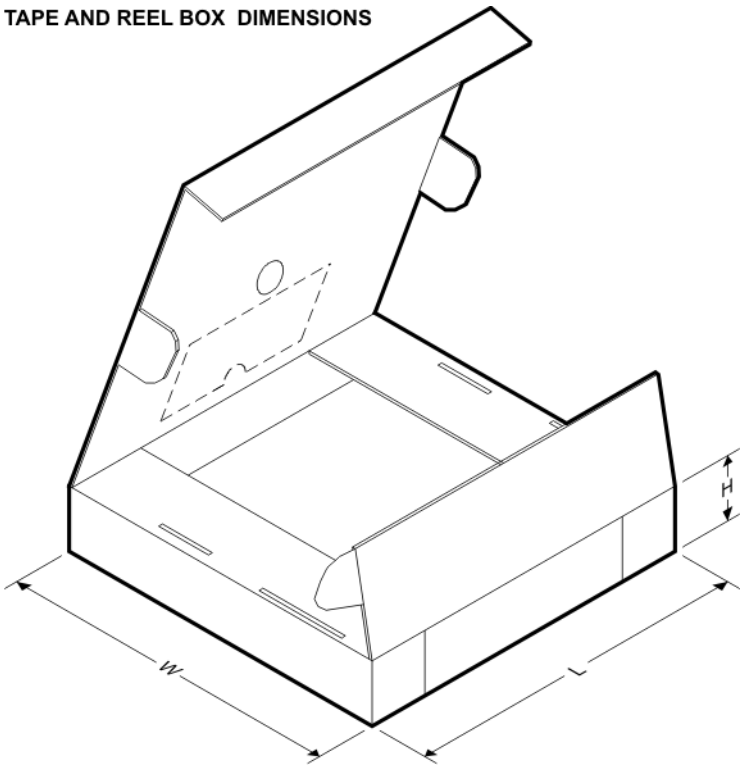
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3420DDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3420DDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421ECDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421ECDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421EGDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421EGDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3422EGDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3422EGDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

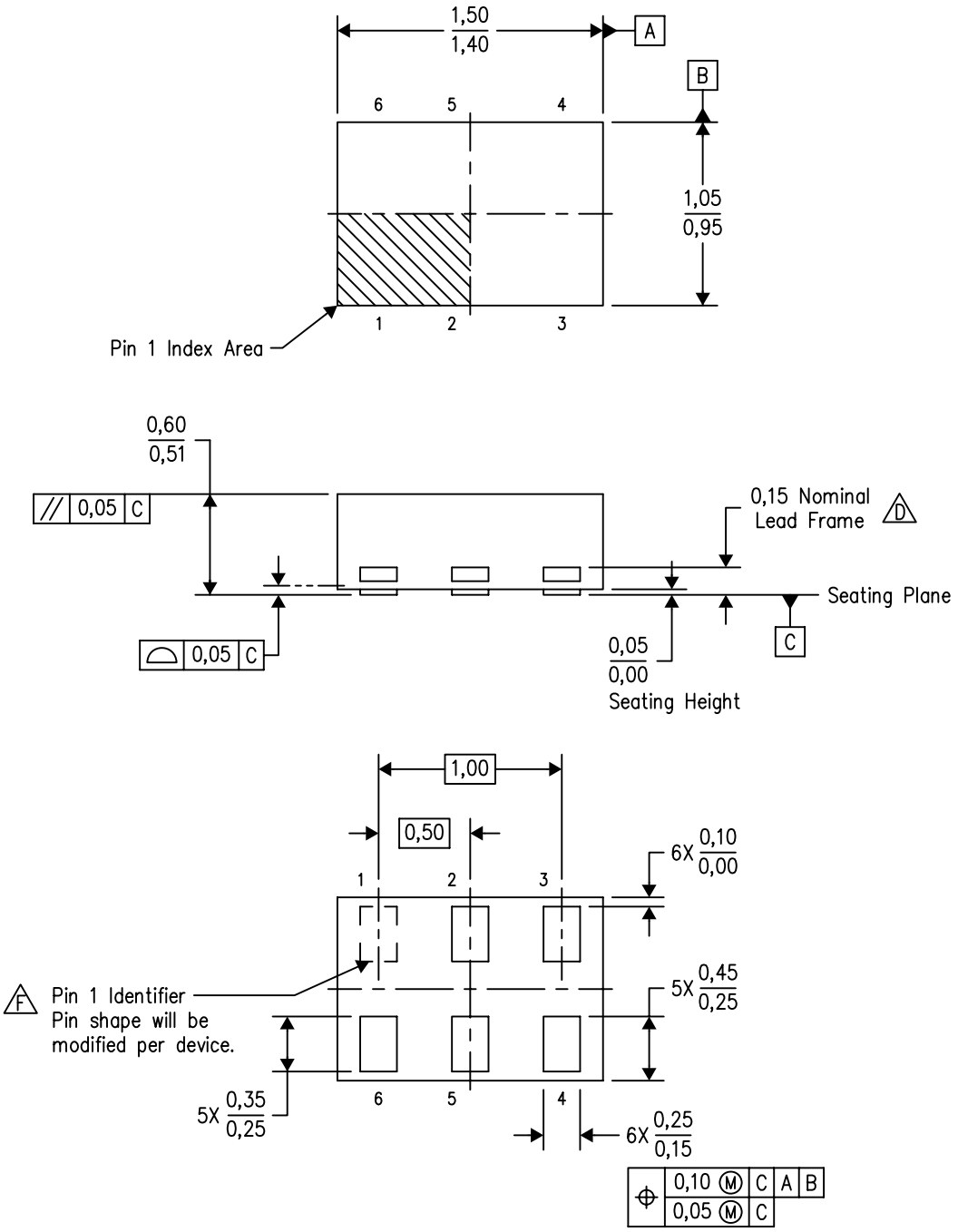
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3420DDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3420DDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3421ECDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3421ECDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3421EGDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3421EGDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3422EGDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3422EGDRYT	SON	DRY	6	250	203.0	203.0	35.0

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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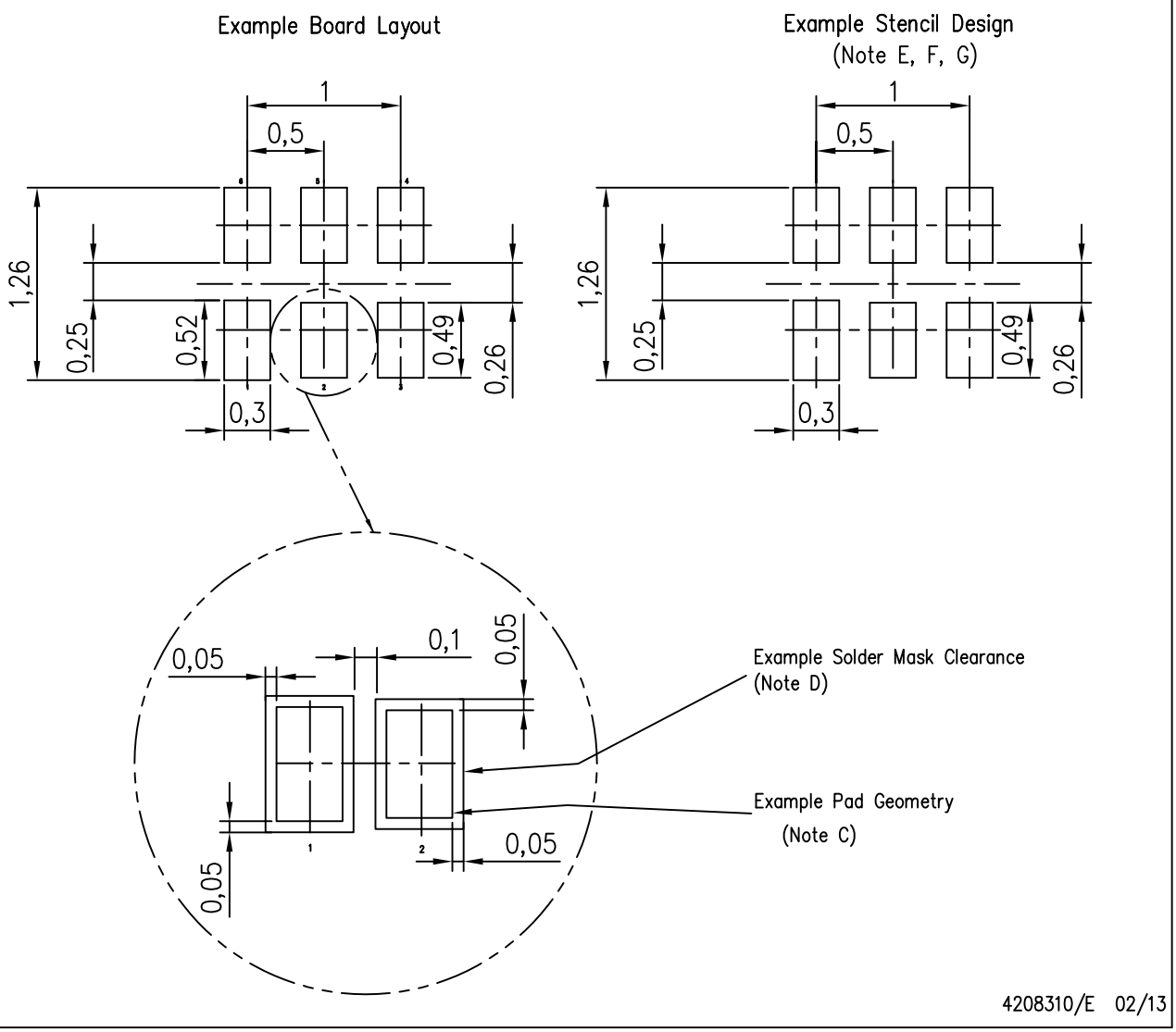
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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