

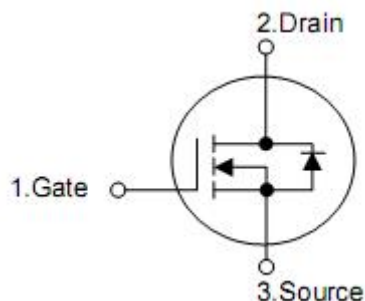
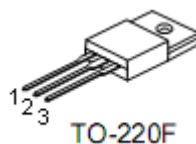
1. Description

This Power MOSFET is produced using KIA semi`s advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

2. Features

- n $R_{DS(on)}=1.15\Omega @ V_{GS}=10V$
- n Low gate charge (typical 22nC)
- n High ruggedness
- n Fast switching
- n 100% avalanche tested
- n Improved dv/dt capability

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

 (T_C= 25 °C , unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V _{DSS}	600	V
Gate-source voltage	V _{GSS}	±30	V
Drain current continuous	I _D	T _C =25°C	7.0*
		T _C =100°C	4.2*
Drain current pulsed (note1)	I _{DM}	28*	A
Avalanche energy	Repetitive (note1)	E _{AR}	17.6
	Single pulse (note2)	E _{AS}	280
Peak diode recovery dv/dt (note3)	dv/dt	4.5	V/ns
Total power dissipation	P _D	T _C =25 °C	39
		derate above 25 °C	0.31
Operating and storage temperature range	T _J , T _{STG}	-55~+150	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T _L	300	°C

* Drain current limited by maximum junction temperature

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance, Junction-ambient	R _{thJA}	62.5	°C/W
Thermal resistance, case-to-sink typ.	R _{thCS}	-	°C/W
Thermal resistance, Junction-case	R _{thJC}	3.2	°C/W

6. Electrical characteristics

 (T_C=25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	-	-	1	μA
		V _{DS} =480V, T _C =125°C	-	-	10	μA
Gate-body leakage current	Forward	I _{GSS}	-	-	100	nA
	Reverse				-100	nA
Breakdown voltage temperature coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, referenced to 25°C	-	0.6	-	V/°C
On characteristics						
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	-	4.0	V
Static drain-source on-resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.5A	-	1.15	1.4	Ω
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	1020	-	pF
Output capacitance	C _{oss}		-	90	-	pF
Reverse transfer capacitance	C _{rss}		-	10.5	-	pF
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} =300V, I _D =7A, R _G =25Ω (note4,5)	-	15	-	ns
Rise time	t _r		-	9	-	ns
Turn-off delay time	t _{d(off)}		-	83	-	ns
Fall time	t _f		-	21	-	ns
Total gate charge	Q _g	V _{DS} =480V, I _D =7A, V _{GS} =10V (note4,5)	-	22	-	nC
Gate-source charge	Q _{gs}		-	5	-	nC
Gate-drain charge	Q _{gd}		-	8	-	nC
Drain-source diode characteristics and maximum ratings						
Drain-source diode forward voltage	V _{SD}	V _{GS} =0V, I _{SD} =7A	-	-	1.4	V
Continuous drain-source current	I _{SD}		-	-	7	A
Pulsed drain-source current	I _{SM}		-	-	28	A
Reverse recovery time	t _{rr}	V _{GS} =0V, I _{SD} =7A di/dt=100A/μs (note4)	-	405	-	ns
Reverse recovery charge	Q _{rr}		-	3.3	-	μC

Note:1. Repetitive rating: pulse width limited by maximum junction temperature

 2. L=9mH, I_{AS}=7A, V_{DD}=50V, R_G=25Ω, starting T_J=25°C

 3. I_{SD}≤7.0A, di/dt≤200A/μs, V_{DD}≤BV_{DSS}, starting T_J=25 °C

4. Pulse test: pulse width≤300μs, duty cycle≤2%

5. Essentially independent of operating temperature

7. Test circuits and waveforms

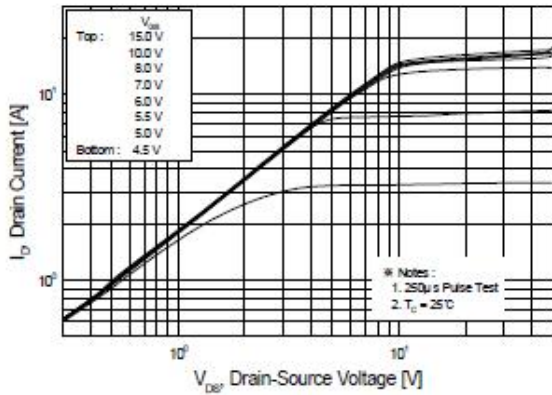


Figure 1. On-Region Characteristics

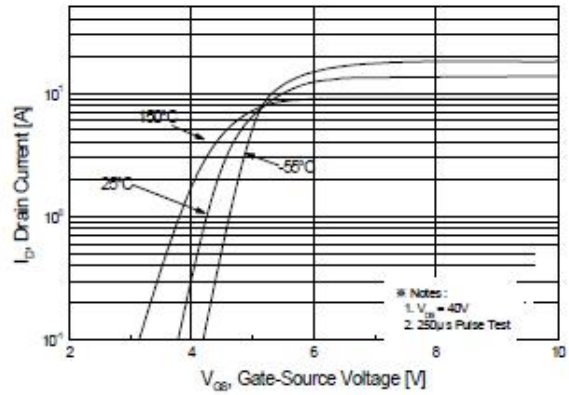


Figure 2. Transfer Characteristics

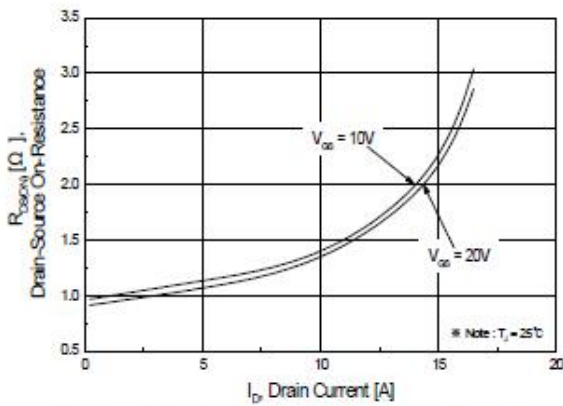


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

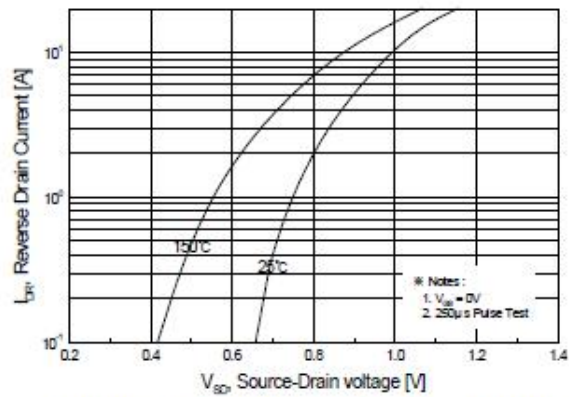


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

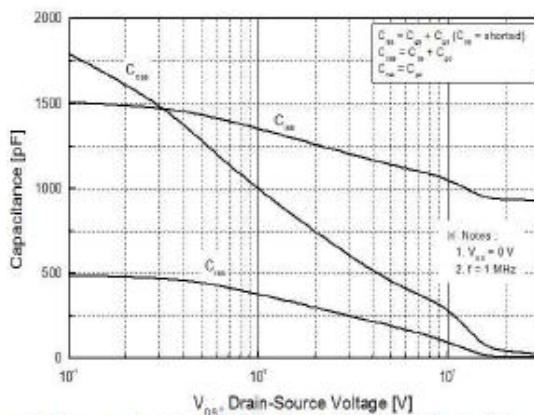


Figure 5. Capacitance Characteristics

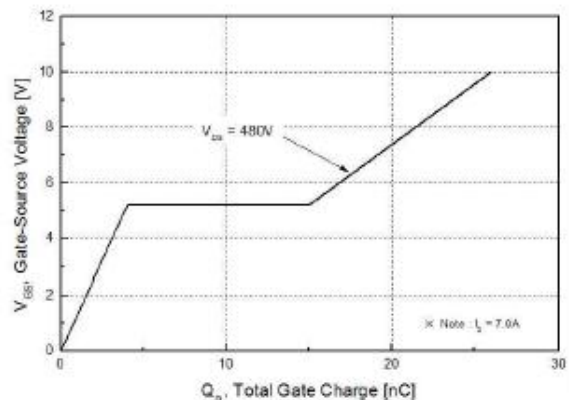


Figure 6. Gate Charge Characteristics

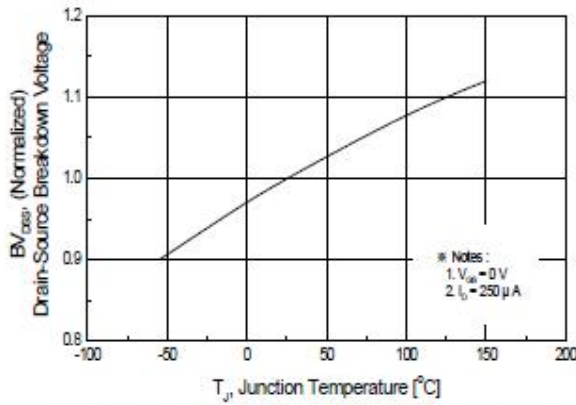


Figure 7. Breakdown Voltage Variation vs Temperature

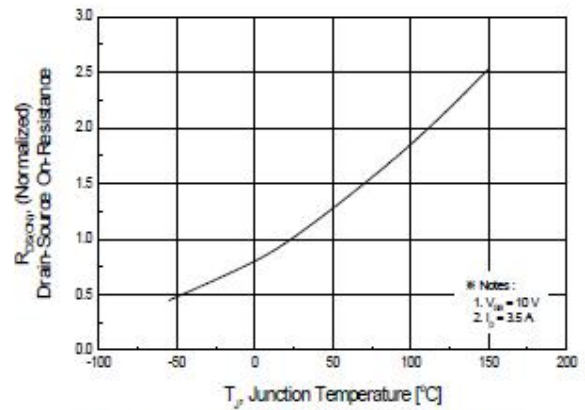


Figure 8. On-Resistance Variation vs Temperature

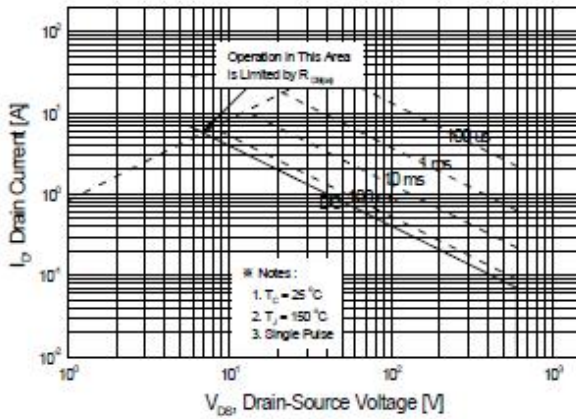


Figure 9 Maximum Safe Operating Area

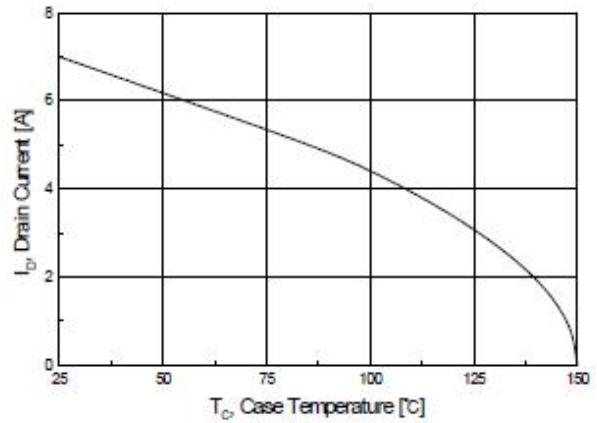


Figure 10. Maximum Drain Current vs Case Temperature

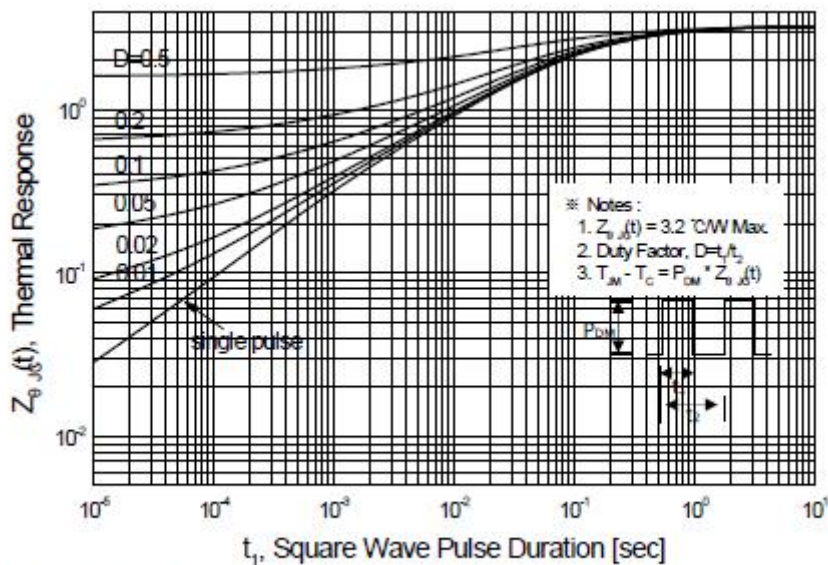
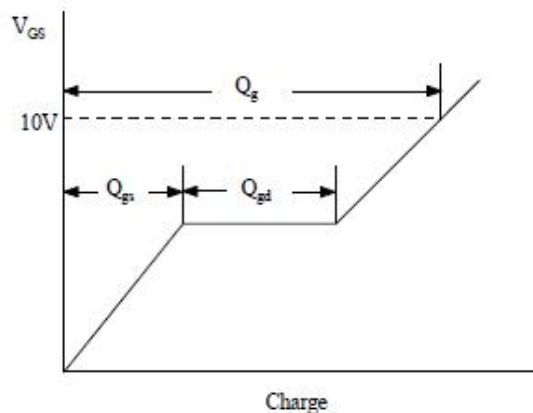
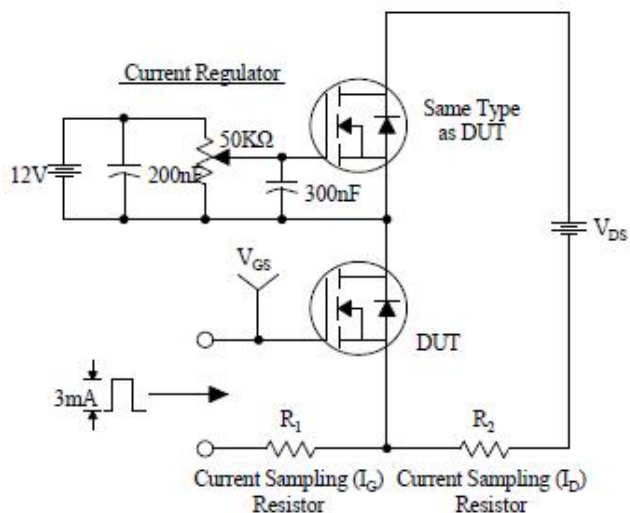
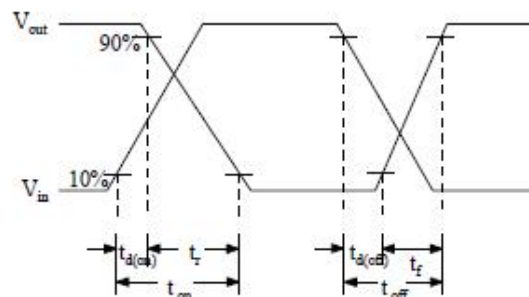
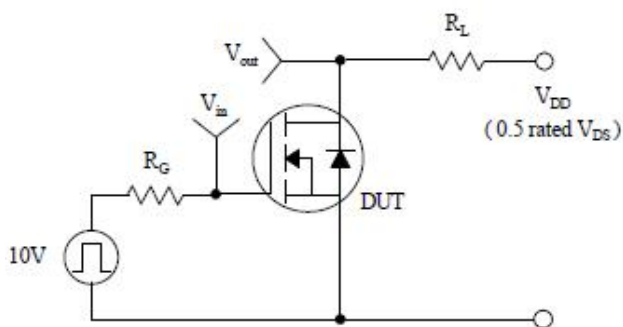


Figure 11 Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

