NB3N5573

Clock Generator, Crystal to 25 MHz, 100 MHz, 125 MHz, 200 MHz, 3.3 V, with Dual HCSL

ON Semiconductor®

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Description

The NB3N5573 is a precision, low phase noise clock generator that supports PCI Express and Ethernet requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal and generates a differential HCSL output at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies. Outputs can interface with LVDS with proper termination (See Figure 4).

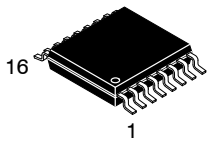
This device is housed in 5.0 mm x 4.4 mm narrow body TSSOP 16 pin package.

Features

- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- External Loop Filter is Not Required
- HCSL Differential Output or LVDS with Proper Termination
- Four Selectable Multipliers of the Input Frequency
- Output Enable with Tri−State Outputs
- PCIe Gen1, Gen2, Gen3, Gen4, QPI, UPI Jitter Compliant
- Phase Noise: @ 100 MHz

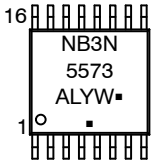
Offset	Noise Power
100 Hz	−109.4 dBc
1 kHz	−127.8 dBc
10 kHz	−136.2 dBc
100 kHz	−138.8 dBc
1 MHz	−138.2 dBc
10 MHz	−161.4 dBc
20 MHz	−163.00 dBc

- Typical Period Jitter RMS of 1.5 ps
- Operating Range 3.3 V ±10%
- Industrial Temperature Range −40°C to +85°C
- These are Pb−Free Devices



TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

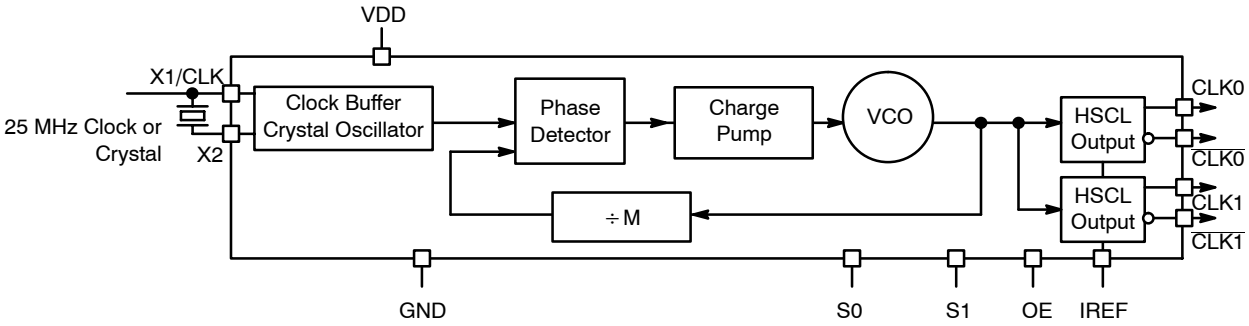


Figure 1. NB3N5573 Simplified Logic Diagram

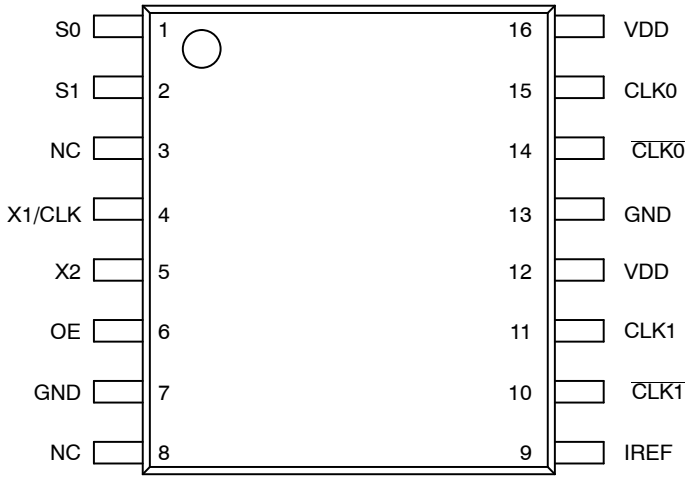


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	S0	Input	LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to V_{DD}. See output select table 2 for details.
2	S1	Input	LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to V_{DD}. See output select Table 2 for details.
12, 16	V_{DD}	Power Supply	Positive supply voltage pins are connected to +3.3 V supply voltage.
4	X1/CLK	Input	Crystal or Clock input. Connect to 25 MHz crystal source or single−ended clock.
5	X2	Input	Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input.
6	OE	Input	Output enable tri−states output when connected to GND. Internal pullup resistor to V_{DD}.
7, 13	GND	Power Supply	Ground 0 V. These pins provide GND return path for the devices.
9	I_{REF}	Output	Output current reference pin. Precision resistor (typ. 475 Ω) is connected to set the output current.
11	CLK1	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 4)
10	$\overline{CLK1}$	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 4)
15	CLK0	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 4)
14	$\overline{CLK0}$	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 4)
3, 8	NC		Do not connect

Table 2. OUTPUT FREQUENCY SELECT TABLE WITH 25MHz CRYSTAL

S1*	S0*	CLK Multiplier	f_{CLKout} (MHz)
L	L	1x	25
L	H	4x	100
H	L	5x	125
H	H	8x	200

*Pins S1 and S0 default high when left open.

Recommended Crystal Parameters

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25 °C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Drive Level	100 μW Max

Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model	> 2 kV
RPU – OE, S0 and S1 Pull−up Resistor		100 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		7623
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage (V_{IN})	GND = 0 V	GND ≤ V_I ≤ V_{DD}	−0.5 V to V_{DD}+0.5 V	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−16 TSSOP−16	138 108	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	TSSOP−16	33 to 36	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS (V_{DD} = 3.3 V ±10%, GND = 0 V, T_A = −40°C to +85°C, Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
VDD	Power Supply Voltage	2.97	3.3	3.63	V
I_{DD}	Power Supply Current		120	135	mA
I_{DDOE}	Power Supply Current when OE is Set Low			65	mA
V_{IH}	Input HIGH Voltage (X/CLK, S0, S1, and OE)	2000		V_{DD} + 300	mV
V_{IL}	Input LOW Voltage (X/CLK, S0, S1, and OE)	GND – 300		800	mV
V_{OH}	Output HIGH Voltage for HCSL Output (See Figure 5)	660	700	850	mV
V_{OL}	Output LOW Voltage for HCSL Output (See Figure 5)	−150	0	150	mV
V_{cross}	Crossing Voltage Magnitude (Absolute) for HCSL Output	250		550	mV
ΔV_{cross}	Change in Magnitude of V_{cross} for HCSL Output			150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Measurement taken with outputs terminated with R_S = 33.2 Ω, R_L = 49.9 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 3.

Table 6. AC CHARACTERISTICS (V_{DD} = 3.3 V ±10%, GND = 0 V, T_A = −40°C to +85°C; Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLKIN}	Clock/Crystal Input Frequency		25		MHz
f_{CLKOUT}	Output Clock Frequency	25		200	MHz
θ_{NOISE}	Phase−Noise Performance f_{CLKx} = 200 MHz/100 MHz				dBc/Hz
	@ 100 Hz offset from carrier		−103/−109		
	@ 1 kHz offset from carrier		−118/−127.8		
	@ 10 kHz offset from carrier		−122/−136.2		
	@ 100 kHz offset from carrier		−130/−138.8		
	@ 1 MHz offset from carrier		−132/−138.2		
	@ 10 MHz offset from carrier		−149/−164		
t_{JITTER}	Period Jitter Peak−to−Peak (Note 6) f_{CLKx} = 200 MHz		10	20	ps
	Period Jitter RMS (Note 6) f_{CLKx} = 200 MHz		1.5	3	
	Cycle−Cycle RMS Jitter (Note 7) f_{CLKx} = 200 MHz		2	5	
	Cycle−to−Cycle Peak to Peak Jitter (Note 7) f_{CLKx} = 200 MHz		20	35	ps
$t_{JIT(\Phi)}$	Additive Phase RMS Jitter, Integration Range 12 kHz to 20 MHz		0.4		ps
OE	Output Enable/Disable Time		10		μs
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at cross point)	45	50	55	%
t_R	Output Risetime (Measured from 175 mV to 525 mV, Figure 5)	175	340	700	ps
t_F	Output Falltime (Measured from 525 mV to 175 mV, Figure 5)	175	340	700	ps
Δt_R	Output Risetime Variation (Single−Ended)			125	ps
Δt_F	Output Falltime Variation (Single−Ended)			125	ps
Stabilization Time	Stabilization Time From Powerup V_{DD} = 3.3 V		3.0		ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Measurement taken from differential output on single−ended channel terminated with R_S = 33.2 Ω, R_L = 49.9 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 3.
6. Sampled with 10000 cycles.
7. Sampled with 1000 cycles.

Table 7. ELECTRICAL CHARACTERISTICS – PHASE JITTER PARAMETERS

Symbol	Parameter	Conditions (Notes 8 and 9)	Min	Typ	Max	Industry Limit	Unit
$t_{jphPCIeG1}$	RMS Phase Jitter	PCIe Gen 1 (Notes 10 and 11)		10	16	86	ps (p–p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 10)		0.2	0.25	3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 10)		0.9	1.2	3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2–4 MHz, CDR = 10 MHz) (Note 10)		0.2	0.3	1	ps (rms)
$t_{jphPCIeG4}$		PCIe Gen 4 (PLL BW of 2–4 MHz, CDR = 10 MHz) (Note 10)		0.21	0.3	0.5	ps (rms)
t_{jphUPI}		UPI (9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI)		0.62	0.7	1.0	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Note 12)		0.1	0.3	0.5	ps (rms)
		QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Note 12)		0.1	0.15	0.3	ps (rms)
		QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Note 12)		0.07	0.1	0.2	ps (rms)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Applies to all outputs.
9. Guaranteed by design and characterization, not tested in production
10. See http://www.pcisig.com for complete specs
11. Sample size of at least 100K cycles. This figures extrapolates to 108 ps pk–pk @ 1M cycles for a BER of 1–12.
12. Calculated from Intel–supplied Clock Jitter Tool v 1.6.3.

HCSL INTERFACE

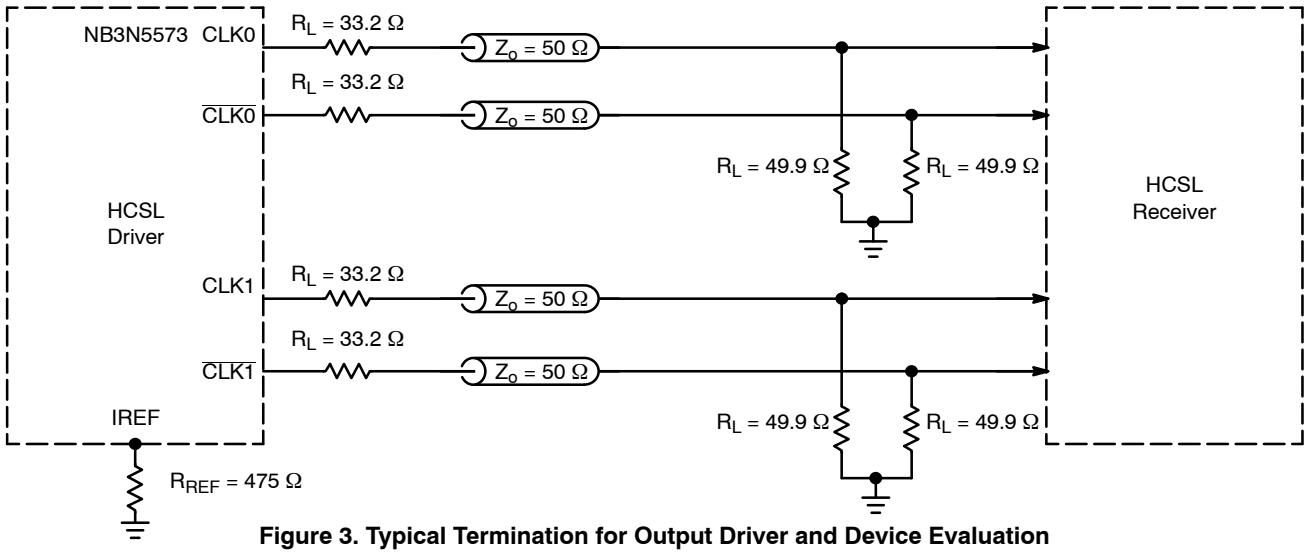


Figure 3. Typical Termination for Output Driver and Device Evaluation

LVDS COMPATIBLE INTERFACE

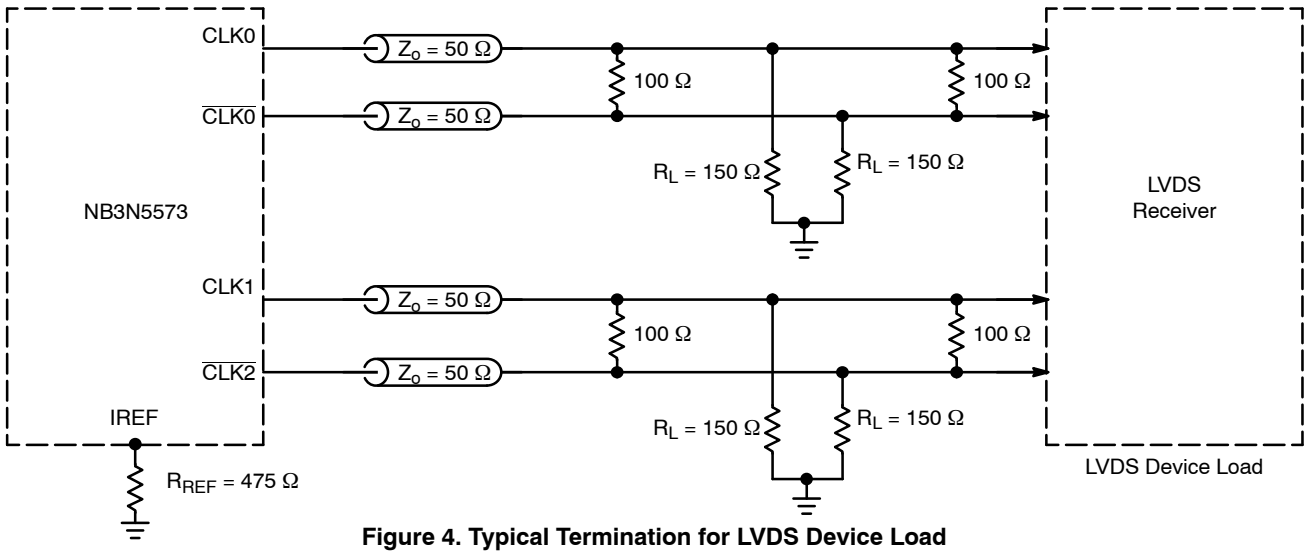


Figure 4. Typical Termination for LVDS Device Load

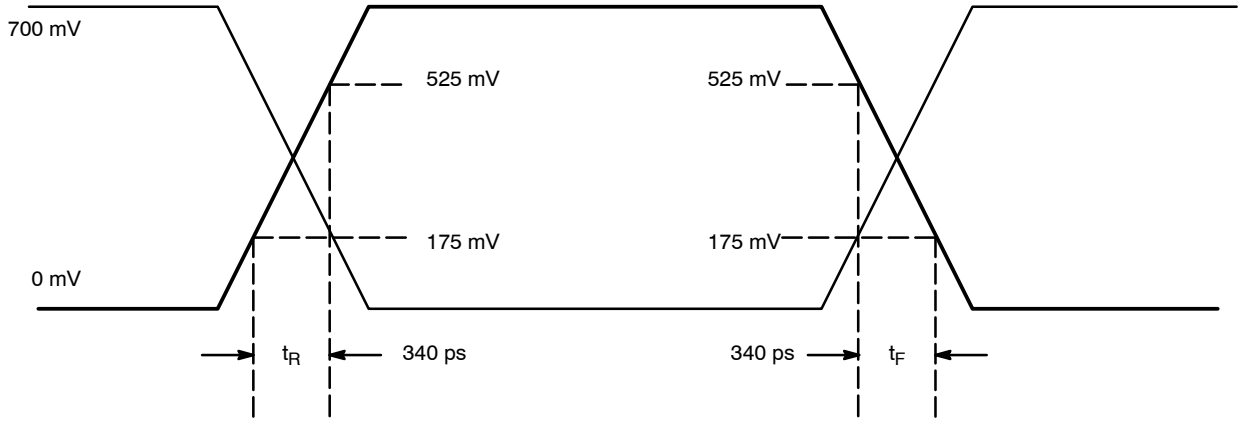


Figure 5. HCSL Output Parameter Characteristics

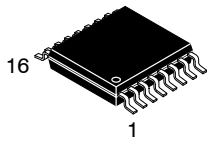
ORDERING INFORMATION

Device	Package	Shipping†
NB3N5573DTG	TSSOP−16 (Pb−Free)	96 Units / Rail
NB3N5573DTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

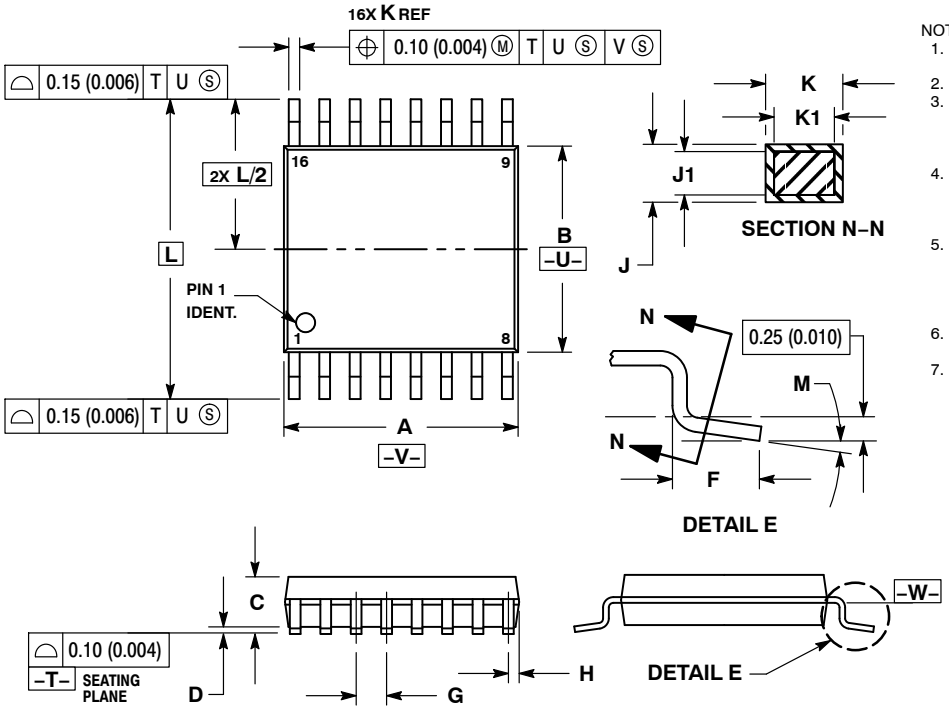
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

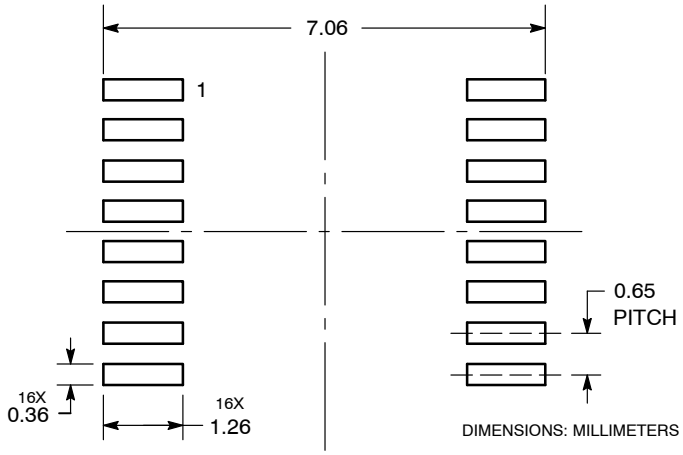
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

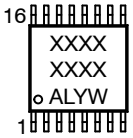
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSSOP−16	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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