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FDV302P Digital FET, P-Channel

General Description

This P-Channel logic level enhancement mode field effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one P-channel FET can replace several digital transistors with different bias resistors such as the DTCx and DCDx series.

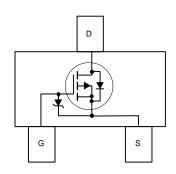
Features

- Very low level gate drive requirements allowing direct operation in 3V circuits. V_{GS(th)} < 1.5V.
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Compact industry standard SOT-23 surface mount package.
- Replace many PNP digital transistors (DTCx and DCDx) with one DMOS FET.



Mark:302





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	FDV302P	Units
V _{DSS}	Drain-Source Voltage	-25	V
V_{GSS}	Gate-Source Voltage	-8	V
I _D	Drain Current - Continuous	-0.12	А
	- Pulsed	-0.5	
P_{D}	Maximum Power Dissipation	0.35	W
T _J ,T _{STG}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV
THERMA	L CHARACTERISTICS		•
R _{eJA}	Thermal Resistance, Junction-to-Ambient	357	°C/W

Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHAR	ACTERISTICS					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-25			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25 °C		-20		mV /°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -20 \text{ V}, \ V_{GS} = 0 \text{ V}$			-1	μA
		T _J = 55°C			-10	μA
I _{GSS}	Gate - Body Leakage Current	$V_{GS} = -8 \text{ V}, \ V_{DS} = 0 \text{ V}$			-100	nA
	CTERISTICS (Note)		•			
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25 °C		1.9		mV /°C
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-0.65	-1	-1.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -2.7 \text{ V}, I_D = -0.05 \text{ A}$		10.6	13	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -0.2 \text{ A}$		7.9	10	1
		T _J =125°C		12	18	1
I _{D(ON)}	On-State Drain Current	$V_{GS} = -2.7 \text{ V}, \ V_{DS} = -5 \text{ V}$	-0.05			Α
9 _{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -0.2 \text{ A}$		0.135		S
DYNAMIC C	HARACTERISTICS	•	•			
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, \ V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$		11		pF
C _{oss}	Output Capacitance			7		pF
C _{rss}	Reverse Transfer Capacitance			1.4		pF
SWITCHING	CHARACTERISTICS (Note)					
t _{D(on)}	Turn - On Delay Time	$V_{DD} = -6 \text{ V}, \ I_{D} = -0.2 \text{ A},$ $V_{GS} = -4.5 \text{ V}, \ R_{GEN} = 50 \Omega$		5	12	ns
t _r	Turn - On Rise Time			8	16	ns
$\mathbf{t}_{D(off)}$	Turn - Off Delay Time			9	18	ns
t,	Turn - Off Fall Time			5	10	ns
Q_g	Total Gate Charge	$V_{DS} = -5 \text{ V}, I_{D} = -0.2 \text{ A},$ $V_{GS} = -4.5 \text{ V}$		0.22	0.31	nC
Q_{gs}	Gate-Source Charge			0.11		nC
Q_{gd}	Gate-Drain Charge			0.04		nC
DRAIN-SOU	RCE DIODE CHARACTERISTICS AND MAX	KIMUM RATINGS		•	1	
I _s	Maximum Continuous Drain-Source Diode Forward Current				-0.2	Α
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -0.2 \text{ A} \text{ (Note)}$		-1	-1.5	V

Note: Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

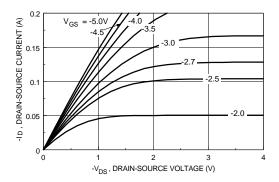


Figure 1. On-Region Characteristics.

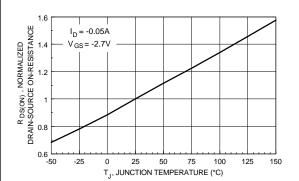


Figure 3. On-Resistance Variation with Temperature.

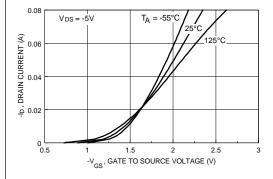


Figure 5. Transfer Characteristics.

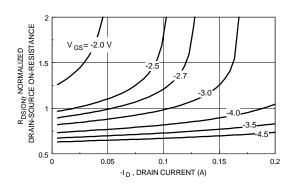


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

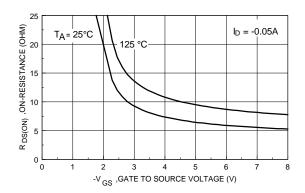


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

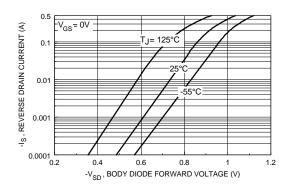


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical And Thermal Characteristics

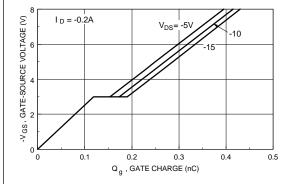


Figure 7. Gate Charge Characteristics.

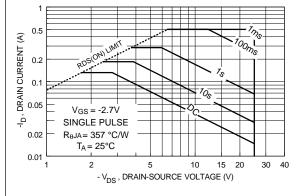


Figure 9. Maximum Safe Operating Area.

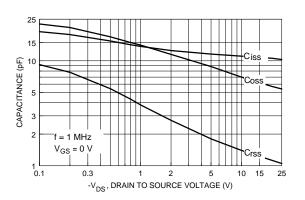


Figure 8. Capacitance Characteristics.

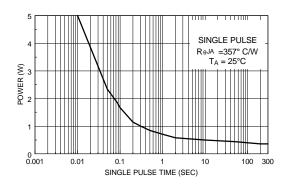


Figure 10. Single Pulse Maximum Power Dissipation.

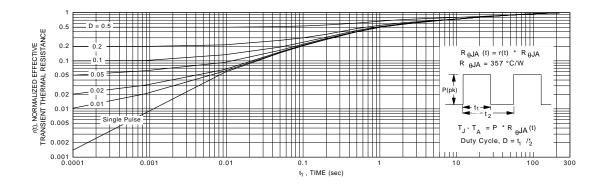


Figure 11. Transient Thermal Response Curve.

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