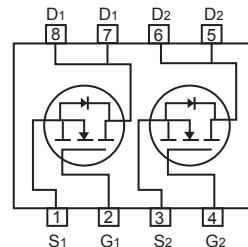
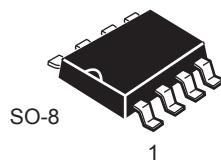


## Dual N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 20V, 6A,  $R_{DS(ON)} = 27m\Omega$  @ $V_{GS} = 4.5V$ .  
 $R_{DS(ON)} = 40m\Omega$  @ $V_{GS} = 2.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- Lead free product is acquired.
- Surface mount Package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	6	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	35	A
Maximum Power Dissipation	$P_D$	2.0	W
Operating and Store Temperature Range	$T_J, T_{Stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$



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## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	20			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}$			1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 12\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -12\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics<sup>c</sup></b>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	0.5		1.5	V
Static Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 4.5\text{V}, I_D = 6\text{A}$		21	27	$\text{m}\Omega$
		$V_{\text{GS}} = 2.5\text{V}, I_D = 5.2\text{A}$		32	40	$\text{m}\Omega$
<b>Dynamic Characteristics<sup>d</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 8\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		720		pF
Output Capacitance	$C_{\text{oss}}$			130		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			95		pF
<b>Switching Characteristics<sup>d</sup></b>						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 10\text{V}, I_D = 1\text{A}, V_{\text{GS}} = 4.5\text{V}, R_{\text{GEN}} = 6\Omega$		10	20	ns
Turn-On Rise Time	$t_r$			7	14	ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			34	68	ns
Turn-Off Fall Time	$t_f$			6	12	ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 10\text{V}, I_D = 6\text{A}, V_{\text{GS}} = 4.5\text{V}$		6.8	8.8	nC
Gate-Source Charge	$Q_{\text{gs}}$			0.5		nC
Gate-Drain Charge	$Q_{\text{gd}}$			1.8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				1.7	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 1.7\text{A}$			1.2	V

Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature.
- b.Surface Mounted on FR4 Board,  $t \leq 10 \text{ sec.}$
- c.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- d.Guaranteed by design, not subject to production testing.



# CEM9926A

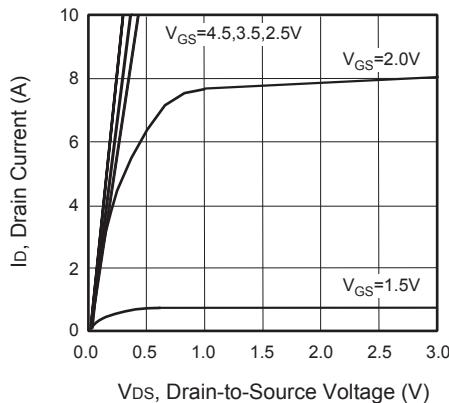


Figure 1. Output Characteristics

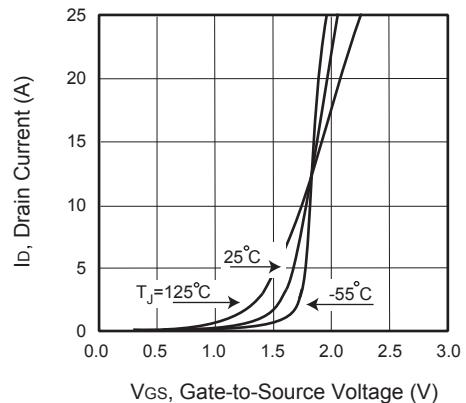


Figure 2. Transfer Characteristics

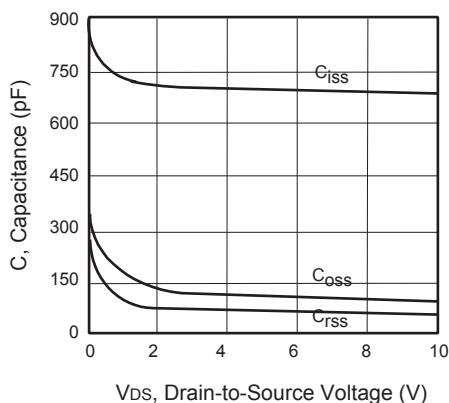


Figure 3. Capacitance

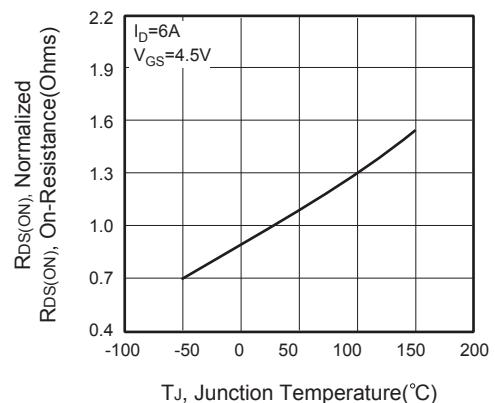


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

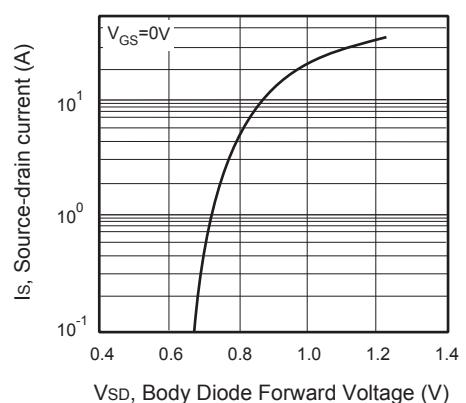


Figure 6. Body Diode Forward Voltage Variation with Source Current



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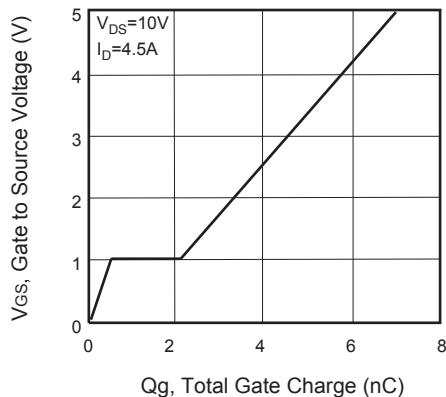


Figure 7. Gate Charge

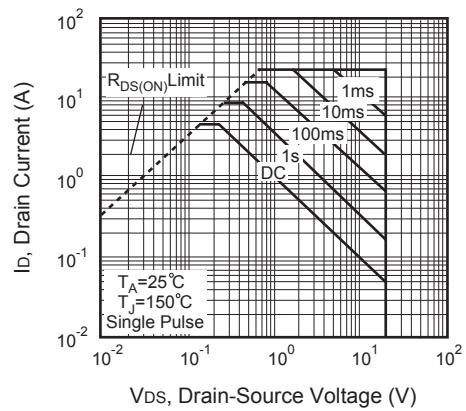


Figure 8. Maximum Safe Operating Area

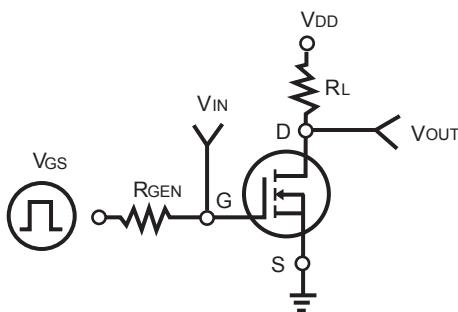


Figure 9. Switching Test Circuit

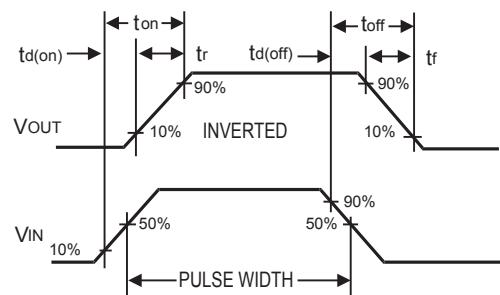


Figure 10. Switching Waveforms

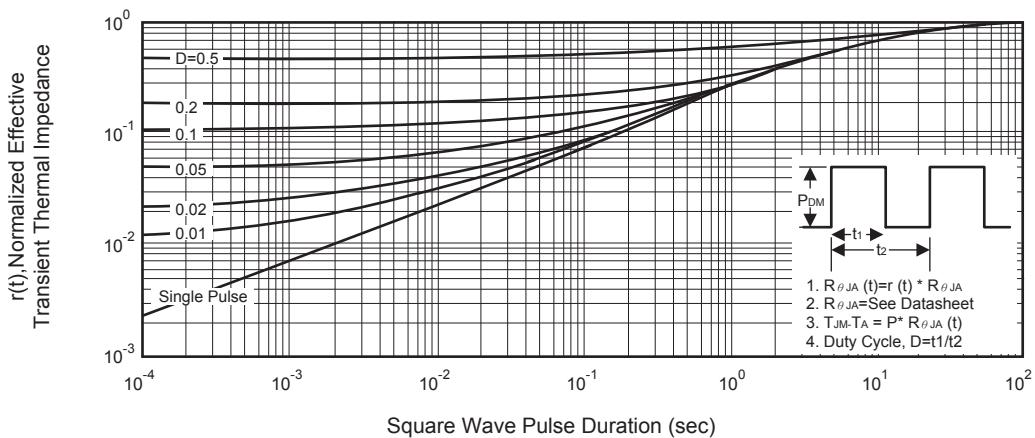


Figure 11. Normalized Thermal Transient Impedance Curve