TIOS101 Digital Sensor Output Drivers with Integrated Surge Protection

1 Features

- 7-V to 36-V Supply Voltage
- PNP, NPN or Push-Pull Configurable Output
- Low Residual Voltage of 1.75 V at 250 mA
- 50-mA to 350-mA Configurable Current Limit
- Tolerant to ±65-V Transients < 100 µs
- Reverse Polarity Protection of up to 55 V on VCC, OUT and GND
- Integrated EMC Protection on VCC and OUT
  - ±16 kV IEC 61000-4-2 ESD Contact Discharge
  - ±4 kV IEC 61000-4-4 Electrical Fast Transient
  - ±1.2 kV/500 Ω IEC 61000-4-5 Surge
- Fast Demagnetization of Inductive Loads up to 1.5 H
- Large Capacitive Load Driving Capability
- < 2.2-mA Quiescent Supply Current
- Integrated LDO Options for up to 20 mA Current
  - TIOS101: No LDO
  - TIOS101-3: 3.3-V LDO
  - TIOS101-5: 5-V LDO
- Overtemperature Warning and Thermal Protection
- Fault Indicator
- Extended Ambient Temperature: -40°C to 125°C
- 2.5 mm x 3 mm 10-pin VSON Package

2 Applications

- Proximity Switches
- Capacitive and Inductive Sensors
- Digital Outputs

3 Description

The TIOS101 devices are configurable as high-side, low-side or push-pull drivers. These devices are capable of withstanding up to 1.2 kV (500 Ω) of IEC 61000-4-5 surge and feature integrated reverse polarity protection.

A simple pin-programmable interface allows easy interfacing to the controller circuits. The output current limit can be configured using an external resistor.

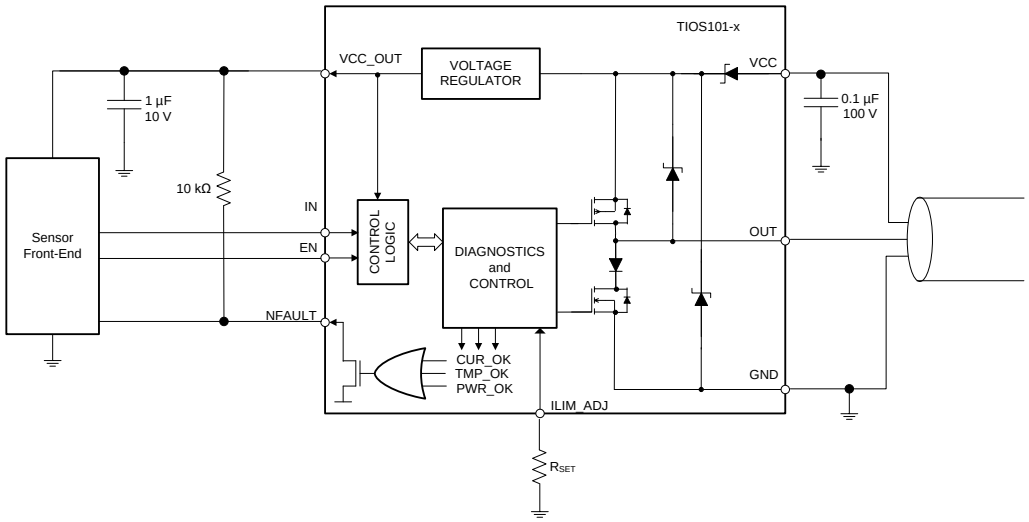
Fault reporting and internal protection functions are provided for under voltage, over circuit current and over temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TIOS101	VSON (10)	2.50 mm x 3.00 mm
TIOS101-3		
TIOS101-5		

(1) For all available devices, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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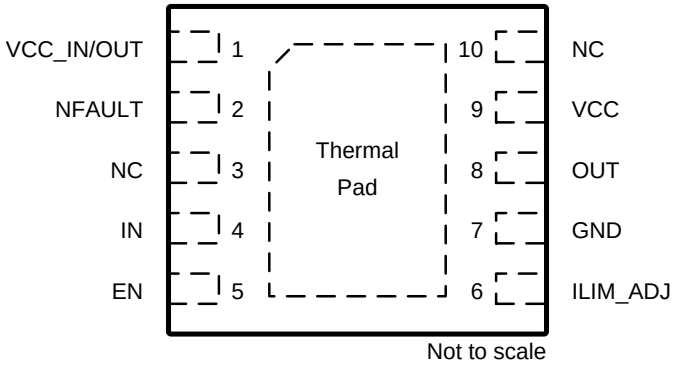
4 Revision History

Changes from Original (July 2017) to Revision A	Page
• Changed the *Thermal Information* table values	5

5 Pin Configuration and Functions

DMW Package
10-Pin (VSON)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	8	O	Switch output
VCC	9	POWER	Supply voltage (24 V nominal)
GND	7	POWER	Device ground
EN	5	I	Driver enable input signal from the local controller. Logic low sets the OUT output at Hi-Z. Weak internal pull-down.
IN	4	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
VCC_IN/OUT	1	POWER	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply input for option without LDO.
ILIM_ADJ	6	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and GND.
NFAULT	2	OPEN-DRAIN	Fault indicator output signal to the microcontroller. A low level indicates either an over- current, an undervoltage in supply or an overtemperature condition. Connect this pin via pull-up resistor to VCC_IN/OUT.
NC	3, 10	—	No internal connection.
Thermal Pad	—	—	Connect to GND plane for optimal thermal and electrical performance

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for VCC and OUT	–55	55	V
	Transient pulse width < 100 µs for VCC and OUT	–65	65	V
Voltage difference	$\lvert V_{(VCC)} - V_{(OUT)} \rvert$		55	V
Logic supply voltage (TIOS101)	VCC_IN	–0.3	6	V
Input logic voltage	IN, EN, ILIM_ADJ	–0.3	6	V
Output current	NFAULT	–5	5	mA
Storage temperature, T_{stg}		-55	170	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with reference to the GND pin, unless otherwise specified.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
		Contact discharge, per IEC 61000-4-2(2)(3)	Pins VCC, OUT and GND	±16000	
		Electrical fast transient, per IEC 61000-4-4(2)		±4000	
		Surge protection with 500 Ω, per IEC 61000-4-5; 1.2/50 µs (2)		±1200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Minimum 100-nF capacitor is required between VCC and GND. Minimum 1-µF capacitor is required between VCC_IN/OUT and GND.
(3) Passing level is ±4500 V if the device is powered and EN=IN=HIGH.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VCC)}$	Supply voltage		7	24	36	V
$V_{(VCC\_IN)}$	Logic level input voltage (TIOS101 only)	3.3 V configuration	3	3.3	3.6	V
		5 V configuration	4.5	5	5.5	V
R_{SET}	External resistor for OUT current limit		0		100	kΩ
$1/t_{BIT}$	Signaling rate (push-pull mode)				250	kbps
$I_{(VCC\_OUT)}$	LDO output current (TIOS101-3 and TIOS101-5 only)				20	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Junction temperature				150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TIOS101 DMW (10 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	25.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCC)						
$I_{(VCC)}$	Quiescent supply current	EN = LOW, no load		1.5	2.2	mA
		EN = HIGH, no load		2	2.7	mA
LOGIC-LEVEL INPUTS (EN, IN)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
R_{PD}	Pull-down (EN) resistance			100		kΩ
R_{PU}	Pull-up (IN) resistance			200		kΩ
CONTROL OUTPUT (NFAULT)						
V_{OL}	Output logic low voltage	I_O = 4 mA			0.5	V
I_{OZ}	Output high impedance leakage	Output in Hi-Z, V_O = 0 V or VCC_IN/OUT	–1		1	µA
DRIVER OUTPUT (OUT)						
$V_{DS(ON)}$	High-side driver residual voltage	I = 250 mA			1.75	V
		I = 200 mA			1.5	V
		I = 100 mA			1.1	V
	Low-side driver residual voltage	I = 250 mA			1.75	V
		I = 200 mA			1.5	V
		I = 100 mA			1.1	V
I_P	OUT pull-up/down current	EN = LOW, IN = LOW, pull-down current	40	50	80	µA
		EN = LOW, IN = HIGH, pull-up current	40	50	80	µA
$I_{O(LIM)}$	Driver output current limit	R_{SET} = 100 kΩ	35	50	70	mA
		R_{SET} = 0 kΩ	300	350	400	mA
		R_{SET} = OPEN(1)	300	350	400	mA
PROTECTION CIRCUITS						
$V_{(UVLO)}$	VCC under voltage lockout	VCC falling; NFAULT = Hi-Z			6	V
		VCC rising; NFAULT = LOW			6.5	V
$V_{(UVLO,HYS)}$	VCC under voltage hysteresis	Rising to falling threshold	100			mV
$V_{(UVLO\_IN)}$	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z		2.4		V
		VCC_IN rising; NFAULT = LOW		2.5		V
$V_{(UVLO,HYS)}$	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold		100		mV
$T_{(WRN)}$	Thermal warning	Die temperature T_J	125			°C
$T_{(SDN)}$	Thermal shutdown		150	160		°C
$T_{(HYS)}$	Thermal hysteresis for shutdown			10		°C

(1) Current fault indication will be active. Current fault auto recovery will be de-activated.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{REV}	Leakage current in reverse polarity	$V_{(OUT)} < V_{(VCC)}$ or $V_{(OUT} > V_{(VCC)}$, up to |36 V|				50	µA
		$V_{(OUT)} < V_{(VCC)}$ or $V_{(VCC)} > V_{(VCC)}$, up to |55 V|				80	µA
		EN = HIGH, IN = LOW; $V_{(OUT\ to\ VCC)}$ = 3 V				550	µA
		EN = HIGH, IN = HIGH; $V_{(OUT\ to\ GND)}$ = -3 V				10	µA
LINEAR REGULATOR (LDO)							
$V_{(VCC\_OUT)}$	Voltage regulator output	TIOS101-5		4.75	5	5.25	V
		TIOS101-3		3.13	3.3	3.46	V
$V_{(DROP)}$	Voltage regulator drop-out voltage ($V_{(VCC)} – V_{(VCC\_OUT)}$)	I_{CC} = 20 mA load current	TIOS101-5			1.9	V
			TIOS101-3			2.3	V
REG	Line regulation ($dV_{(VCC\_OUT)}/dV_{(VCC)}$	$I_{(VCC\_OUT)}$ = 1 mA				1.7	mV/V
L_{REG}	Load regulation ($dV_{(VCC\_OUT)}/V_{(VCC\_OUT)}$)	$V_{(VCC)}$ = 24 V, $I_{(VCC\_OUT)}$ = 100 µA to 20 mA				1%	
PSSR	Power Supply Rejection Ratio	100 kHz, $I_{(VCC\_OUT)}$ = 20 mA			40		dB

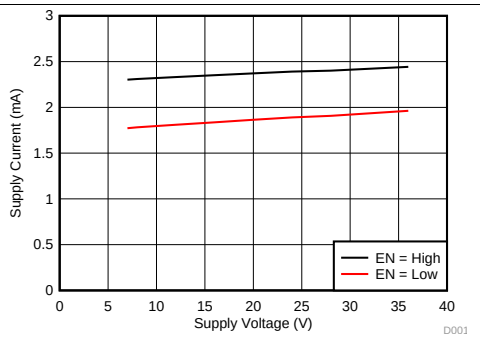
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Driver propagation delay	See Figure 5 See Figure 6 See Figure 7 R_L = 2 kΩ C_L = 5 nF $R_{(SET)}$ = 0 Ω		600	800	ns
$t_{P(skew)}$	Driver propagation delay skew. |t_{PLH} - t_{PHL}|			100		ns
t_{PZH}, t_{PZL}	Driver enable delay				4	µs
t_{PHZ}, t_{PLZ}	Driver disable delay				4	µs
t_r, t_f	Driver output rise, fall time				150	ns
|t_r – t_f|	Difference in rise and fall time				50	ns
t_{SC}	Current fault blanking time		175	200		µs
t_{pSC}	Current fault indication delay				260	µs
t_{SCEN}	Current fault driver re-enable wait time			15		ms
$t_{(UVLO)}$	OUT re-enable delay after UVLO (1)	$V_{(UVLO)}$ rising threshold crossing time to OUT enable time	10	30	50	ms

(1) OUT output remains Hi-Z for this time

6.7 Typical Characteristics



No load IN = OPEN 25°C

Figure 1. Supply Current vs Supply Voltage

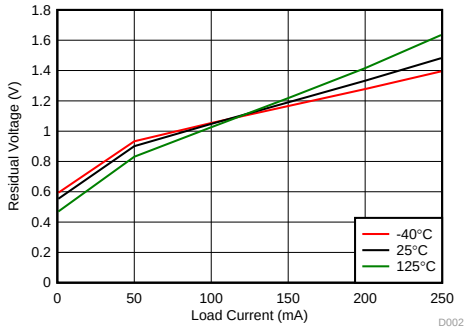


Figure 2. Residual Voltage vs Load Current: High Side

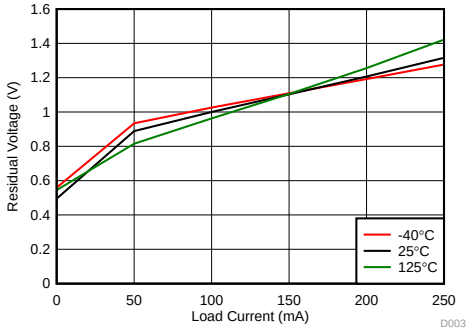


Figure 3. Residual Voltage vs Load Current: Low Side

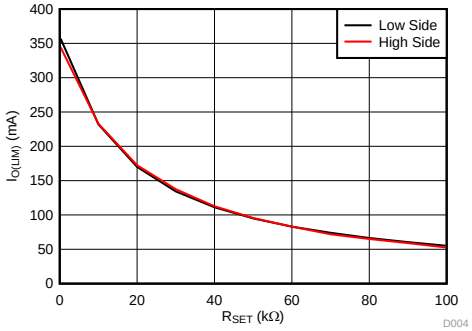


Figure 4. Current Limit vs R_{SET}

7 Parameter Measurement Information

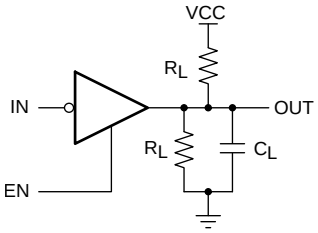


Figure 5. Test Circuit for Driver Switching

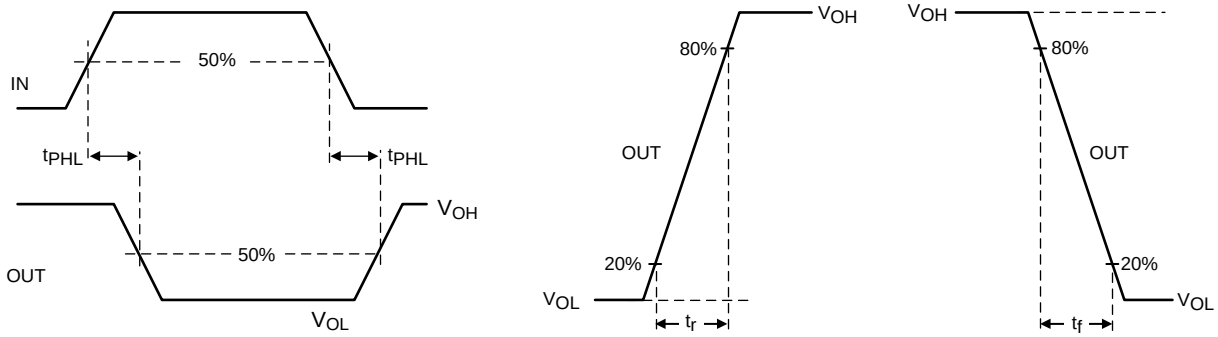


Figure 6. Waveforms for Driver Output Switching Measurements

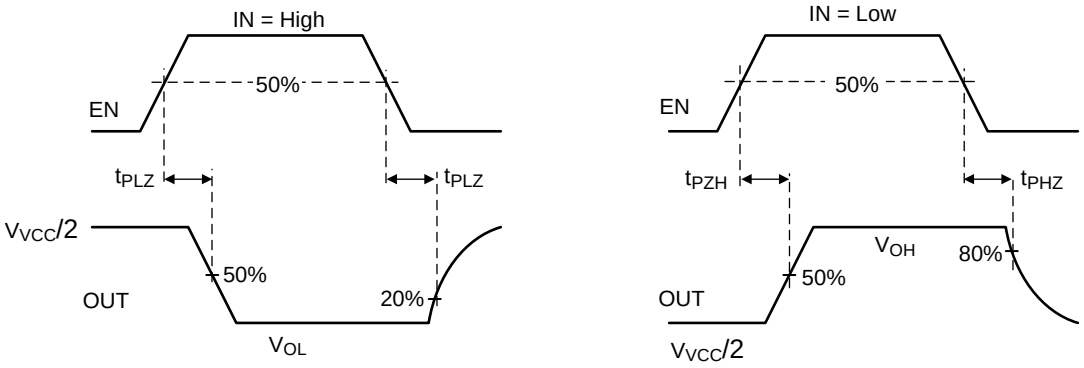


Figure 7. Waveforms for Driver Enable or Disable Time Measurements

8 Detailed Description

8.1 Overview

Figure 8 shows that the device driver output (OUT) can be used in a push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (IN) input pins. OUT can drive resistive, large capacitive or large inductive loads.

TIOS101 and TIOS101-x devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ±65-V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system-level design by reducing the external protection circuitry.

These devices implement protection features for over-current, over-voltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The TIOS101-x devices derive the low voltage supply from the typical 24 V industrial supply via an internal linear regulator to provide power to the local controller and sensor circuitry.

8.2 Functional Block Diagrams

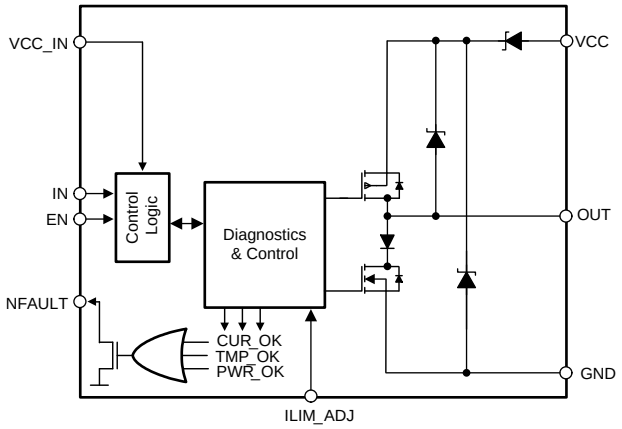


Figure 8. Block Diagram, TIOS101

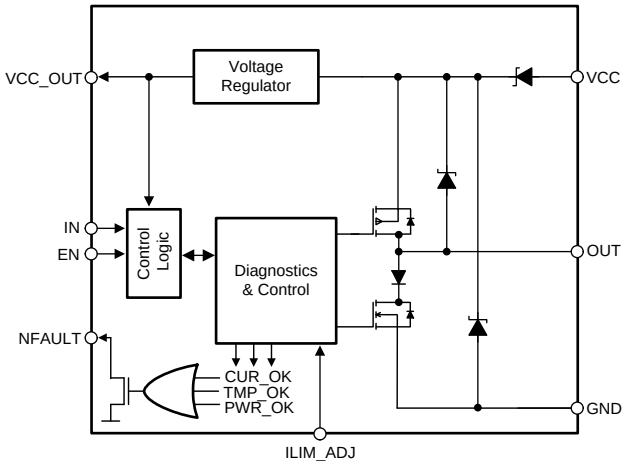


Figure 9. Block Diagram, TIOS101-x

8.3 Feature Description

8.3.1 Current Limit Configuration

The output current can be configured with an internal resistor on ILIM_ADJ pin. The maximum settable current limit is 300 mA. This maximum setting specifies a minimum of 300 mA over temperature and voltage.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitances.

Table 1. Current Limitation

ILIM_ADJ Pin Condition	OUT Current Limit	NFAULT Indication During Fault	Output Disable and Auto Recovery
R_{SET} resistor to GND	Variable	Yes	Yes
Connected to GND	300 mA	Yes	Yes
OPEN	300 mA	Yes	No

8.3.2 Current Fault Detection, Indication and Auto Recovery

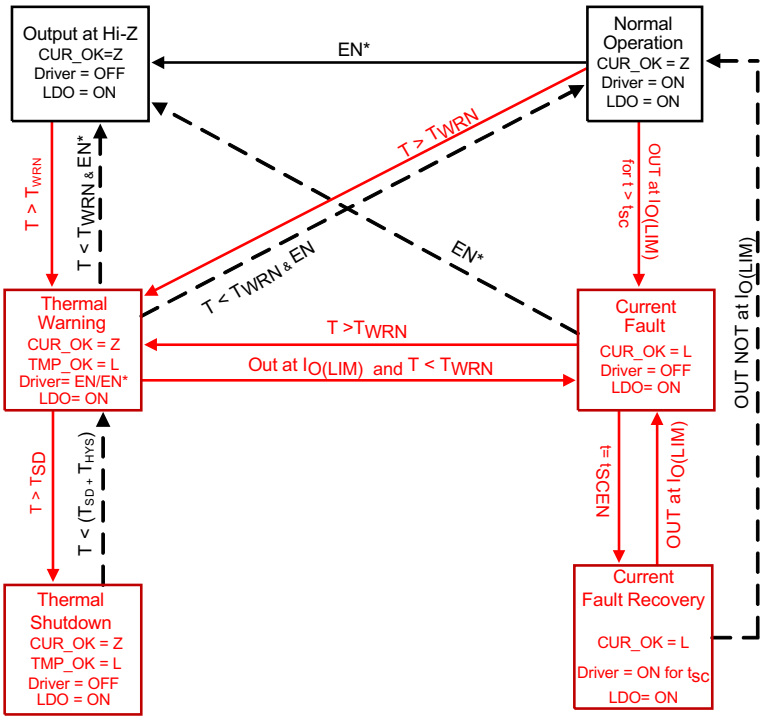
If the output current at OUT exceeds the internally set current limit $I_{O(LIM)}$ for a duration longer than t_{SC}, the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{SCEN} intervals. Current fault auto recovery mode can be disabled by setting ILIM_ADJ = OPEN. See Table 3.Toggling EN will clear NFAULT.

8.3.3 Thermal Warning, Thermal Shutdown

If the die temperature exceeds $T_{(WRN)}$, the NFAULT flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN and IN pins.

8.3.4 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded $T_{(WRN)}$ or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.



NFAULT = [CUR_OK && PWR_OK && TMP_OK]

Figure 10. Device State Diagram

8.3.5 Device Function Tables

Table 2. Driver Function

EN	IN	OUT	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	OUT is sourcing current (high-side drive)
H	H / Open	L	OUT is sinking current (low-side drive)

Table 3. Current Limit Indicator Function ($t > t_{SC}$)

EN	IN	OUT CURRENT	NFAULT	COMMENT
H	H / Open	$\lvert I_{(OUT)} \rvert > I_{O(LIM)}$	L	OUT current exceeds the set limit for over t_{SC}
		$\lvert I_{(OUT)} \rvert < I_{O(LIM)}$	Z	Normal operation
H	L	$\lvert I_{(OUT)} \rvert > I_{O(LIM)}$	L	OUT current exceeds the set limit for over t_{SC}
		$\lvert I_{(OUT)} \rvert < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, current limit indicator is inactive

8.3.6 The Integrated Voltage Regulator (LDO)

The TIOS101-3 and TIOS101-5 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for VCC voltages in the range of 7 V to 36 V with respect to GND. The LDO is capable of delivering up to 20 mA. The LDO output is current limited to 35-mA to limit the inrush current onto VCC_OUT decoupling capacitors during initial power up.

The LDO is designed to be stable with standard ceramic capacitors with values of 1 μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 μF.

8.3.7 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the VCC, OUT and GND pins. The maximum voltage between any of the pins may not exceed 55 V DC at any time.

Figure 11 and Figure 12 shows all the possible connection combinations.

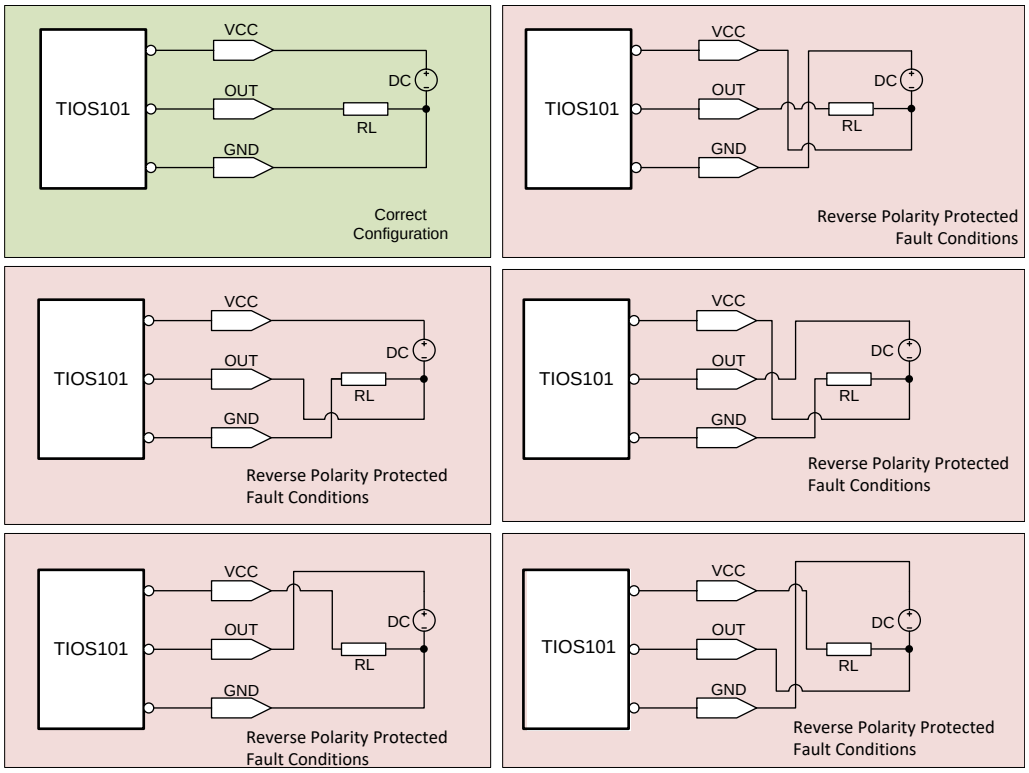


Figure 11. High-Side Driver Configuration

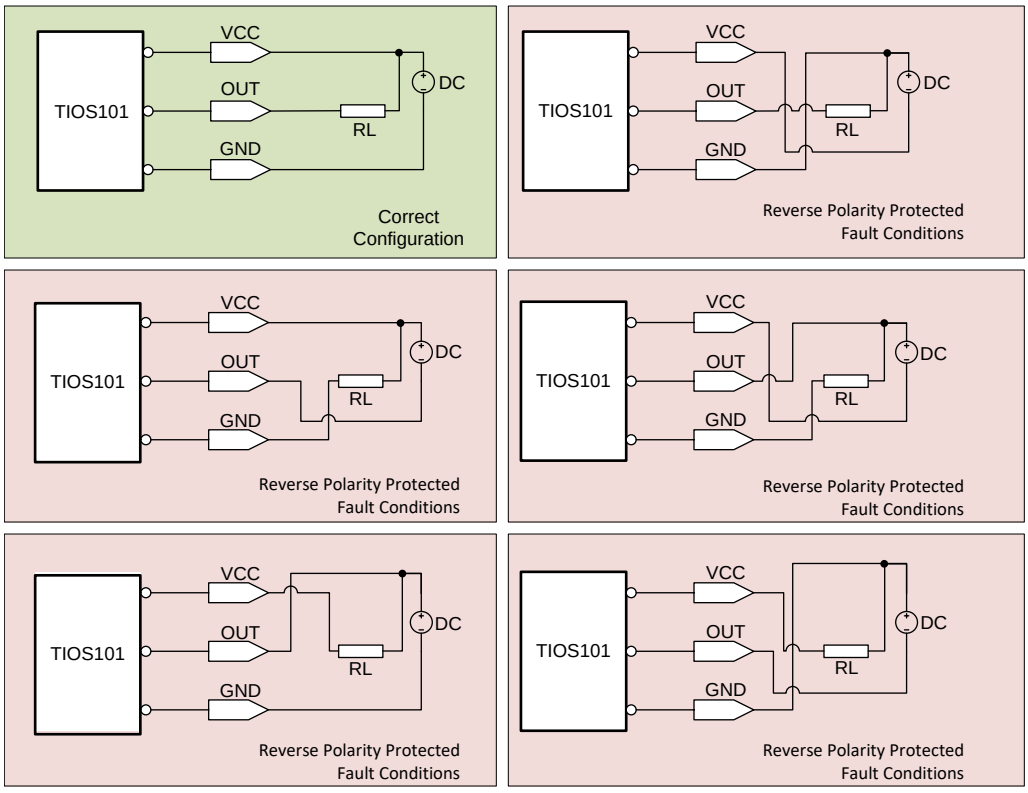
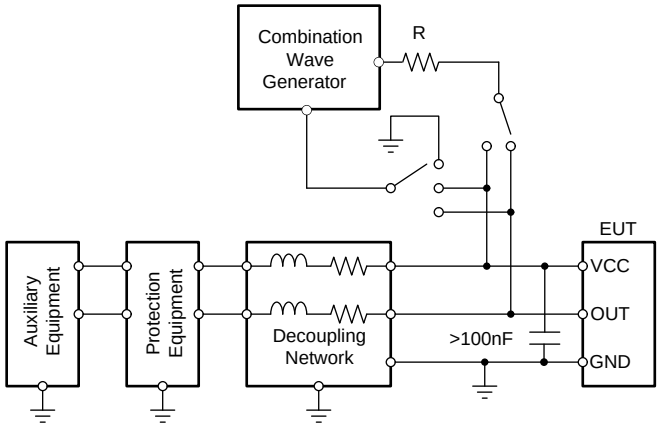


Figure 12. Low-Side Driver Configuration

8.3.8 Integrated Surge Protection and Transient Waveform Tolerance

The VCC and OUT pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 – 8/20 µs IEC 61000-4-5 surge with a source impedance of 500 Ω. The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between VCC and GND, and 1 µF between VCC_IN/OUT and GND.

External TVS diodes may be required for higher transient protection levels. The system designer should ensure that the maximum clamping voltage of the external diodes should be < 65 V at the desired current level. The device is capable of withstanding up to ±65-V transient pulses < 100 µs.



1.2/50 - 80/20 µs CWG

R = 500 Ω

Figure 13. Surge Test Setup

8.3.9 Power Up Sequence

VCC_IN and VCC domains can be powered up in any sequence. In the event of VCC is powered and VCC_IN is not, the OUT pin remains in high impedance.

8.3.10 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the VCC voltage falls below $V_{(UVLO)}$. (For the device without the integrated LDO, the device monitors VCC_IN in addition to VCC. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below $V_{(UVLO)}$), NFAULT is pulled low, the LDO is turned off and the OUT output is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above $V_{(UVLO)}$, NFAULT returns to Hi-Z (given no other fault conditions present) and the LDO will be enabled immediately. The OUT output will be turned on after $T_{(UVLO)}$ delay.

8.4 Device Functional Modes

These devices can operate in three different modes.

8.4.1 NPN Configuration (N-Switch Mode)

Set IN pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on OUT.

8.4.2 PNP Configuration (P-Switch Mode)

Set IN pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on OUT.

8.4.3 Push-Pull Mode

Set EN pin high and toggle IN as control for realizing the function of a push-pull output on OUT. Table 4, Table 5 and Table 6 summarize the pin configurations to accomplish the functional modes.

Table 4. NPN Mode

EN	IN	OUT
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

Table 5. PNP Mode

EN	IN	OUT
L / Open	L	Hi-Z
H	L	P-Switch

Table 6. Push-Pull Mode

EN	IN	OUT
L / Open	X	Hi-Z
H	H / Open	N-Switch
H	L	P-Switch

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TIOS101 and TIOS101-x are robust 24-V digital drivers for industrial sensors.

9.2 Typical Application

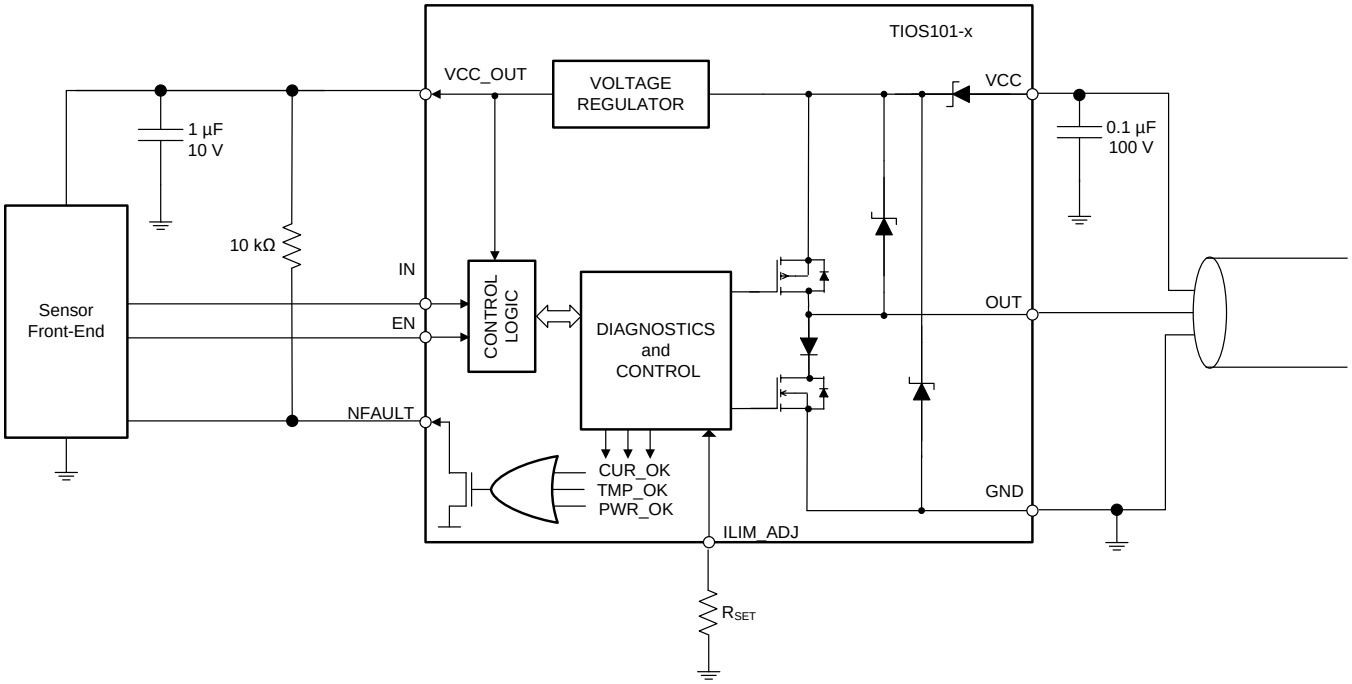


Figure 14. Typical Application Schematic

9.2.1 Design Requirements

Table 7 shows recommended components for a typical system design.

Table 7. Design Parameters

PARAMETERS	VALUE
Input voltage range (VCC)	24 V, 30 V (max)
Output current (OUT)	200 mA
Output voltage (VCC_OUT), Pick TIOS101-5	5 V
Maximum LDO output current ($I_{VCC(OUT)}$)	5 mA
Pull-up resistors for NFAULT	10 kΩ
VCC decoupling capacitor	0.1 µF / 100 V
LDO output capacitor	1 µF / 10 V
ILIM_ADJ resistor (R_{SET})	10 kΩ
Maximum Ambient Temperature, T_A	105°C

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Junction Temperature Check

For a 200 mA current limit:

- The maximum driver output current limit, $I_{O(LIM)}$ = 250 mA (allowed for current limit tolerance).
- The maximum voltage drop across the high-side switch is given with $V_{DS(ON)}$ = 1.75 V.

This causes a power consumption of:

$$PD_{OP} = V_{DS(ON)} \, x \, I_{O(LIM)} = 1.75V \, x \, 250 \, mA = 437.5 \, mW \quad (1)$$

For a 5 mA LDO current output,

$$PD_{LDO} = \left(V_{L+} - V_{VCC\_OUT}\right) \text{x } I_{VCC\_OUT} = (30 - 5)\text{V x 5 mA} = 125 \text{ mW} \quad (2)$$

Total power dissipation,

$$PD = PD_{OP} + PD_{LDO} = 437.5 \, mW + 125 \, mW = 562.5 \, mW \quad (3)$$

Multiply this value with the Junction-to-ambient thermal resistance of θ_{JA} = 68.1°C/W (taken from the *Thermal Information* table) to receive the difference between junction temperature, T_J, and ambient temperature, T_A:

$$\Delta T = T_J - T_A = PD \text{ x } \theta_{JA} = 562.5 \, mW \, x \, 68.1°C/W = 38.3°C \quad (4)$$

Add this value to the maximum ambient temperature of T_A = 105°C to receive the final junction temperature:

$$T_{J-max} = T_{A-max} + \Delta T = 105°C + 38.3°C = 143.3°C \quad (5)$$

As long as $T_{J\text{-max}}$ is below the recommended maximum value of 150°C, no thermal shutdown will occur. However, thermal warning may occur as the junction temperature is greater than T_{WRN}.

Note that the modeling of the complete system may be necessary to predict junction temperature in smaller PCBs and/or enclosures without air flow.

9.2.2.2 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the OUT output. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \text{ x } t_{SC}]}{V_{(VCC)}} \quad (6)$$

Higher capacitive loads can be driven if a series resistor is connected between the OUT and the load. Capacitive loads can be connected to VCC and GND.

9.2.2.3 Driving Inductive Loads

The TIOS101 family is capable of magnetizing and demagnetizing inductive loads up to 1.5 H. These devices contain internal circuitry that enables fast demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the OUT pin is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the OUT pin. This voltage is clamped internally at about -75 V.

Similarly in N-switch configuration, the load inductor L is magnetized when the OUT pin is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the OUT pin. This voltage is clamped internally at about 75 V.

The equivalent protection circuits are shown in Figure 15 and Figure 16. The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(VCC)}}{I_{O(LIM)}} \quad (7)$$

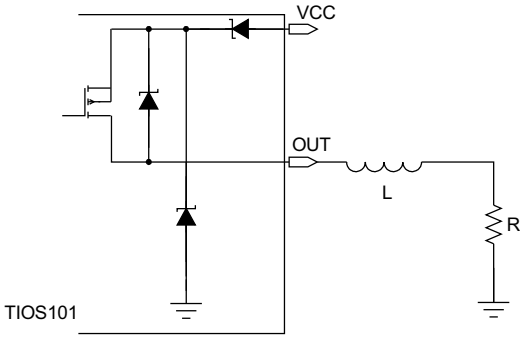


Figure 15. PNP Mode

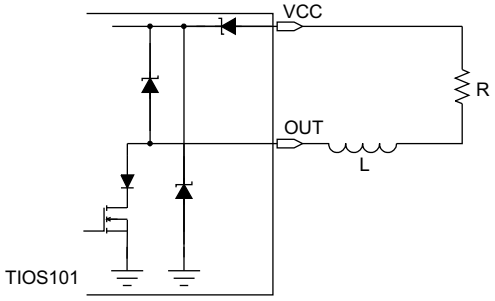


Figure 16. NPN Mode

9.2.3 Application Curves

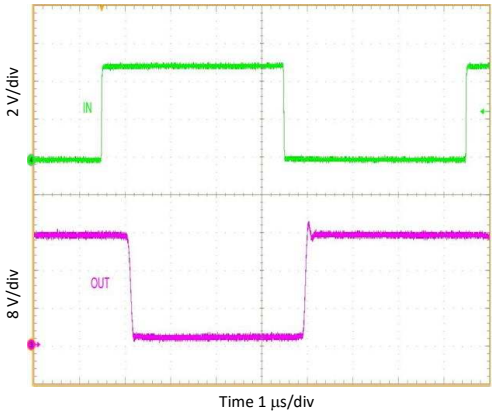


Figure 17. OUT in Push-Pull Mode

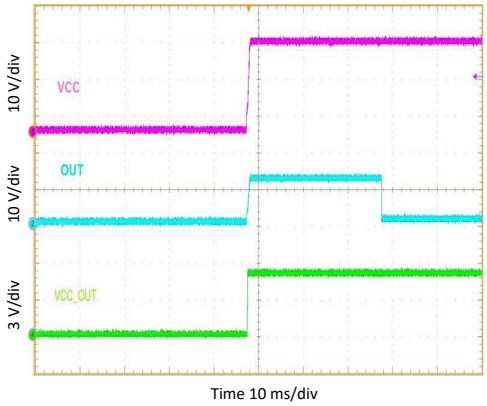


Figure 18. OUT Power Up Delay, Low Side Mode

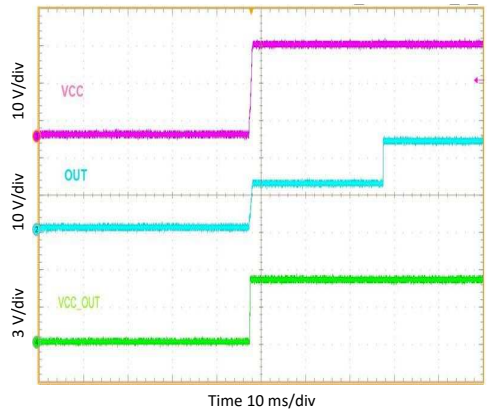


Figure 19. OUT Power Up Delay, High Side Mode

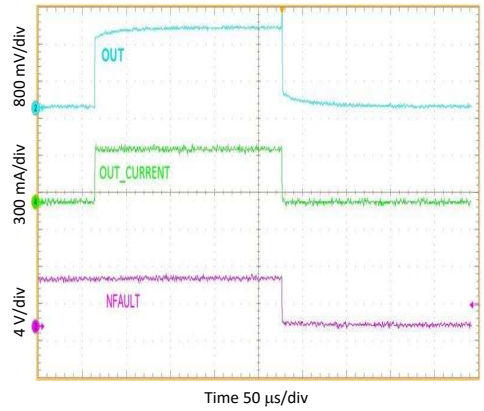


Figure 20. OUT In Current Fault, Low Side Mode

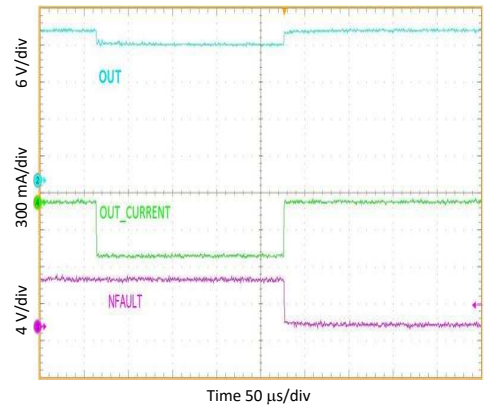


Figure 21. OUT In Current Fault, High Side Mode

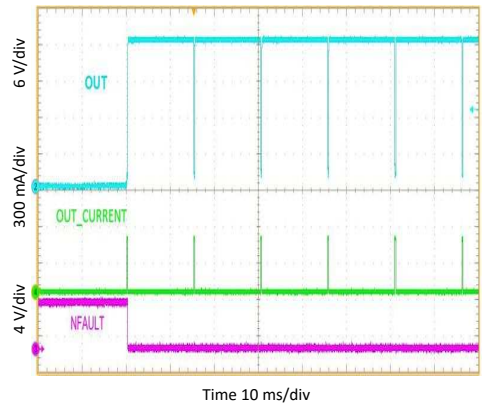


Figure 22. OUT In Current Fault Auto Recovery, Low Side Mode

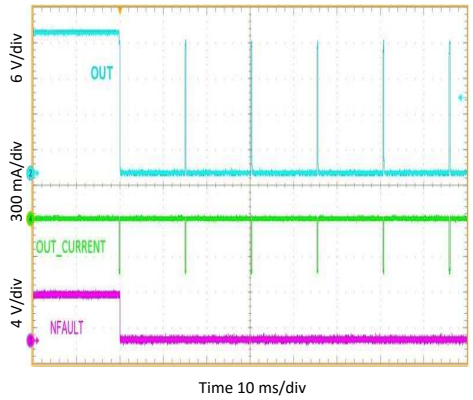
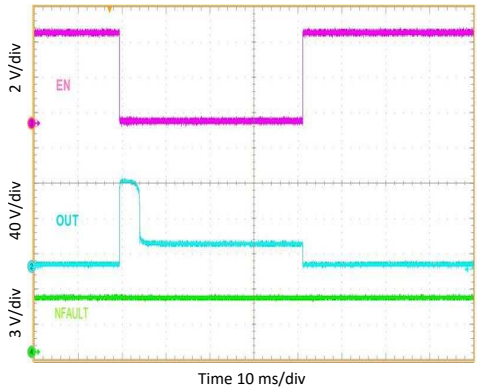
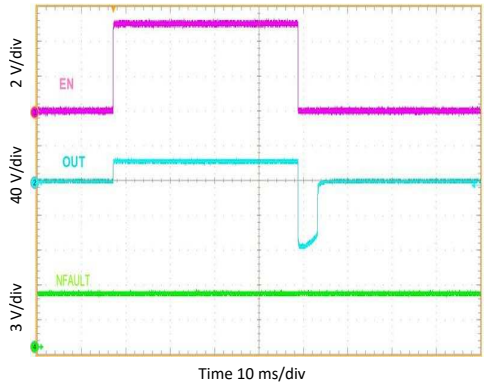


Figure 23. OUT In Current Fault Auto Recovery, High Side Mode



1.5-H Inductor With = 100 Ω R_{SET} = OPEN

Figure 24. OUT Driving, Low Side Mode



1.5-H Inductor With = 100 Ω R_{SET} = OPEN

Figure 25. OUT Driving, High Side Mode

10 Power Supply Recommendations

The TIOS101 and TIOS101-x are designed to operate from a 24-V nominal supply at VCC, which can vary by +12 V and -17 V from the nominal value to remain within the device's recommended supply voltage range of 7 V to 36 V. This supply should be buffered with at least a 100-nF/100-V capacitor.

11 Layout

11.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as GND, layer 3 for the 24-V supply plane (VCC), and layer 4 for the regulated output supply (VCC_IN/OUT).
- Connect the thermal pad to GND with maximum amount of thermal vias for best thermal performance.
- Use entire planes for VCC, VCC_IN/OUT and GND to assure minimum inductance.
- The VCC terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor with a minimum value of 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- • The optimum placement of the capacitor is closest to the VCC and GND terminals to reduce supply drops during large supply current loads. See Figure 26 for a PCB layout example.
- Connect all open-drain control outputs via 10 kΩ pull-up resistors to the VCC_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R_{SET} resistor between ILIM_ADJ and GND.
- Decouple the regulated output voltage at VCC_IN/OUT to ground with a low-ESR, 1 µF, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

11.2 Layout Example

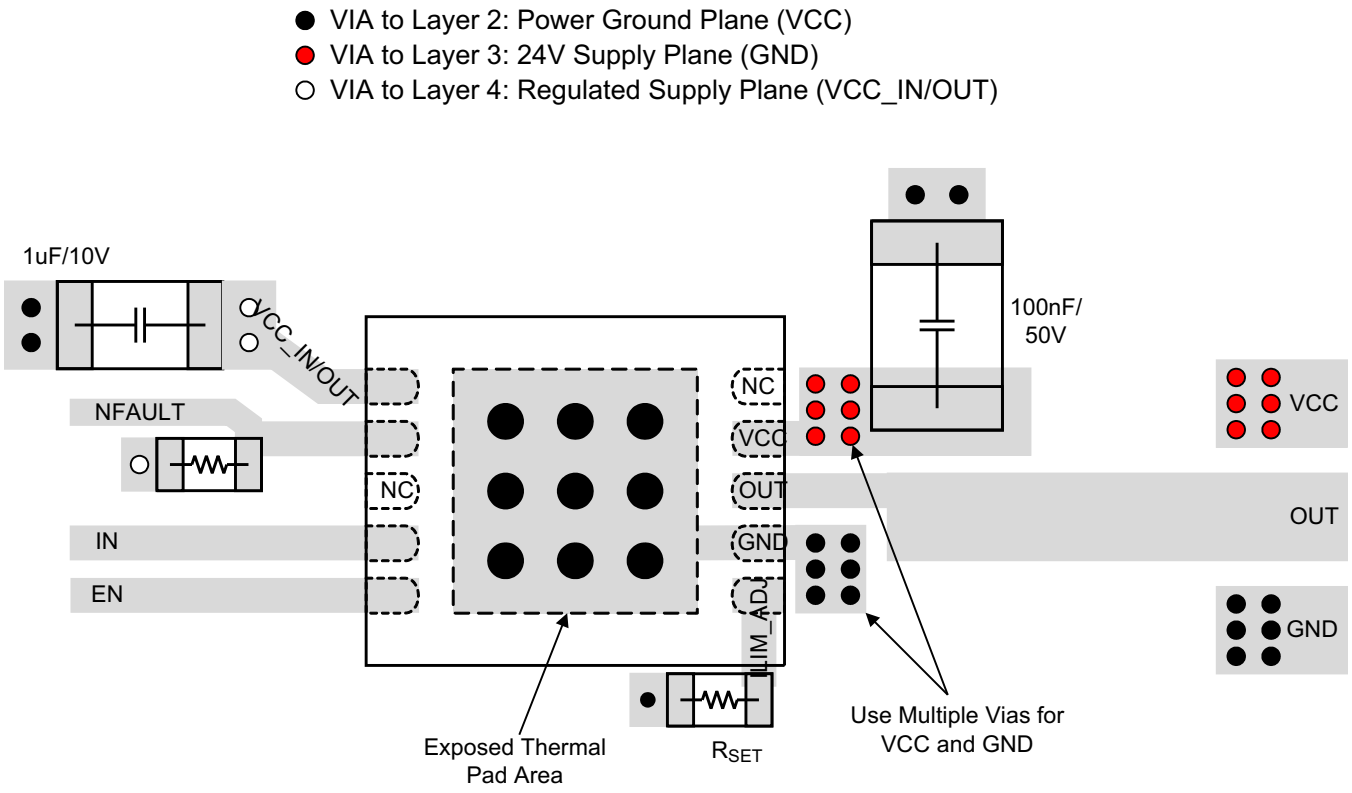


Figure 26. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIOS1013DMWR	ACTIVE	VSON	DMW	10	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1013	Samples
TIOS1013DMWT	ACTIVE	VSON	DMW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1013	Samples
TIOS1015DMWR	ACTIVE	VSON	DMW	10	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1015	Samples
TIOS1015DMWT	ACTIVE	VSON	DMW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1015	Samples
TIOS101DMWR	ACTIVE	VSON	DMW	10	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS101	Samples
TIOS101DMWT	ACTIVE	VSON	DMW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS101	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

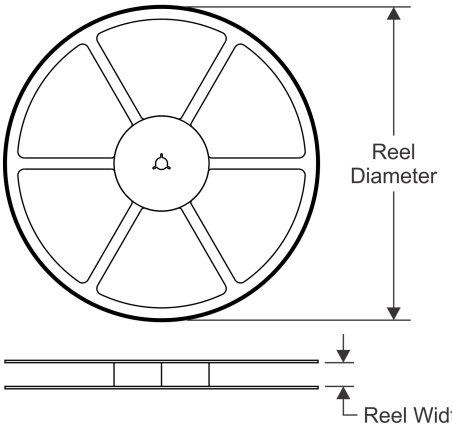
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

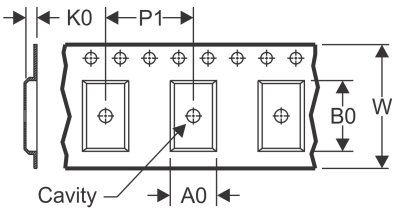
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

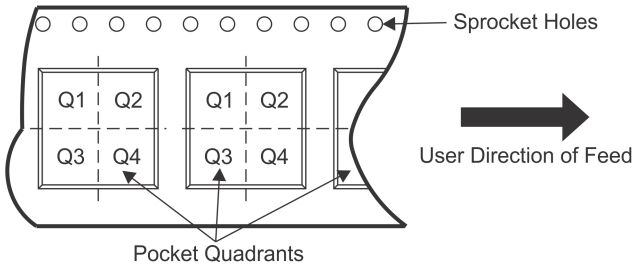


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

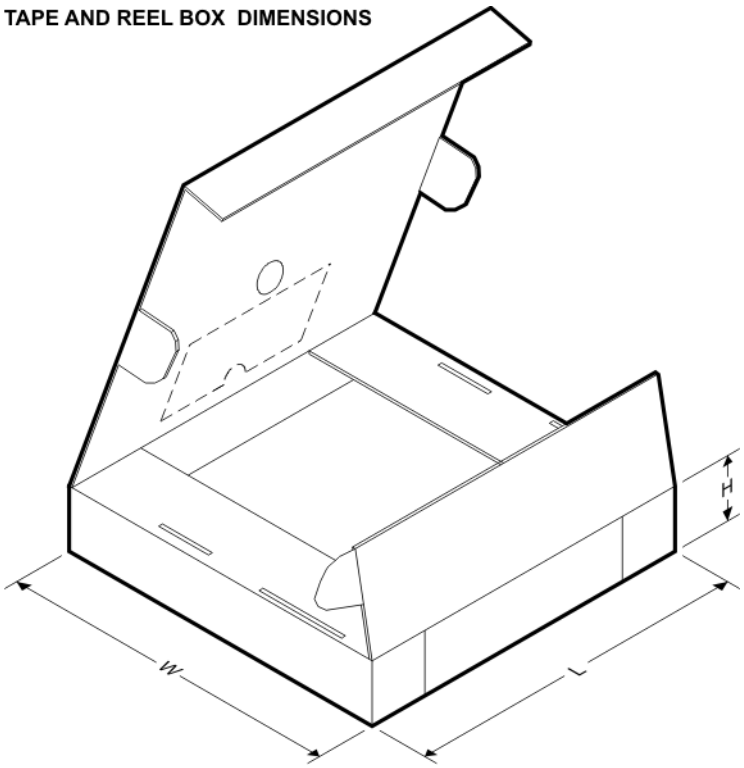
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

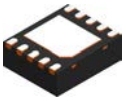
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOS1013DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS1013DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS1015DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS1015DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS101DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS101DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOS1013DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOS1013DMWT	VSON	DMW	10	250	189.0	185.0	36.0
TIOS1015DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOS1015DMWT	VSON	DMW	10	250	189.0	185.0	36.0
TIOS101DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOS101DMWT	VSON	DMW	10	250	189.0	185.0	36.0

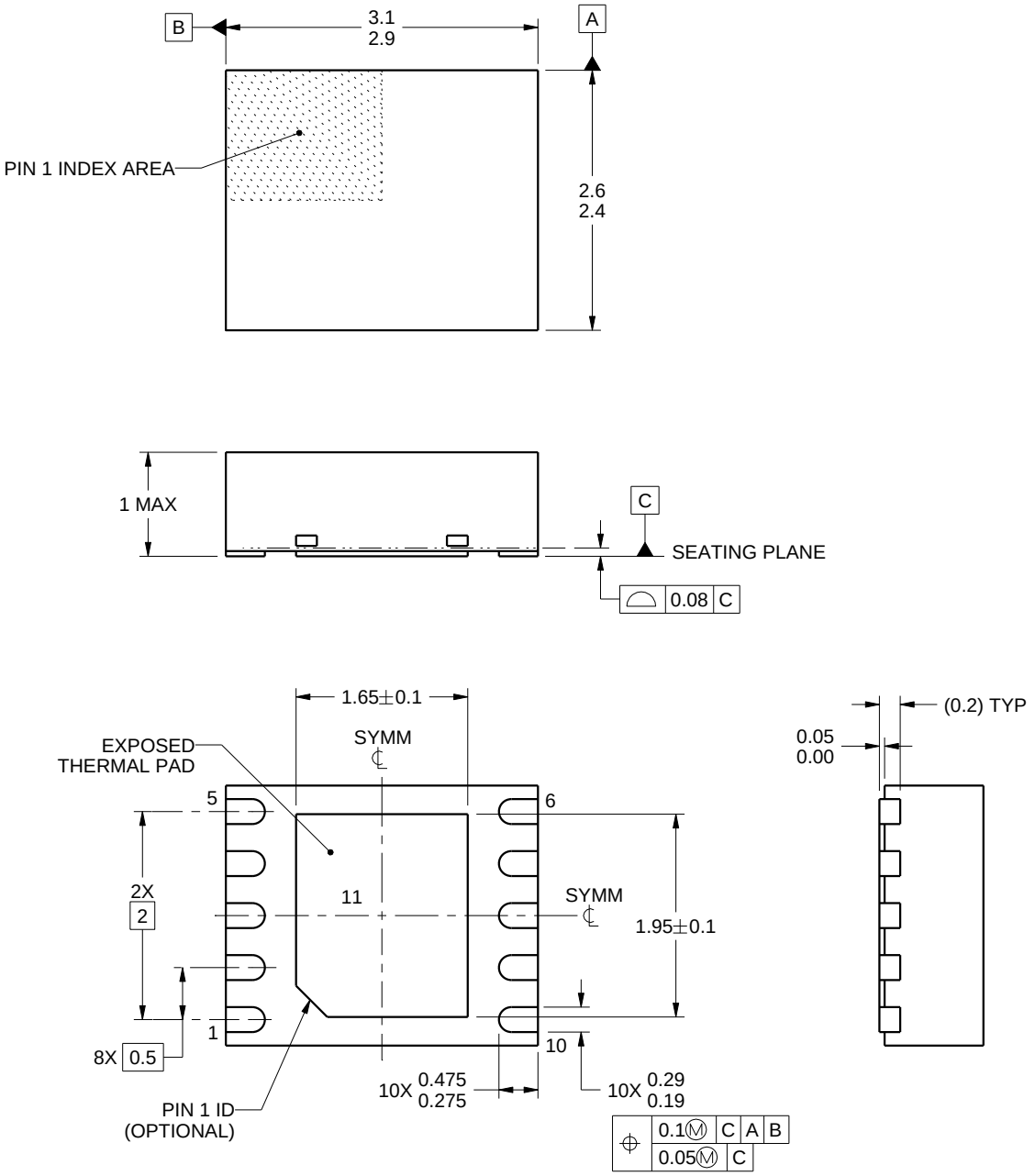


PACKAGE OUTLINE

DMW0010A

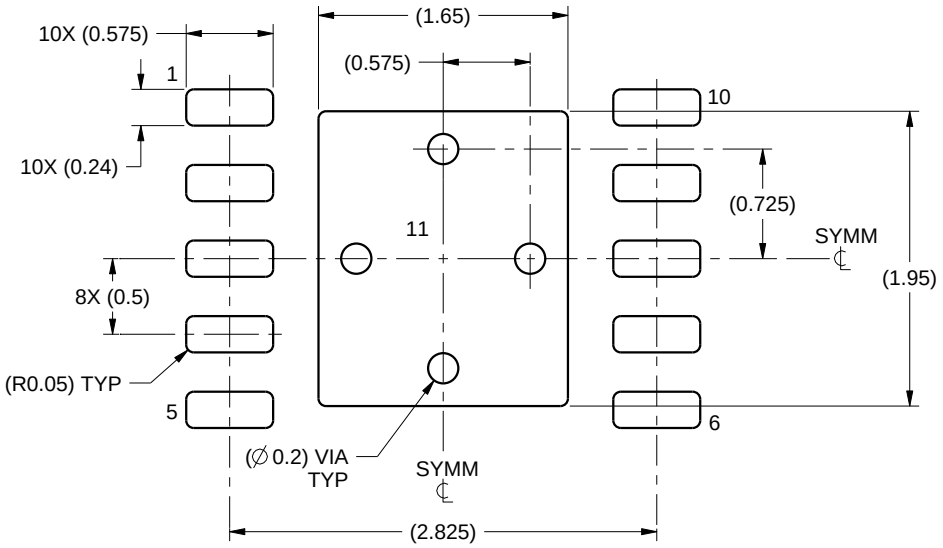
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

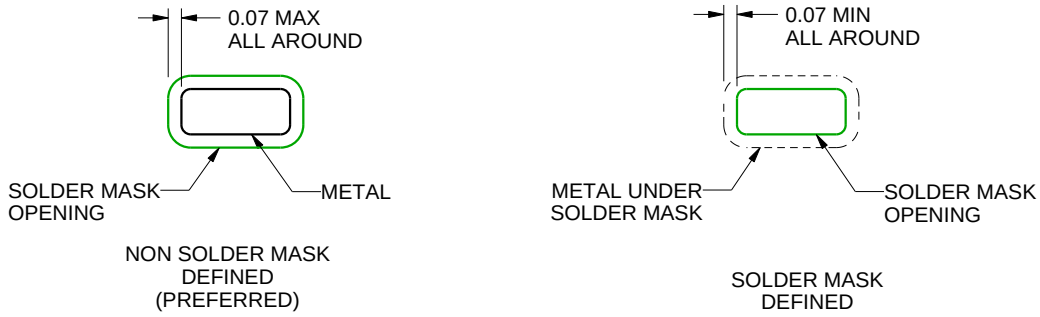


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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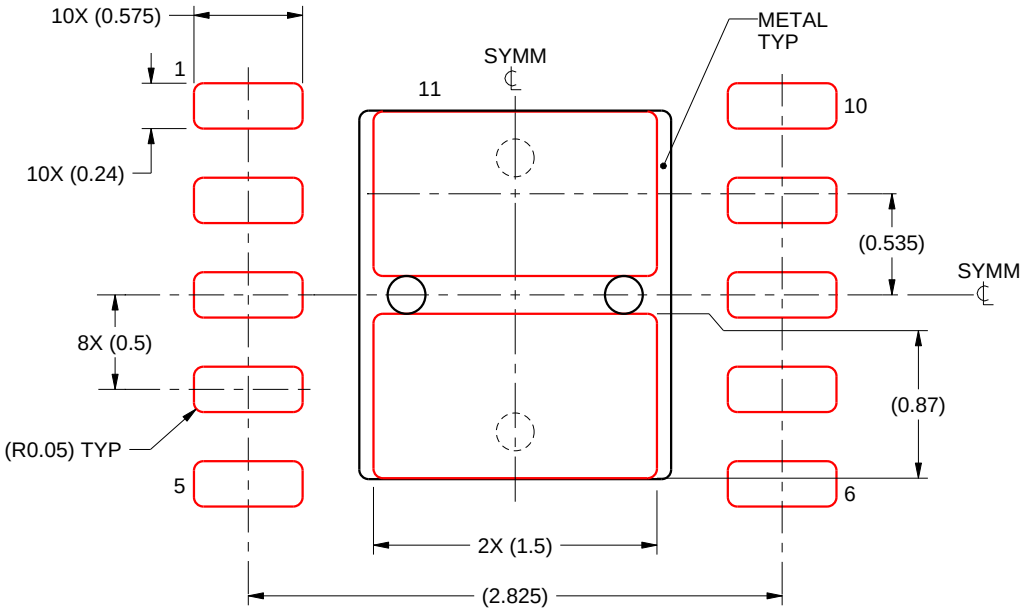
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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