

## LP5912-Q1 汽车类 500mA 低噪声、低 I<sub>Q</sub> LDO

### 1 特性

- 适用于汽车电子 应用
- 具有符合 AEC Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 分类等级 2
  - 器件组件充电模式 (CDM) 分类等级 C6
- 输入电压范围：1.6V 至 6.5V
- 输出电压范围：0.8V 至 5.5V
- 输出电流最高达 500 mA
- 低输出电压噪声：12μV<sub>RMS</sub> 典型值
- 1kHz 时的电源抑制比 (PSRR)：75dB (典型值)
- 输出电压容差 (V<sub>OUT</sub> ≥ 3.3V)：±2%
- 低 I<sub>Q</sub> (使能时，无负载)：30μA (典型值)
- 低压降 (V<sub>OUT</sub> ≥ 3.3V)：500mA 负载时典型值为 95mV
- 与 1μF 陶瓷输入和输出电容搭配使用，性能稳定
- 热过载保护和短路保护
- 反向电流保护
- 无需噪声旁路电容
- 自动输出放电实现快速关断
- 电源正常状态输出具有 140μs 典型延迟
- 内部软启动限制浪涌电流
- -40°C 至 +125°C 的运行结温范围

### 2 应用

- 车用信息娱乐
- 车载通讯系统
- 高级驾驶员辅助系统 (ADAS) 摄像机和雷达
- 导航系统

### 3 说明

LP5912-Q1 是一款能提供高达 500mA 输出电流的低噪声 LDO。LP5912-Q1 器件专为满足射频 (RF) 和模拟电路的要求而设计，具备低噪声、高 PSRR、低静态电流以及低线路或负载瞬态响应等特性。LP5912-Q1 无需噪声旁路电容便可提供出色的噪声性能，并且支持远距离安置输出电容。

此器件适合与 1μF 输入和 1μF 输出陶瓷电容搭配使用 (无需独立的噪声旁路电容)。

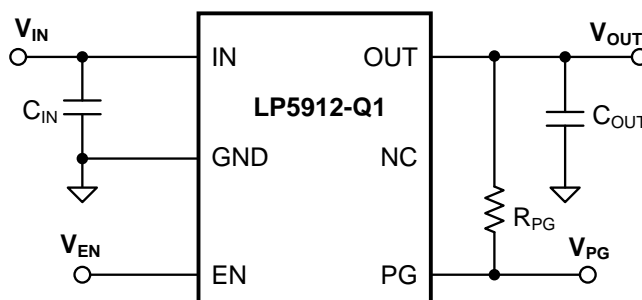
其固定输出电压介于 0.8V 和 5.5V 之间 (以 25mV 为单位增量)。如需特定的电压选项，请联系德州仪器 (TI) 销售代表。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
LP5912-Q1	WSON (6)	2.00mm x 2.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录 (POA)。

简化电路原理图



Copyright © 2016, Texas Instruments Incorporated



## 目录

<b>1</b>	特性 .....	<b>1</b>	8.3	Feature Description .....	<b>17</b>
<b>2</b>	应用 .....	<b>1</b>	8.4	Device Functional Modes .....	<b>19</b>
<b>3</b>	说明 .....	<b>1</b>	<b>9</b>	<b>Applications and Implementation</b> .....	<b>20</b>
<b>4</b>	修订历史记录 .....	<b>2</b>	9.1	Application Information .....	<b>20</b>
<b>5</b>	<b>Voltage Options</b> .....	<b>3</b>	9.2	Typical Application .....	<b>20</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>23</b>
<b>7</b>	<b>Specifications</b> .....	<b>4</b>	<b>11</b>	<b>Layout</b> .....	<b>24</b>
7.1	Absolute Maximum Ratings .....	<b>4</b>	11.1	Layout Guidelines .....	<b>24</b>
7.2	ESD Ratings .....	<b>4</b>	11.2	Layout Example .....	<b>24</b>
7.3	Recommended Operating Conditions .....	<b>4</b>	<b>12</b>	<b>器件和文档支持</b> .....	<b>25</b>
7.4	Thermal Information .....	<b>4</b>	12.1	相关文档 .....	<b>25</b>
7.5	Electrical Characteristics .....	<b>5</b>	12.2	接收文档更新通知 .....	<b>25</b>
7.6	Output and Input Capacitors .....	<b>7</b>	12.3	社区资源 .....	<b>25</b>
7.7	Typical Characteristics .....	<b>8</b>	12.4	商标 .....	<b>25</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>17</b>	12.5	静电放电警告 .....	<b>25</b>
8.1	Overview .....	<b>17</b>	12.6	Glossary .....	<b>25</b>
8.2	Functional Block Diagram .....	<b>17</b>	<b>13</b>	<b>机械、封装和可订购信息</b> .....	<b>25</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision B (June 2016) to Revision C</b>	<b>Page</b>
• 已更改 数据表标题和 列表的措辞应用 .....	<b>1</b>
• 已更改 的第一句的措辞说明 .....	<b>1</b>

<b>Changes from Revision A (April 2016) to Revision B</b>	<b>Page</b>
• 已更改 第 1 页的“线性稳压器”改为“LDO” .....	<b>1</b>

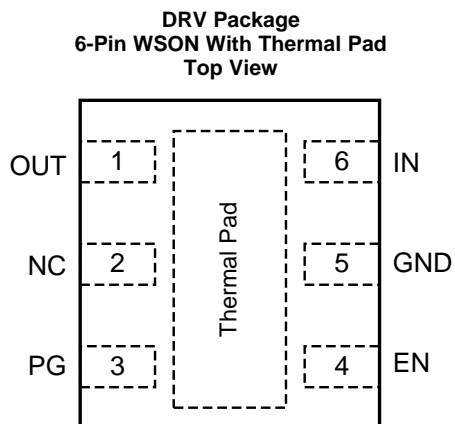
  

<b>Changes from Original (December 2015) to Revision A</b>	<b>Page</b>
• 已更改 器件状态从“预览”改为“量产数据” .....	<b>1</b>
• Changed Block Diagram .....	<b>17</b>

## 5 Voltage Options

This device is capable of providing fixed output voltages from 0.8 V to 5.5 V in 25-mV steps. For all available package and voltage options, see the POA at the end of this datasheet. Contact Texas Instruments Sales for specific voltage option needs.

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Regulated output voltage
2	NC	—	No internal connection. Leave open, or connect to ground.
3	PG	O	Power-good indicator. Requires external pullup.
4	EN	I	Enable input. Logic high = device is ON, logic low = device is OFF, with internal 3-M $\Omega$ pulldown.
5	GND	G	Ground
6	IN	I	Unregulated input voltage
—	Exposed thermal pad	—	Connect to copper area under the package to improve thermal performance. The use of thermal vias to transfer heat to inner layers of the PCB is recommended. Connect the thermal pad to ground, or leave floating. Do not connect the thermal pad to any potential other than ground.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	-0.3	7	V
V <sub>OUT</sub>	Output voltage	-0.3	7	V
V <sub>EN</sub>	Enable input voltage	-0.3	7	V
V <sub>PG</sub>	Power Good (PG) pin OFF voltage	-0.3	7	V
T <sub>J</sub>	Junction temperature		150	°C
P <sub>D</sub>	Continuous power dissipation <sup>(3)</sup>	Internally Limited		W
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) Internal thermal shutdown circuitry protects the device from permanent damage.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input supply voltage	1.6	6.5	V
V <sub>OUT</sub>	Output voltage	0.8	5.5	V
V <sub>EN</sub>	Enable input voltage	0	V <sub>IN</sub>	V
V <sub>PG</sub>	PG pin OFF voltage	0	6.5	V
I <sub>OUT</sub>	Output current	0	500	mA
T <sub>J-MAX-OP</sub>	Operating junction temperature <sup>(2)</sup>	-40	125	°C

- (1) All voltages are with respect to the GND pin.
- (2)  $T_{J-MAX-OP} = (T_{A(MAX)} + (P_{D(MAX)} \times R_{\theta JA}))$ .

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LP5912-Q1	UNIT	
	DRV (WSON)		
	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance, High-K <sup>(2)</sup>	71.2 <sup>(3)</sup>	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	93.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	40.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	41.1	°C/W
ψ <sub>JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	11.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Thermal resistance value R<sub>θJA</sub> is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- (3) The PCB for the WSON (DRV) package R<sub>θJA</sub> includes two (2) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

## 7.5 Electrical Characteristics

$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.6\text{ V}$ , whichever is greater;  $V_{EN} = 1.3\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $I_{OUT} = 1\text{ mA}$  (unless otherwise stated).<sup>(1)(2)(3)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT VOLTAGE</b>						
$\Delta V_{OUT}$	Output voltage tolerance	For $V_{OUT(NOM)} \geq 3.3\text{ V}$ : $V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $I_{OUT} = 1\text{ mA to }500\text{ mA}$	-2%		2%	
		For $1.1\text{ V} \leq V_{OUT(NOM)} < 3.3\text{ V}$ : $V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $I_{OUT} = 1\text{ mA to }500\text{ mA}$	-3%		3%	
		For $V_{OUT(NOM)} < 1.1\text{ V}$ : $1.6\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $I_{OUT} = 1\text{ mA to }500\text{ mA}$				
	Line regulation	For $V_{OUT(NOM)} \geq 1.1\text{ V}$ : $V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$		0.8		%V
For $V_{OUT(NOM)} < 1.1\text{ V}$ : $1.6\text{ V} \leq V_{IN} \leq 6.5\text{ V}$						
	Load regulation	$I_{OUT} = 1\text{ mA to }500\text{ mA}$		0.0022		%/mA
<b>CURRENT LEVELS</b>						
$I_{SC}$	Short-circuit current limit	$T_J = 25^\circ\text{C}$ , see <sup>(4)</sup>	700	900	1100	mA
$I_{RO}$	Reverse leakage current <sup>(5)</sup>	$V_{IN} < V_{OUT}$		10	150	$\mu\text{A}$
$I_Q$	Quiescent current <sup>(6)</sup>	$V_{EN} = 1.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$		30	55	$\mu\text{A}$
		$V_{EN} = 1.3\text{ V}$ , $I_{OUT} = 500\text{ mA}$		400	600	
$I_{Q(SD)}$	Quiescent current, shutdown mode <sup>(6)</sup>	$V_{EN} = 0\text{ V}$ $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$		0.2	1.5	$\mu\text{A}$
		$V_{EN} = 0\text{ V}$		0.2	5	
$I_G$	Ground current <sup>(7)</sup>	$V_{EN} = 1.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$		35		$\mu\text{A}$
<b><math>V_{DO}</math> DROPOUT VOLTAGE</b>						
$V_{DO}$	Dropout voltage <sup>(8)</sup>	$I_{OUT} = 500\text{ mA}$ , $1.6\text{ V} \leq V_{OUT(NOM)} < 3.3\text{ V}$		170	250	mV
		$I_{OUT} = 500\text{ mA}$ , $3.3\text{ V} \leq V_{OUT(NOM)} \leq 5.5\text{ V}$		95	180	mV

- (1) All voltages are with respect to the device GND pin, unless otherwise stated.
- (2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise stated. Typical values represent the most likely parametric norm at  $T_A = 25^\circ\text{C}$ , and are provided for reference purposes only.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^\circ\text{C}$ ), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to-ambient thermal resistance of the part/package in the application ( $R_{\theta JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$ .
- (4) Short-circuit current ( $I_{SC}$ ) is equivalent to current limit. To minimize thermal effects during testing,  $I_{SC}$  is measured with  $V_{OUT}$  pulled to 100 mV below its nominal voltage.
- (5) Reverse current ( $I_{RO}$ ) is measured at the IN pin.
- (6) Quiescent current is defined here as the difference in current between the input voltage source and the load at  $V_{OUT}$ .
- (7) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device ( $I_Q + I_{EN}$ ).
- (8) Dropout voltage ( $V_{DO}$ ) is the voltage difference between the input and the output at which the output voltage drops to 150 mV below its nominal value when  $V_{IN} = V_{OUT} + 0.5\text{ V}$ . Dropout voltage is not a valid condition for output voltages less than 1.6 V as compliance with the minimum operating voltage requirement cannot be assured.

**Electrical Characteristics (continued)**
 $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.6\text{ V}$ , whichever is greater;  $V_{EN} = 1.3\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $I_{OUT} = 1\text{ mA}$  (unless otherwise stated).<sup>(1)(2)(3)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b><math>V_{IN}</math> to <math>V_{OUT}</math> RIPPLE REJECTION</b>						
PSRR	Power Supply Rejection Ratio <sup>(9)</sup>	$f = 100\text{ Hz}$ , $V_{OUT} \geq 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		80		dB
		$f = 1\text{ kHz}$ , $V_{OUT} \geq 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		75		
		$f = 10\text{ kHz}$ , $V_{OUT} \geq 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		65		
		$f = 100\text{ kHz}$ , $V_{OUT} \geq 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		40		
		$f = 100\text{ Hz}$ , $0.8\text{ V} < V_{OUT} < 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		65		
		$f = 1\text{ kHz}$ , $0.8\text{ V} < V_{OUT} < 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		65		
		$f = 10\text{ kHz}$ , $0.8\text{ V} < V_{OUT} < 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		65		
		$f = 100\text{ kHz}$ , $0.8\text{ V} < V_{OUT} < 1.1\text{ V}$ , $I_{OUT} = 20\text{ mA}$		40		
<b>OUTPUT NOISE VOLTAGE</b>						
$e_N$	Noise voltage	$I_{OUT} = 1\text{ mA}$ , BW = 10 Hz to 100 kHz		12		$\mu\text{V}_{RMS}$
		$I_{OUT} = 500\text{ mA}$ , BW = 10 Hz to 100 kHz		12		
<b>THERMAL SHUTDOWN</b>						
$T_{SD}$	Thermal shutdown temperature			160		$^{\circ}\text{C}$
$T_{HYS}$	Thermal shutdown hysteresis			15		$^{\circ}\text{C}$
<b>LOGIC INPUT THRESHOLDS</b>						
$V_{EN(OFF)}$	OFF threshold	$V_{IN} = 1.6\text{ V}$ to $6.5\text{ V}$ $V_{EN}$ falling until device is disabled			0.3	V
$V_{EN(ON)}$	ON threshold	$1.6\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ $V_{EN}$ rising until device is enabled	1.3			
$I_{EN}$	Input current at EN pin <sup>(10)</sup>	$V_{EN} = 6.5\text{ V}$ , $V_{IN} = 6.5\text{ V}$		2.5		$\mu\text{A}$
		$V_{EN} = 0\text{ V}$ , $V_{IN} = 3.3\text{ V}$		0.001		
$PG_{HTH}$	PG high threshold (% of nominal $V_{OUT}$ )			94%		
$PG_{LTH}$	PG low threshold (% of nominal $V_{OUT}$ )			90%		
$V_{OL(PG)}$	PG pin low-level output voltage	$V_{OUT} < PG_{LTH}$ , sink current = 1 mA			100	mV
$I_{IKG(PG)}$	PG pin leakage current	$V_{OUT} < PG_{HTH}$ , $V_{PG} = 6.5\text{ V}$			1	$\mu\text{A}$
$t_{PGD}$	PG delay time	Time from $V_{OUT} > PG$ threshold to PG toggling		140		$\mu\text{s}$

(9) This specification is ensured by design.

(10) There is a 3-M $\Omega$  pulldown resistor between the EN pin and GND pin on the device.

## Electrical Characteristics (continued)

 $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.6\text{ V}$ , whichever is greater;  $V_{EN} = 1.3\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $I_{OUT} = 1\text{ mA}$  (unless otherwise stated).<sup>(1)(2)(3)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TRANSITION CHARACTERISTICS</b>						
$\Delta V_{OUT}$	Line transients <sup>(9)</sup>	For $V_{IN} \uparrow$ and $V_{OUT(NOM)} \geq 1.1\text{ V}$ : $V_{IN} = (V_{OUT(NOM)} + 0.5\text{ V})$ to $(V_{OUT(NOM)} + 1.1\text{ V})$ , $V_{IN} t_{rise} = 30\text{ }\mu\text{s}$			1	mV
		For $V_{IN} \uparrow$ and $V_{OUT(NOM)} < 1.1\text{ V}$ : $V_{IN} = 1.6\text{ V}$ to $2.2\text{ V}$ , $V_{IN} t_{rise} = 30\text{ }\mu\text{s}$				
		For $V_{IN} \downarrow$ and $V_{OUT(NOM)} \geq 1.1\text{ V}$ : $V_{IN} = (V_{OUT(NOM)} + 1.1\text{ V})$ to $(V_{OUT(NOM)} + 0.5\text{ V})$ $V_{IN} t_{fall} = 30\text{ }\mu\text{s}$	-1			
		For $V_{IN} \downarrow$ and $V_{OUT(NOM)} < 1.1\text{ V}$ : $V_{IN} = 2.2\text{ V}$ to $1.6\text{ V}$ $V_{IN} t_{fall} = 30\text{ }\mu\text{s}$				
	Load transients <sup>(9)</sup>	$I_{OUT} = 5\text{ mA}$ to $500\text{ mA}$ $I_{OUT} t_{rise} = 10\text{ }\mu\text{s}$	-45			mV
$I_{OUT} = 500\text{ mA}$ to $5\text{ mA}$ $I_{OUT} t_{fall} = 10\text{ }\mu\text{s}$				45		
	Overshoot on start-up <sup>(9)</sup>	Stated as a percentage of $V_{OUT(NOM)}$			5%	
$t_{ON}$	Turnon time	From $V_{EN} > V_{EN(ON)}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$		200		$\mu\text{s}$
<b>OUTPUT AUTO DISCHARGE RATE</b>						
$R_{AD}$	Output discharge pulldown resistance	$V_{EN} = 0\text{ V}$ , $V_{IN} = 3.6\text{ V}$		100		$\Omega$

## 7.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP	MAX	UNIT
$C_{IN}$	Input capacitance <sup>(2)</sup>	Capacitance for stability	0.7	1		$\mu\text{F}$
$C_{OUT}$	Output capacitance <sup>(2)</sup>		0.7	1	10	$\mu\text{F}$
ESR	Output voltage <sup>(2)</sup>		5		500	$\text{m}\Omega$

(1) The minimum capacitance must be greater than  $0.5\text{ }\mu\text{F}$  over full range of operating conditions. The capacitor tolerance must be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application must be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V, and Z5U may be used with consideration of the application conditions.

(2) This specification is verified by design.

### 7.7 Typical Characteristics

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

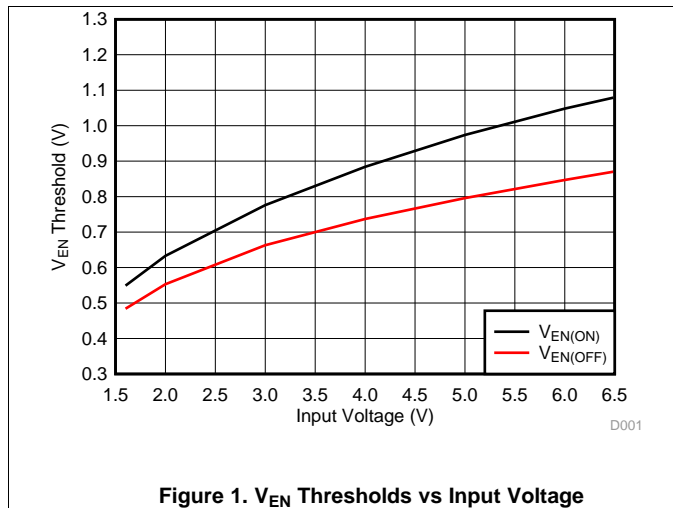


Figure 1.  $V_{EN}$  Thresholds vs Input Voltage

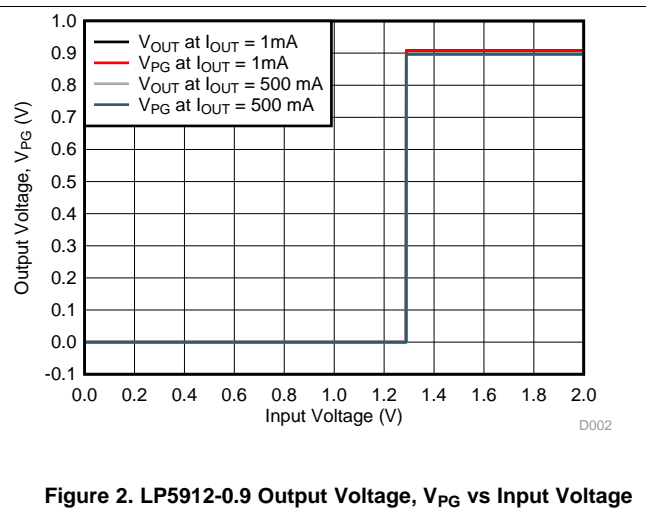


Figure 2. LP5912-0.9 Output Voltage,  $V_{PG}$  vs Input Voltage

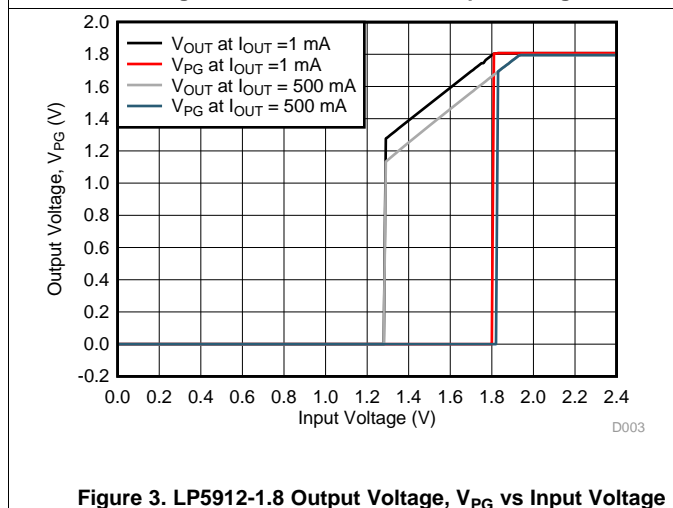


Figure 3. LP5912-1.8 Output Voltage,  $V_{PG}$  vs Input Voltage

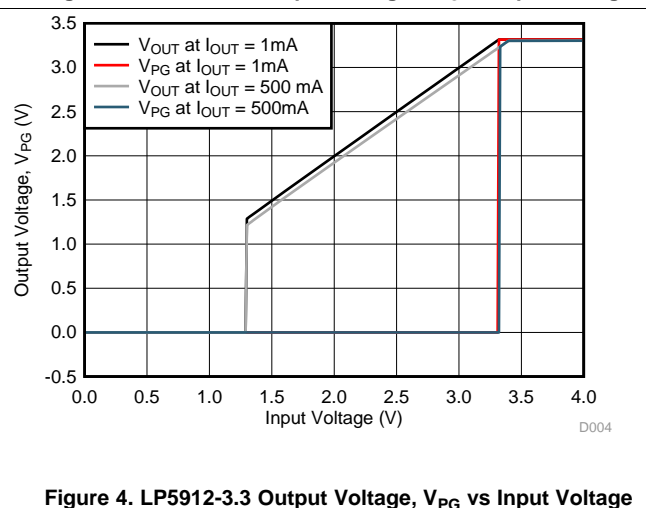


Figure 4. LP5912-3.3 Output Voltage,  $V_{PG}$  vs Input Voltage

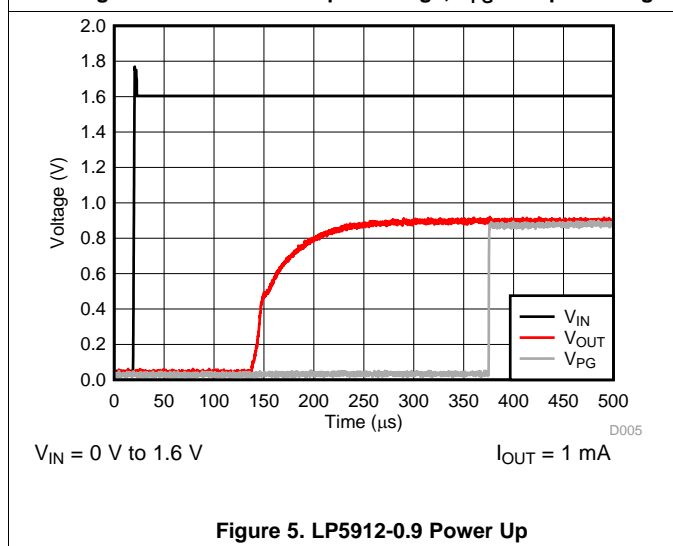


Figure 5. LP5912-0.9 Power Up

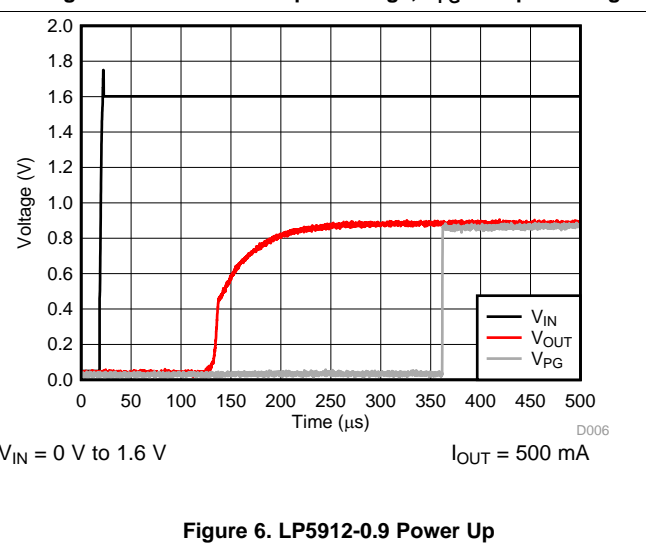


Figure 6. LP5912-0.9 Power Up



Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

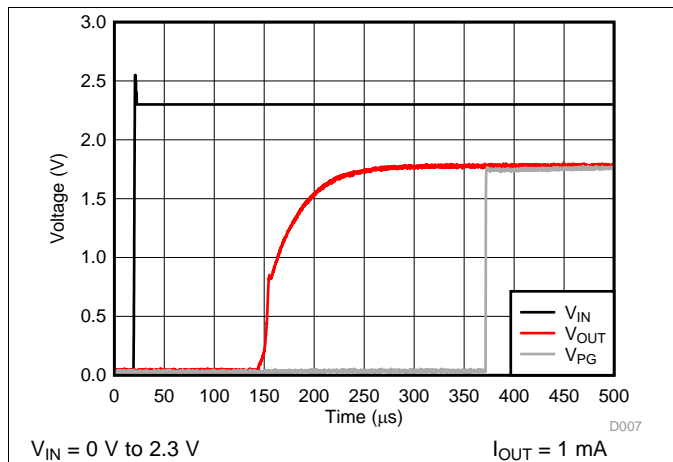


Figure 7. LP5912-1.8 Power Up

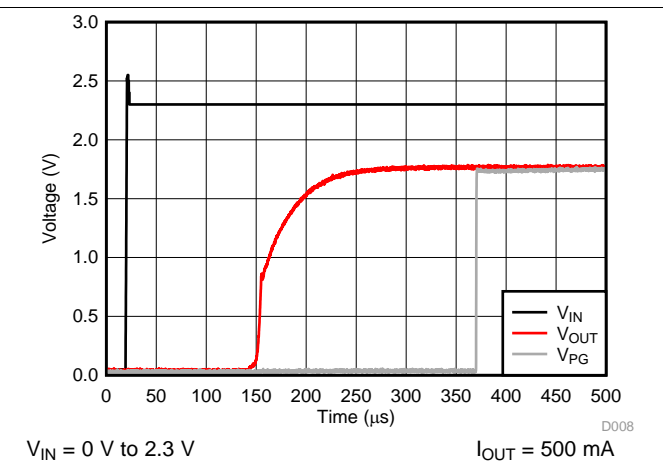


Figure 8. LP5912-1.8 Power Up

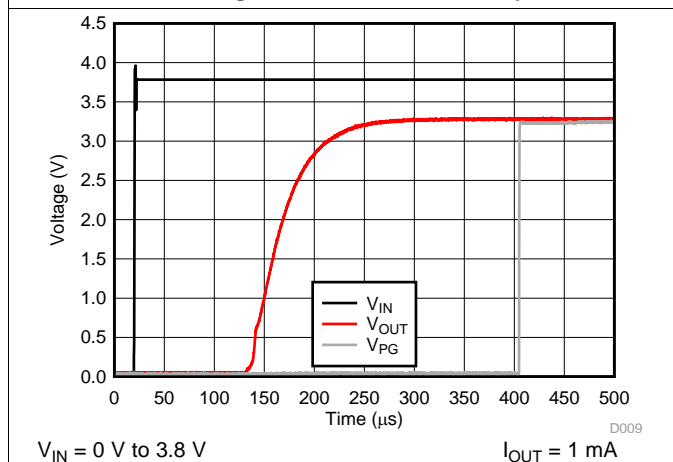


Figure 9. LP5912-3.3 Power Up

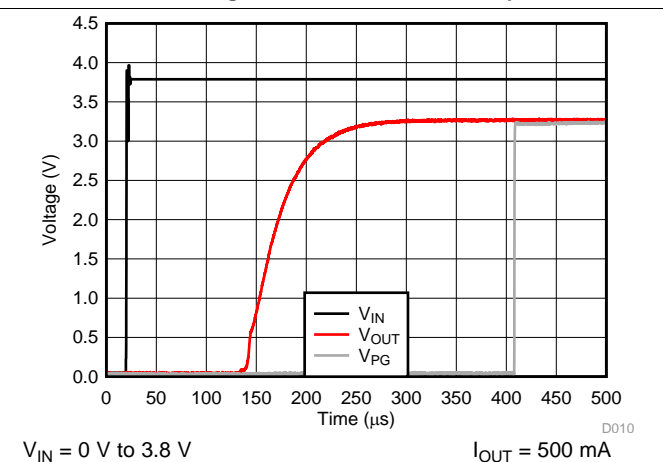


Figure 10. LP5912-3.3 Power Up

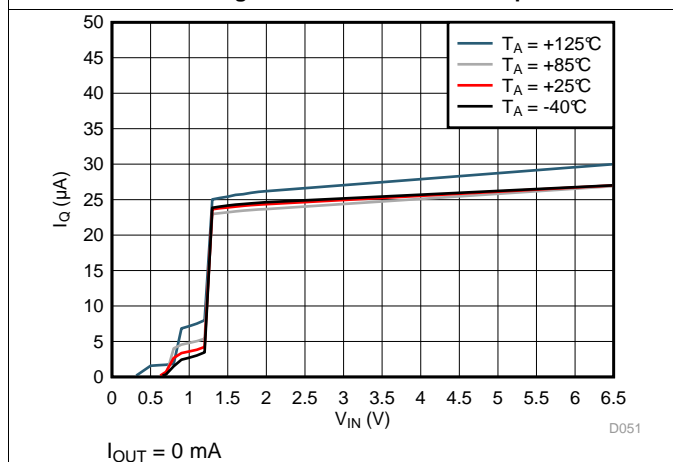


Figure 11. LP5912-0.9  $I_Q$  (No Load) vs  $V_{IN}$

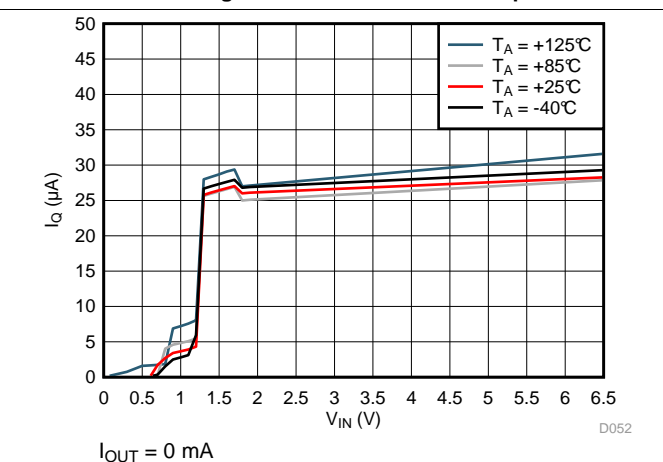


Figure 12. LP5912-1.8  $I_Q$  (No Load) vs  $V_{IN}$

Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

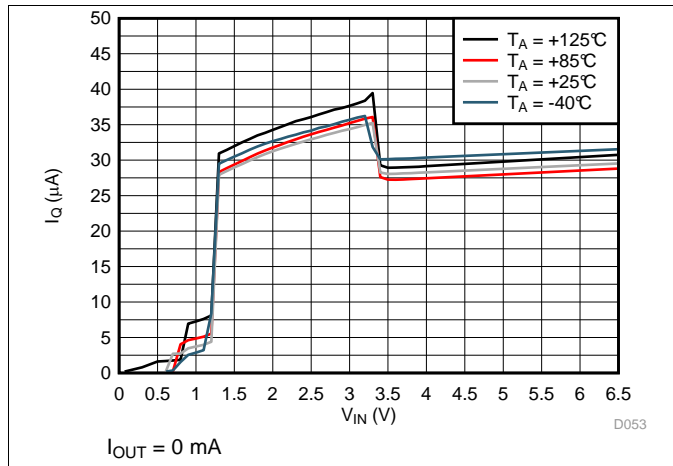


Figure 13. LP5912-3.3  $I_Q$  (No Load) vs  $V_{IN}$

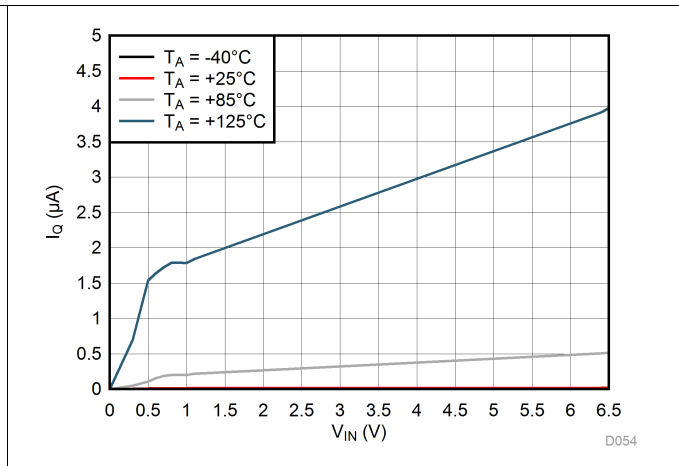


Figure 14. LP5912-0.9  $I_{Q(SD)}$  vs  $V_{IN}$

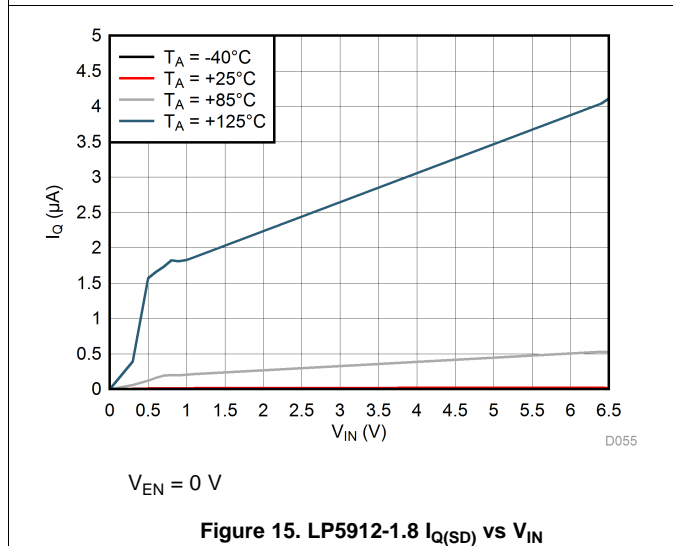


Figure 15. LP5912-1.8  $I_{Q(SD)}$  vs  $V_{IN}$

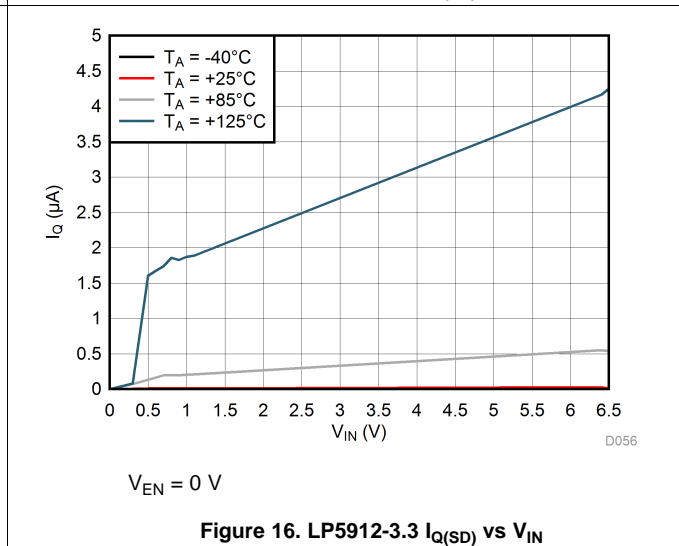


Figure 16. LP5912-3.3  $I_{Q(SD)}$  vs  $V_{IN}$

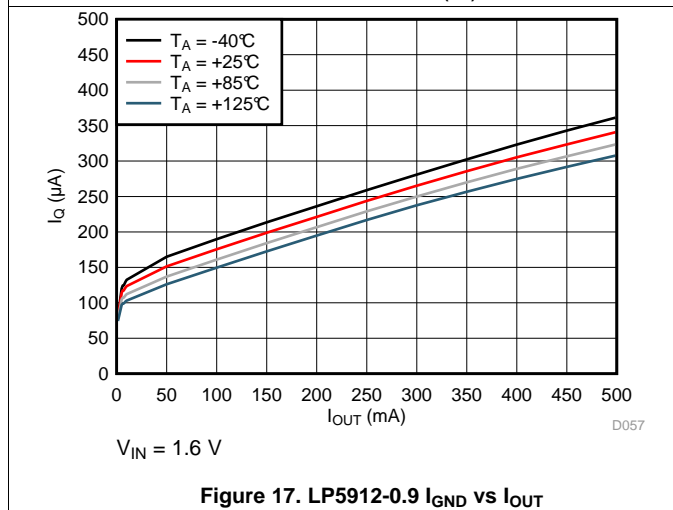


Figure 17. LP5912-0.9  $I_{GND}$  vs  $I_{OUT}$

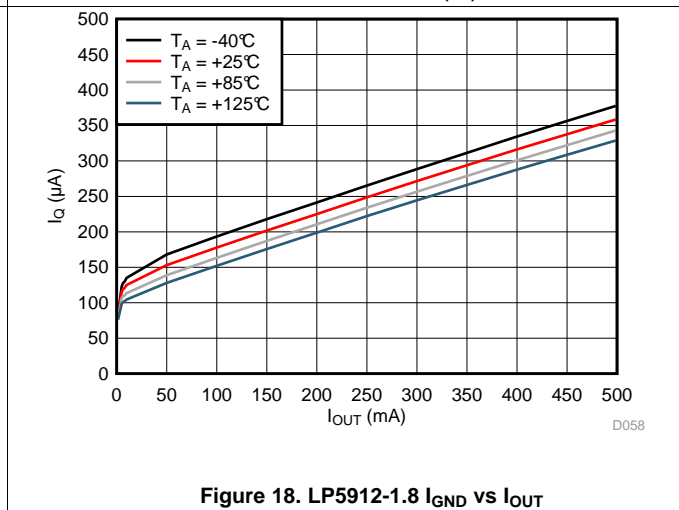


Figure 18. LP5912-1.8  $I_{GND}$  vs  $I_{OUT}$

Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

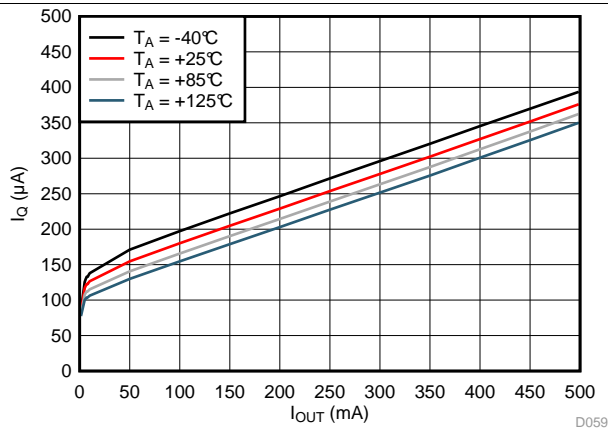


Figure 19. LP5912-3.3  $I_{GND}$  vs  $I_{OUT}$

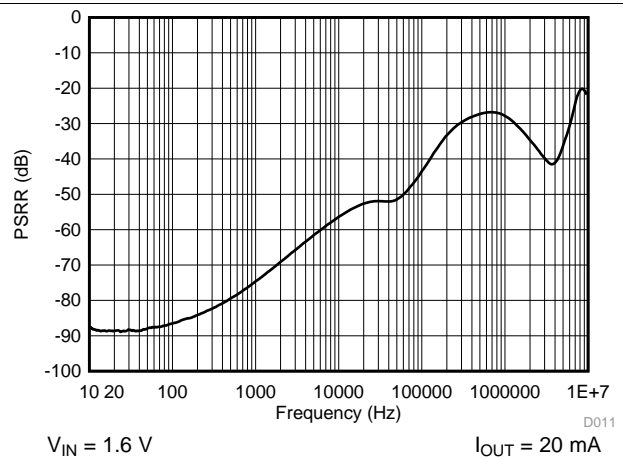


Figure 20. LP5912-0.9 PSRR vs Frequency

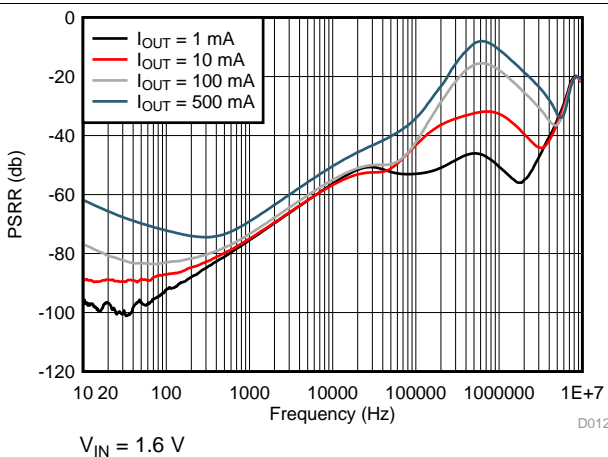


Figure 21. LP5912-0.9 PSRR vs Frequency

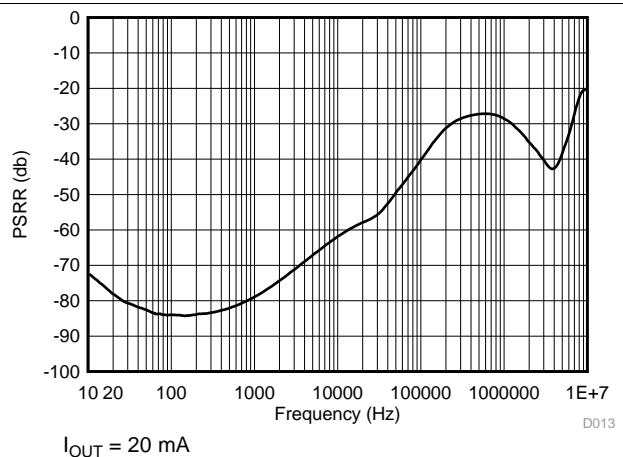


Figure 22. LP5912-1.8 PSRR vs Frequency

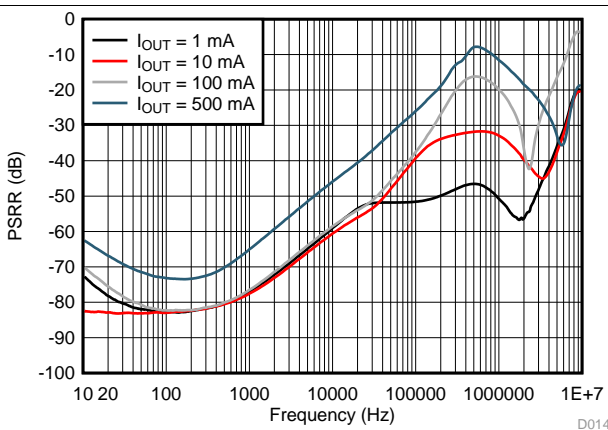


Figure 23. LP5912-1.8 PSRR vs Frequency

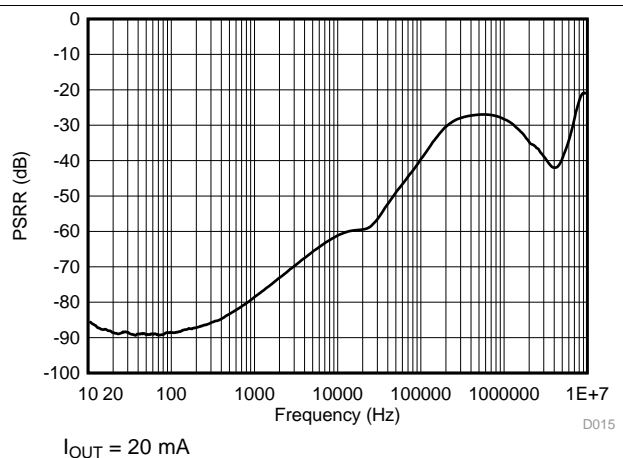


Figure 24. LP5912-3.3 PSRR vs Frequency

Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

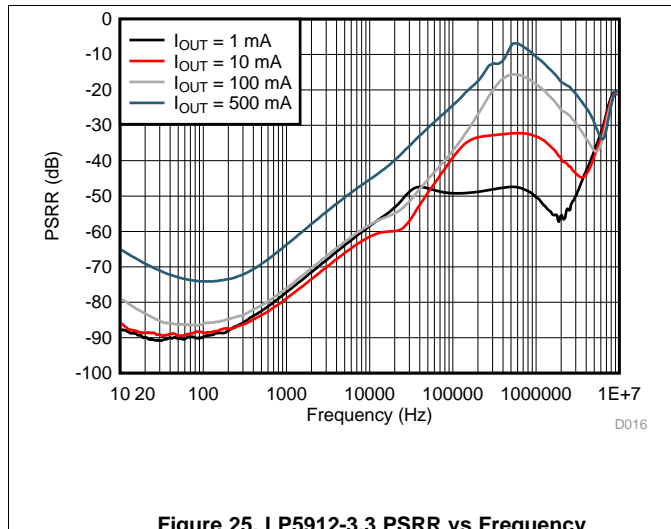


Figure 25. LP5912-3.3 PSRR vs Frequency

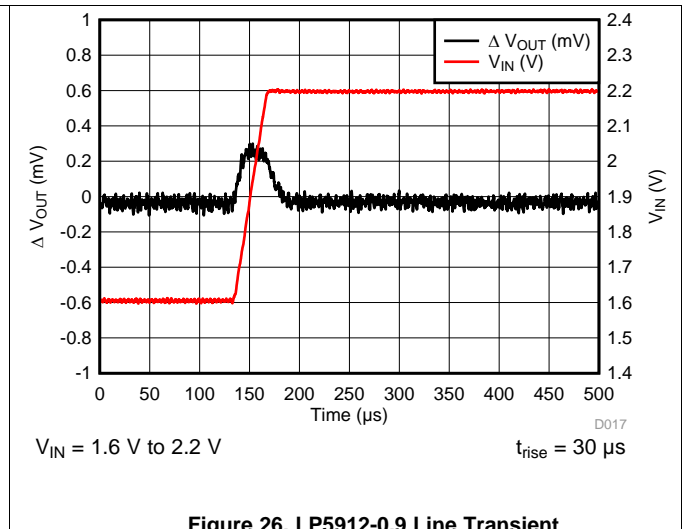


Figure 26. LP5912-0.9 Line Transient

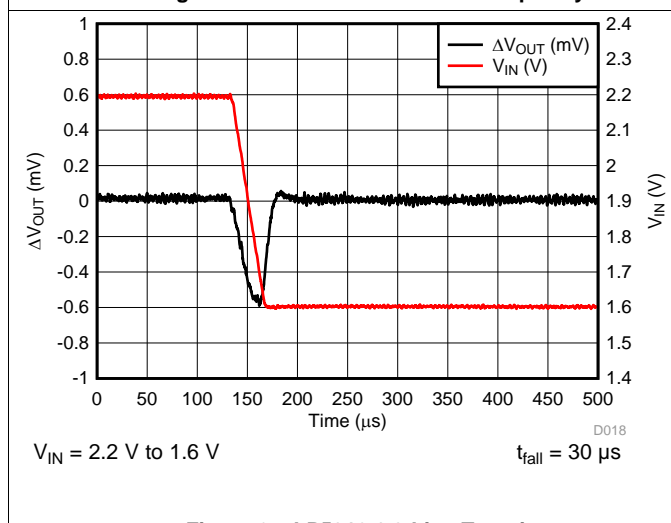


Figure 27. LP5912-0.9 Line Transient

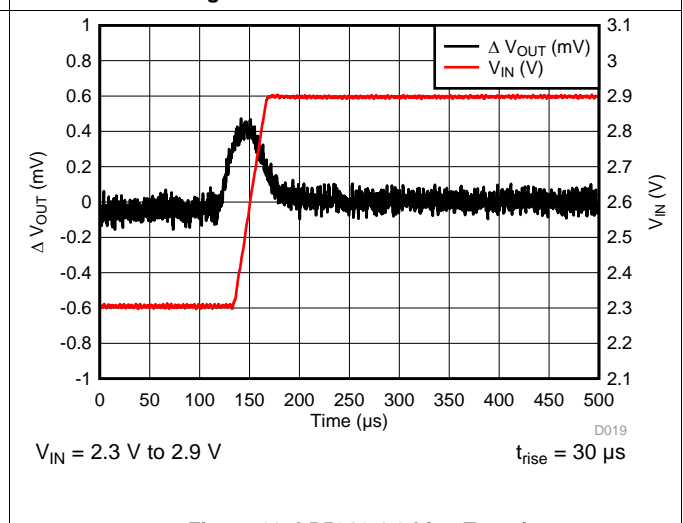


Figure 28. LP5912-1.8 Line Transient

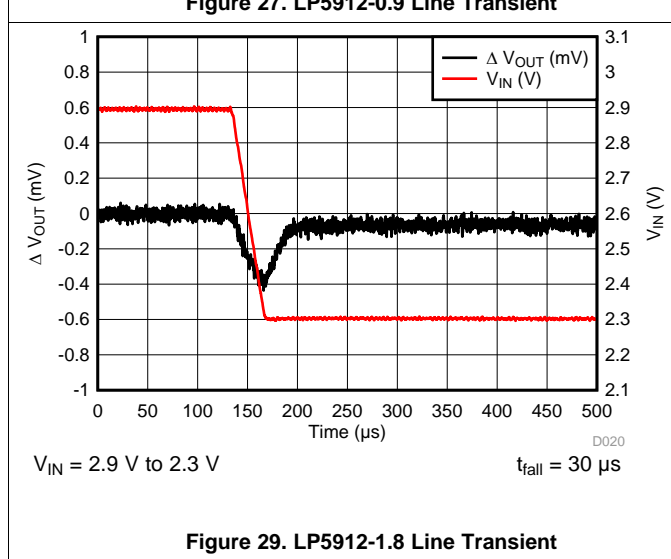


Figure 29. LP5912-1.8 Line Transient

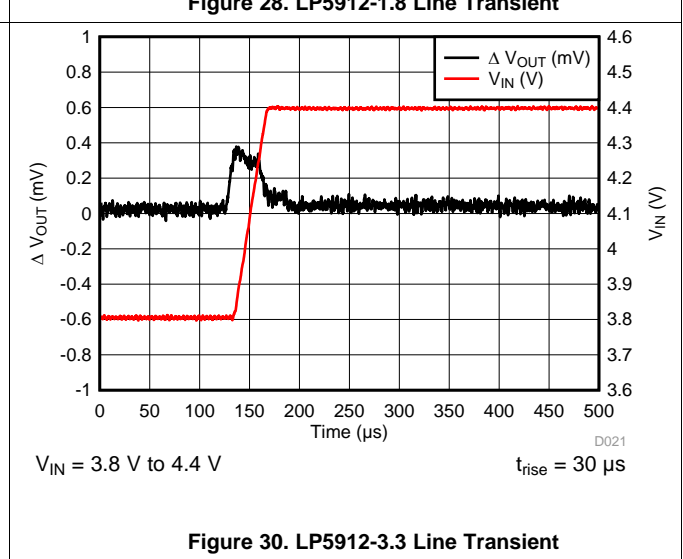


Figure 30. LP5912-3.3 Line Transient

Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

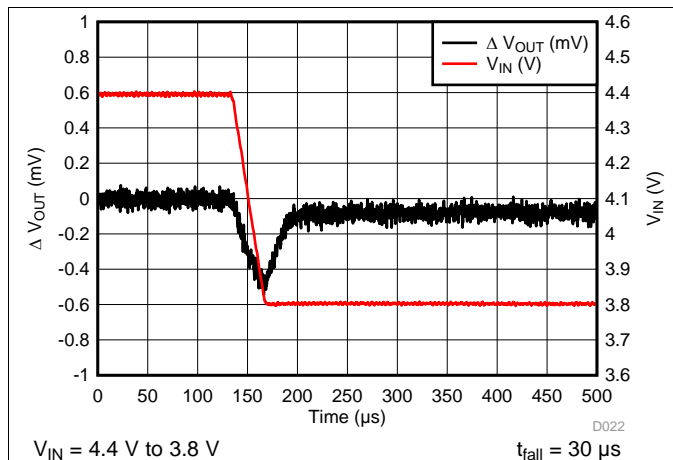


Figure 31. LP5912-3.3 Line Transient

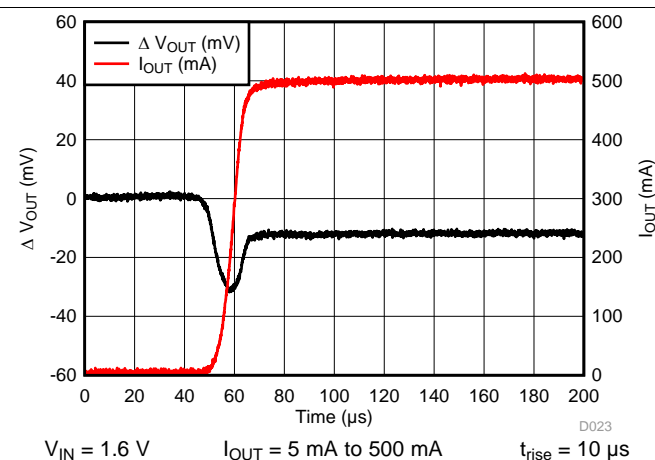


Figure 32. LP5912-0.9 Load Transient Response

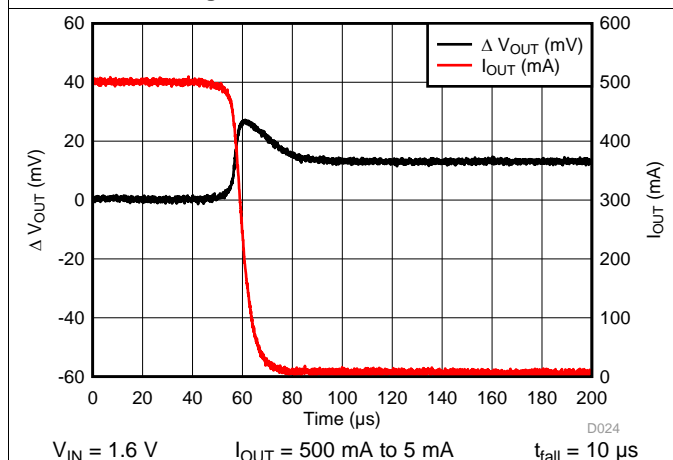


Figure 33. LP5912-0.9 Load Transient Response

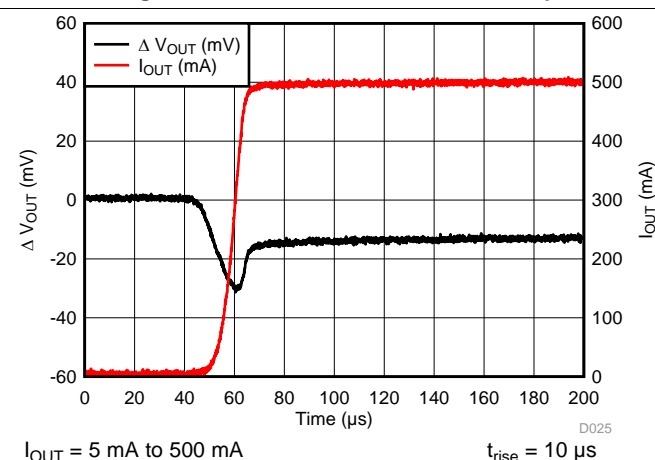


Figure 34. LP5912-1.8 Load Transient Response

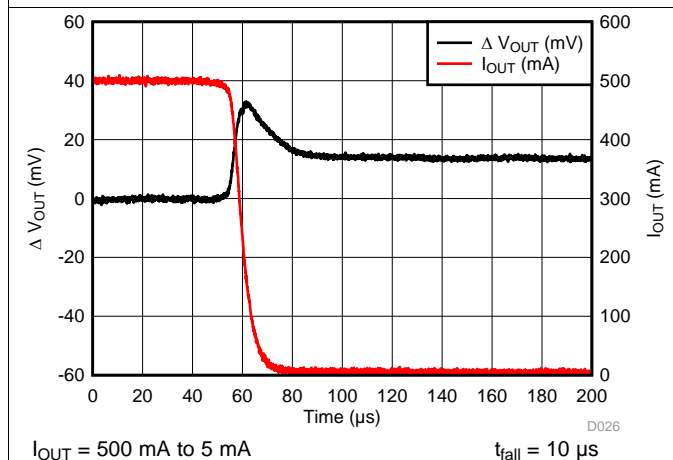


Figure 35. LP5912-1.8 Load Transient Response

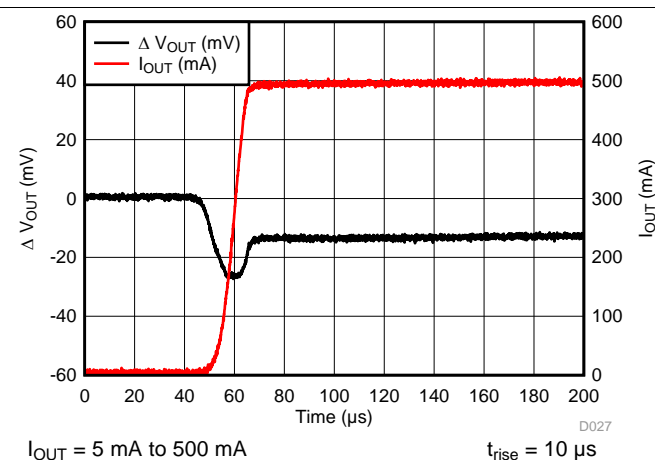


Figure 36. LP5912-3.3 Load Transient Response

Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

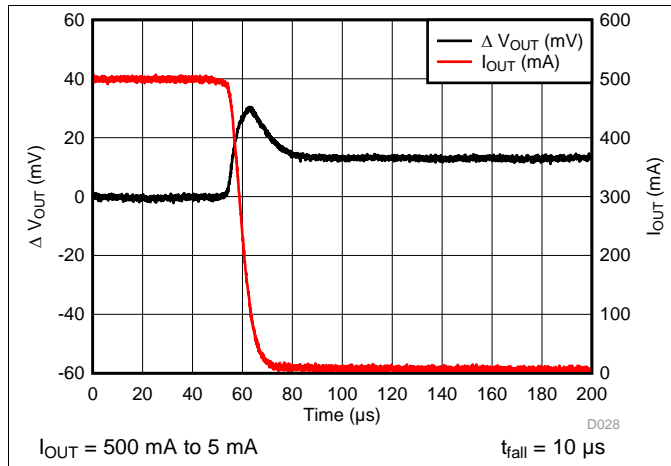


Figure 37. LP5912-3.3 Load Transient Response

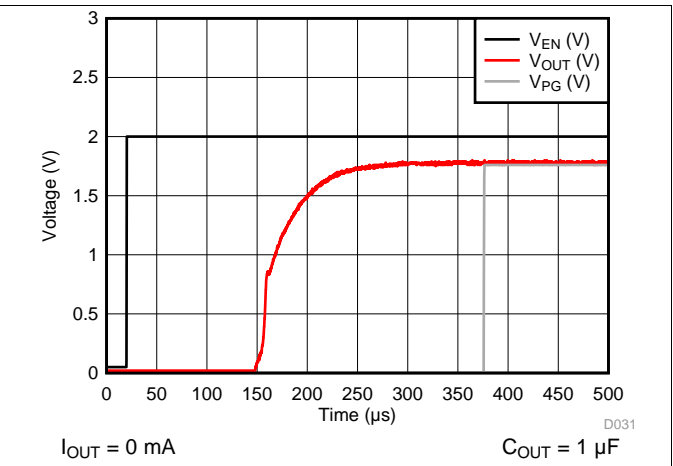


Figure 38. LP5912-1.8  $V_{OUT}$  vs  $V_{EN(ON)}$

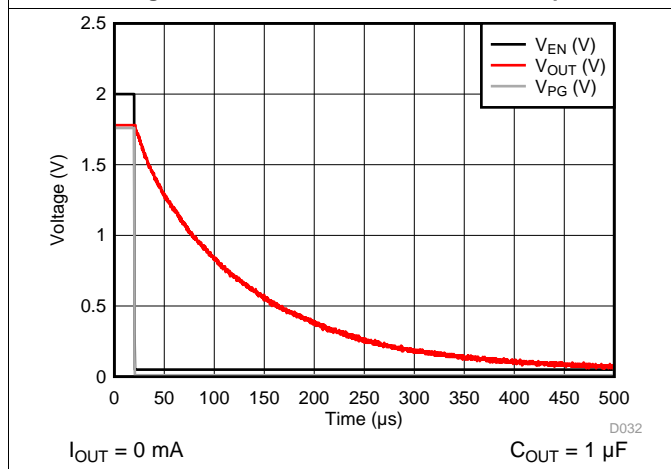


Figure 39. LP5912-1.8  $V_{OUT}$  vs  $V_{EN(OFF)}$

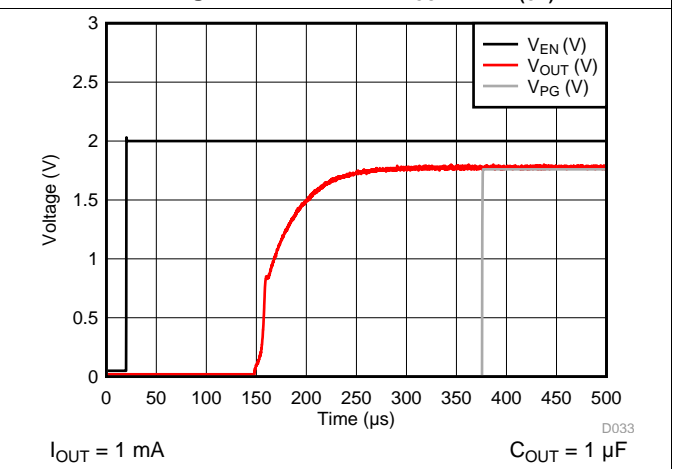


Figure 40. LP5912-1.8  $V_{OUT}$  vs  $V_{EN(ON)}$

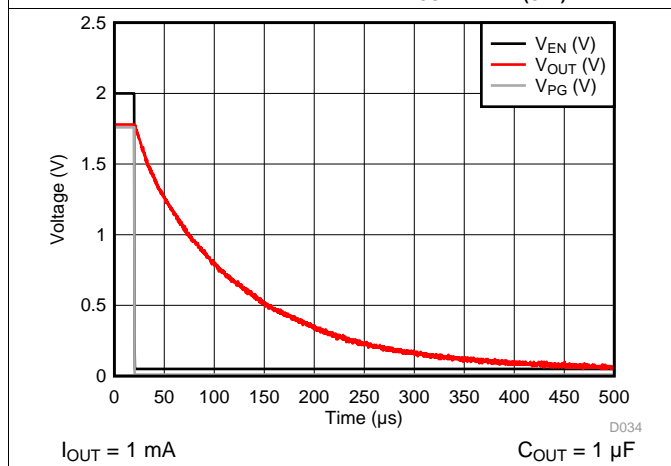


Figure 41. LP5912-1.8  $V_{OUT}$  vs  $V_{EN(OFF)}$

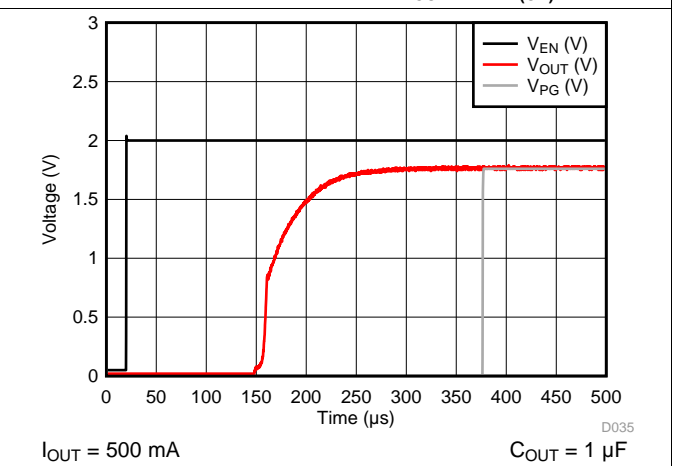


Figure 42. LP5912-1.8  $V_{OUT}$  vs  $V_{EN(ON)}$

Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

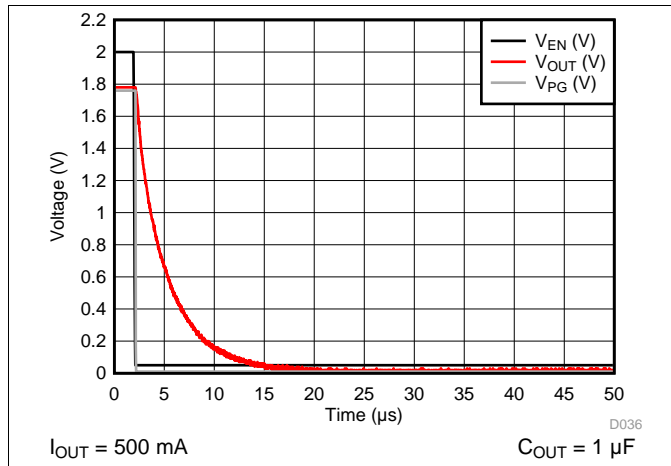


Figure 43. LP5912-1.8  $V_{OUT}$  vs  $V_{EN(OFF)}$

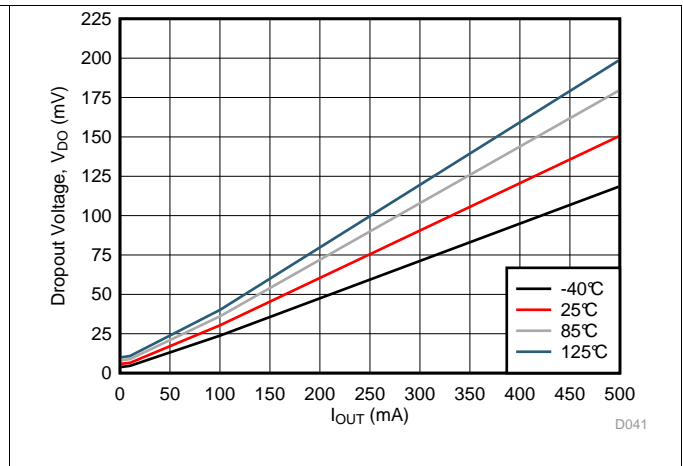


Figure 44. LP5912-1.8 Dropout Voltage ( $V_{DO}$ ) vs  $I_{OUT}$

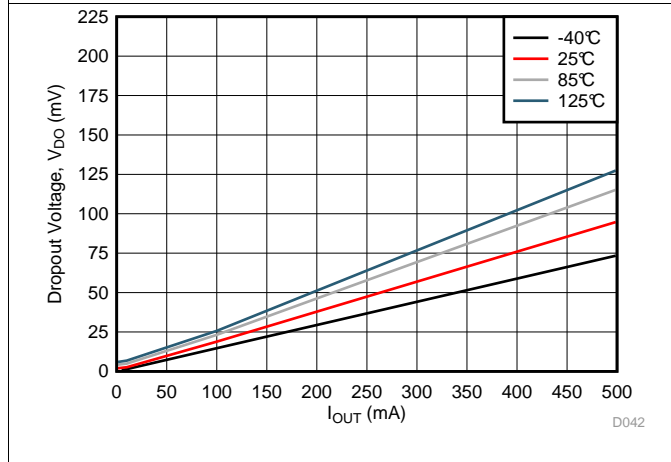


Figure 45. LP5912-3.3 Dropout Voltage ( $V_{DO}$ ) vs  $I_{OUT}$

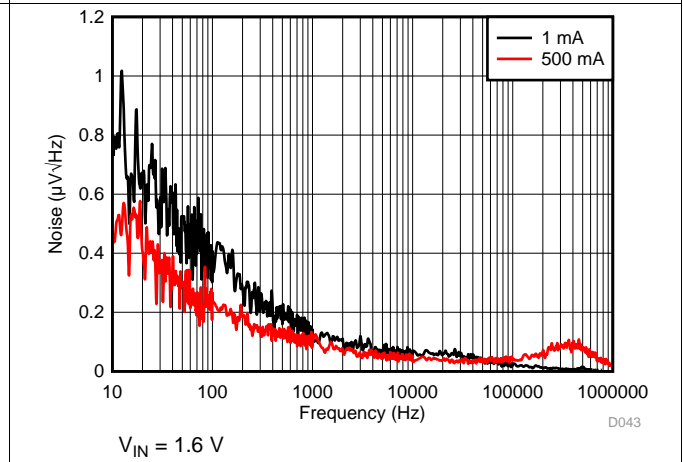


Figure 46. LP5912-0.9 Noise vs Frequency

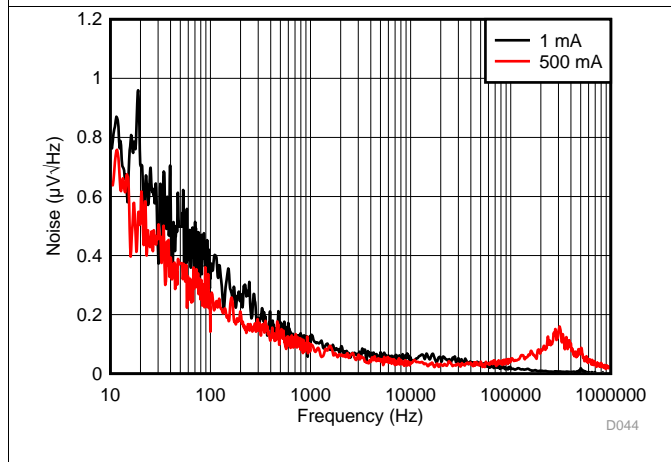


Figure 47. LP5912-1.8 Noise vs Frequency

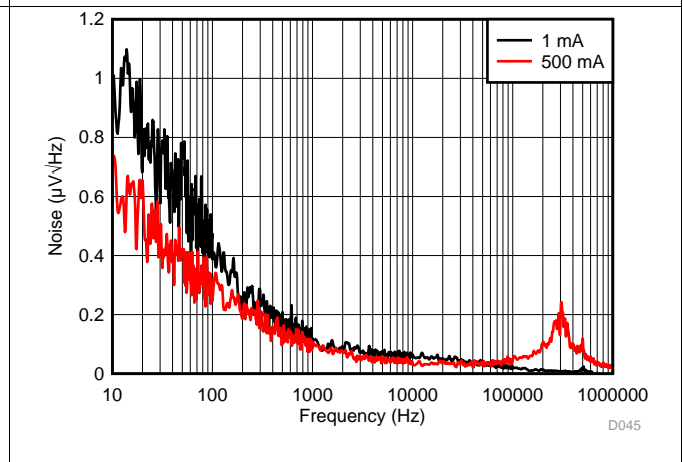


Figure 48. LP5912-3.3 Noise vs Frequency

### Typical Characteristics (continued)

Unless otherwise stated:  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise stated.

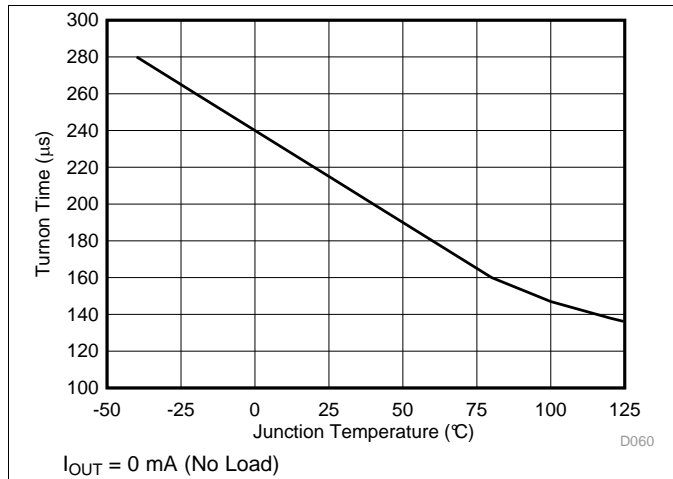


Figure 49. LP5912-3.3 Turnon Time vs Junction Temperature

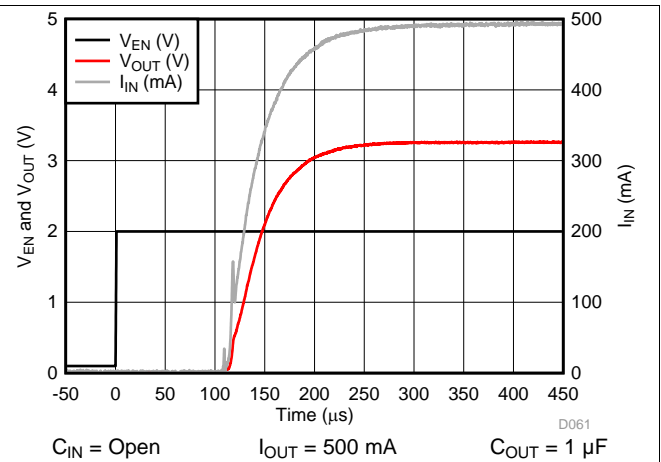


Figure 50. LP5912-3.3 In-Rush Current

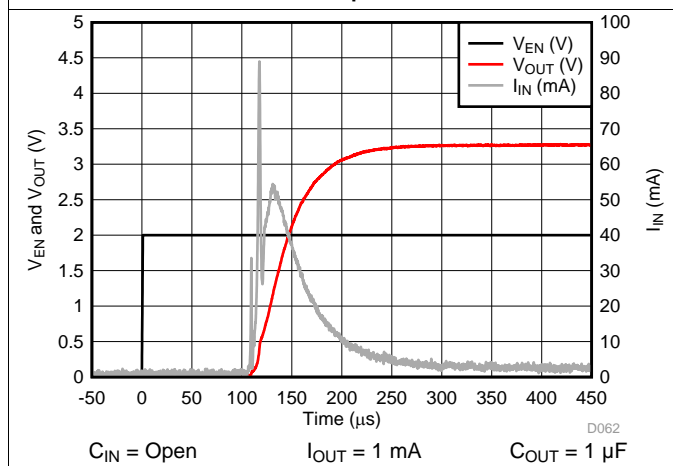


Figure 51. LP5912-3.3 In-Rush Current

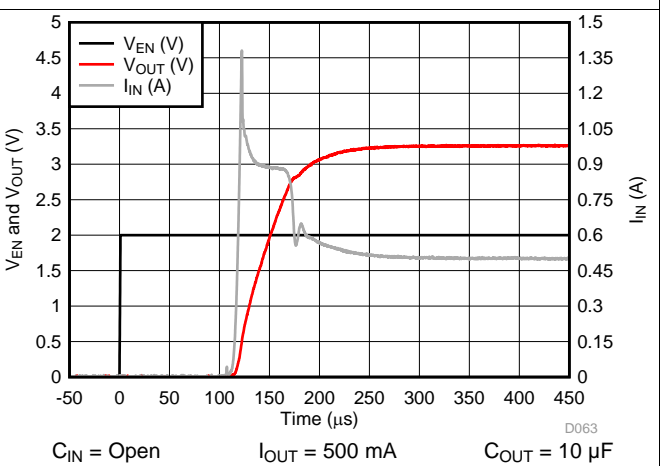


Figure 52. LP5912-3.3 In-Rush Current

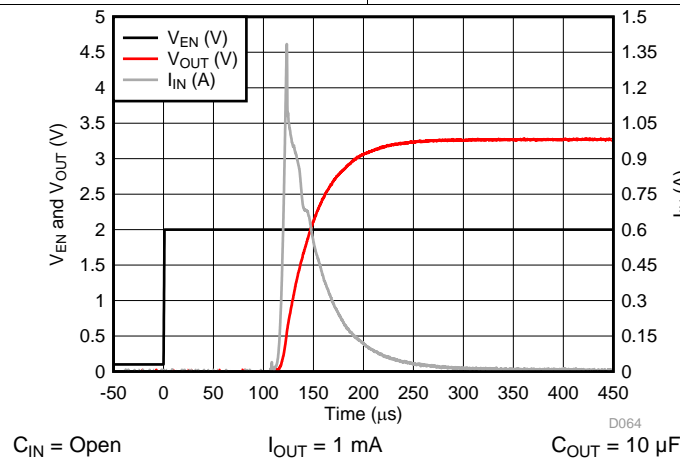


Figure 53. LP5912-3.3 In-Rush Current



## 8 Detailed Description

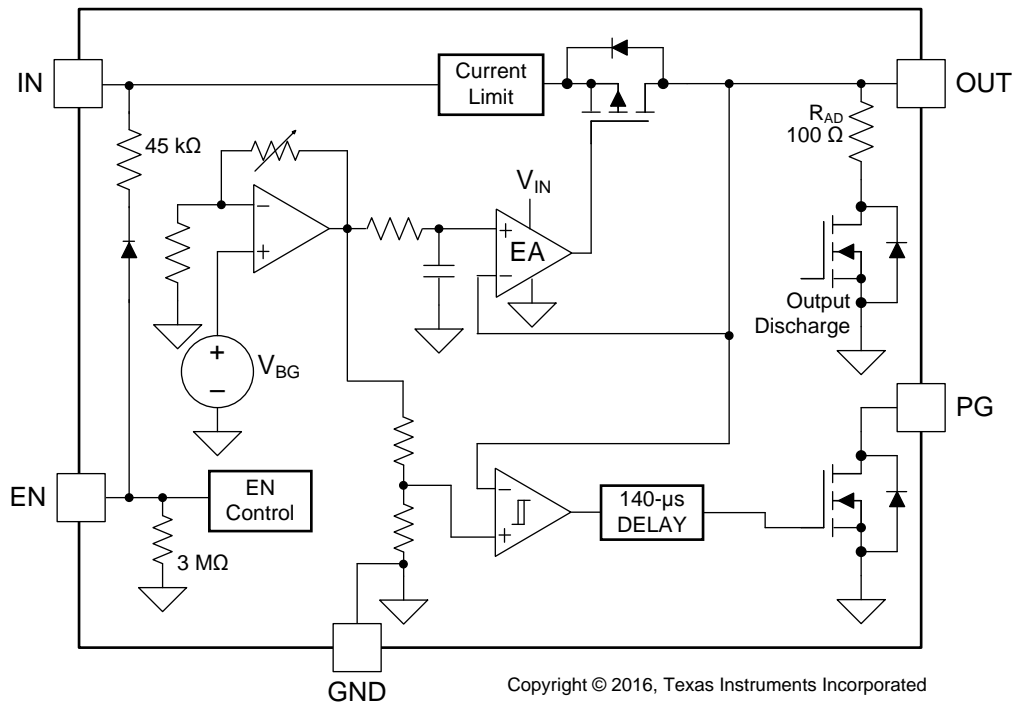
### 8.1 Overview

The LP5912-Q1 is a low-noise, high PSRR, LDO capable of sourcing a 500-mA load. The LP5912-Q1 can operate down to 1.6-V input voltage and 0.8-V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout (LDO) regulator to power a multitude of loads from noise-sensitive communication components to battery-powered system.

The LP5912-Q1 *Functional Block Diagram* contains several features, including:

- Internal output resistor divider feedback;
- Small size and low-noise internal protection circuit current limit;
- Reverse current protection;
- Current limit and in-rush current protection;
- Thermal shutdown;
- Output auto discharge for fast turnoff; and
- Power-good output, with fixed 140- $\mu$ s typical delay.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Enable (EN)

The LP5912-Q1 EN pin is internally held low by a 3-M $\Omega$  resistor to GND. The EN pin voltage must be higher than the  $V_{EN(ON)}$  threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the  $V_{EN(OFF)}$  threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

When the device is disabled the output stage is disabled, the PG output pin is low, and the output automatic discharge is ON.

## Feature Description (continued)

### 8.3.2 Output Automatic Discharge ( $R_{AD}$ )

The LP5912-Q1 output employs an internal 100- $\Omega$  (typical) pulldown resistance to discharge the output when the EN pin is low. Note that if the LP5912-Q1 EN pin is low (the device is OFF) and the OUT pin is held high by a secondary supply, current flows from the secondary supply through the automatic discharge pulldown resistor to ground.

### 8.3.3 Reverse Current Protection ( $I_{RO}$ )

The LP5912-Q1 input is protected against reverse current when output voltage is higher than the input. In the event that extra output capacitance is used at the output, a power-down transient at the input would normally cause a large reverse current through a conventional regulator. The LP5912-Q1 includes a reverse voltage detector that trips when  $V_{IN}$  drops below  $V_{OUT}$ , shutting off the regulator and opening the PMOS body diode connection, preventing any reverse current from the OUT pin from flowing to the IN pin.

If the LP5912 EN pin is low (the LP5912 is OFF) and the OUT pin is held high by a secondary supply, current flows from the secondary supply through the automatic discharge pulldown resistor to ground. This is not reverse current, this is automatic discharge pulldown current.

Note that reverse current ( $I_{RO}$ ) is measured at the IN pin.

### 8.3.4 Internal Current Limit ( $I_{SC}$ )

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate continuously at the  $I_{SC}$  current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

### 8.3.5 Thermal Overload Protection ( $T_{SD}$ )

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

### 8.3.6 Power-Good Output (PG)

The LP5912-Q1 device has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage ( $PG_{LTH}$ ), the PG pin open-drain output engages (low impedance to GND). When the output voltage rises above the PG threshold voltage ( $PGV_{HTH}$ ), the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Use a pullup resistor from 10 k $\Omega$  to 100 k $\Omega$  for best results.

The input supply,  $V_{IN}$ , must be no less than the minimum operating voltage of 1.6 V to ensure that the PG pin output status is valid. The PG pin output status is undefined when  $V_{IN}$  is less than 1.6 V.

In power-good function, the PG output pin being pulled high is typically delayed 140  $\mu$ s after the output voltage rises above the  $PG_{HTH}$  threshold voltage. If the output voltage rises above the  $PG_{HTH}$  threshold and then falls below the  $PG_{LTH}$  threshold voltage the PG pin falls immediately with no delay time.

If the PG function is not needed, the pullup resistor can be eliminated, and the PG pin can be either connected to ground or left floating.

## 8.4 Device Functional Modes

### 8.4.1 Enable (EN)

The LP5912-Q1 EN pin is internally held low by a 3-M $\Omega$  resistor to GND. The EN pin voltage must be higher than the  $V_{EN(ON)}$  threshold to ensure that the device is fully enabled under all operating conditions. When the EN pin voltage is lower than the  $V_{EN(OFF)}$  threshold, the output stage is disabled, the PG pin goes low, and the output automatic discharge circuit is activated. Any charge on the OUT pin is discharged to ground through the internal 100- $\Omega$  (typical) output auto discharge pulldown resistance.

### 8.4.2 Minimum Operating Input Voltage ( $V_{IN}$ )

The LP5912-Q1 device does not include any dedicated UVLO circuit. The device internal circuit is not fully functional until  $V_{IN}$  is at least 1.6 V. The output voltage is not regulated until  $V_{IN}$  has reached at least the greater of 1.6 V or ( $V_{OUT} + V_{DO}$ ).

## 9 Applications and Implementation

### NOTE

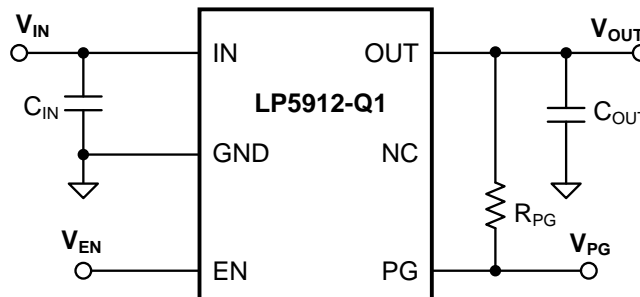
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP5912-Q1 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1  $\mu\text{F}$ . The device delivers this performance in an industry standard WSON package, which for this device is specified with an operating junction temperature ( $T_J$ ) of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### 9.2 Typical Application

Figure 54 shows the typical application circuit for the LP5912-Q1. Input and output capacitances may need to be increased above the 1- $\mu\text{F}$  minimum for some applications.



Copyright © 2016, Texas Instruments Incorporated

**Figure 54. LP5912-Q1 Typical Application**

#### 9.2.1 Design Requirements

For typical RF linear regulator applications, use the parameters listed in [Table 1](#).

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	1.6 to 6.5 V
Output voltage	0.8 to 5.5 V
Output current	500 mA
Output capacitor	1 to 10 $\mu\text{F}$
Input/output capacitor ESR range	5 m $\Omega$ to 500 m $\Omega$

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 External Capacitors

Like most low-dropout regulators, the LP5912-Q1 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

### 9.2.2.2 Input Capacitor

An input capacitor is required for stability. The input capacitor must be at least equal to, or greater than, the output capacitor for good load-transient performance. A capacitor of at least 1  $\mu\text{F}$  must be connected between the LP5912-Q1 IN pin and ground for stable operation over full load-current range. It is acceptable to have more output capacitance than input, as long as the input is at least 1  $\mu\text{F}$ .

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

#### NOTE

To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5912-Q1, increasing the value of the input capacitor to at least 10  $\mu\text{F}$  is recommended. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains 1  $\mu\text{F} \pm 30\%$  over the entire operating temperature range.

### 9.2.2.3 Output Capacitor

The LP5912-Q1 is designed specifically to work with a very small ceramic output capacitor, typically 1  $\mu\text{F}$ . A ceramic capacitor (dielectric types X5R or X7R) in the 1- $\mu\text{F}$  to 10- $\mu\text{F}$  range, and with an ESR from 5 m $\Omega$  to 500 m $\Omega$ , is suitable in the LP5912-Q1 application circuit. For this device the output capacitor must be connected between the OUT pin with a good connection back to the GND pin.

Tantalum or film capacitors may also be used at the device output,  $V_{\text{OUT}}$ , but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 m $\Omega$  to 500 m $\Omega$  for stability.

### 9.2.2.4 Capacitor Characteristics

The LP5912-Q1 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1  $\mu\text{F}$  to 10  $\mu\text{F}$ , ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1- $\mu\text{F}$  ceramic capacitor is in the range of 20 m $\Omega$  to 40 m $\Omega$ , which easily meets the ESR requirement for stability for the LP5912-Q1.

The preferred choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within  $\pm 15\%$  over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1- $\mu\text{F}$  to 10- $\mu\text{F}$  range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. While it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

### 9.2.2.5 Remote Capacitor Operation

To ensure stability the LP5912-Q1 requires at least a 1- $\mu$ F capacitor at the OUT pin. There is no strict requirement about the location of the output capacitor in regards to the LDO OUT pin; the output capacitor may be located 5 to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the OUT pin if there are already respective capacitors in the system. This placement flexibility requires that the output capacitor be connected directly between the LP5912-Q1 OUT pin and GND pin with no vias. This remote capacitor feature can help users to minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum, which means using as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close to ground layer as possible, avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. Keeping parasitic wiring inductance less than 35 nH is recommended. For applications with fast load transients use an input capacitor equal to, or larger than, the sum of the capacitance at the output node for the best load-transient performance.

### 9.2.2.6 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with [Equation 1](#).

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that is greater than the dropout voltage ( $V_{DO}$ ). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad into the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ), according to [Equation 2](#) or [Equation 3](#):

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this  $R_{\theta JA}$  is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The  $R_{\theta JA}$  recorded in [Thermal Information](#) is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout,  $R_{\theta JA}$  is actually the sum of the package junction-to-case (bottom) thermal resistance ( $R_{\theta JCBOT}$ ) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

### 9.2.2.7 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi ( $\Psi$ ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) are given in [Thermal Information](#) and are used in accordance with [Equation 4](#) or [Equation 5](#).

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$  is explained in [Equation 3](#)
- $T_{TOP}$  is the temperature measured at the center-top of the device package. (4)

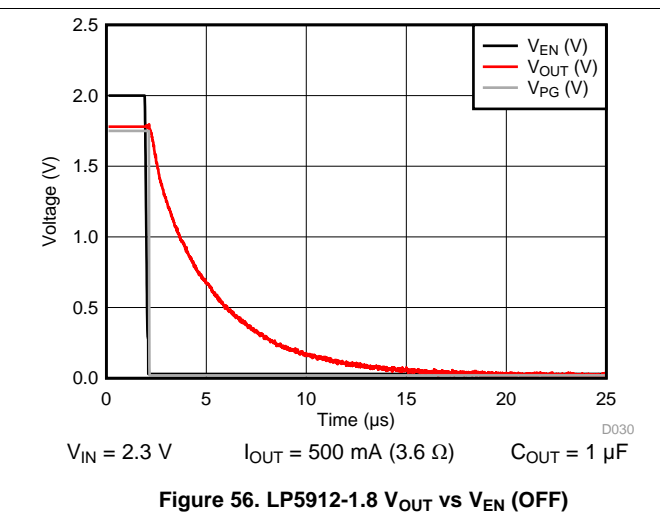
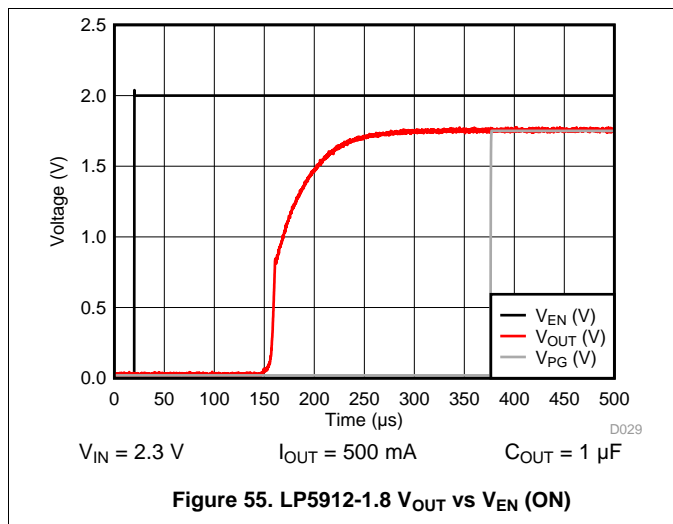
$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$  is explained in [Equation 3](#).
- $T_{BOARD}$  is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics  $\Psi_{JT}$  and  $\Psi_{JB}$ , see [Semiconductor and IC Package Thermal Metrics](#); for more information about measuring  $T_{TOP}$  and  $T_{BOARD}$ , see [Using New Thermal Metrics](#); and for more information about the EIA/JEDEC JESD51 PCB used for validating  $R_{\theta JA}$ , see the TI Application Report [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#). These application notes are available at [www.ti.com](http://www.ti.com).

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5912-Q1 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least  $V_{OUT} + 0.5$  V. A minimum capacitor value of 1  $\mu$ F is required to be within 1 cm of the IN pin.

## 11 Layout

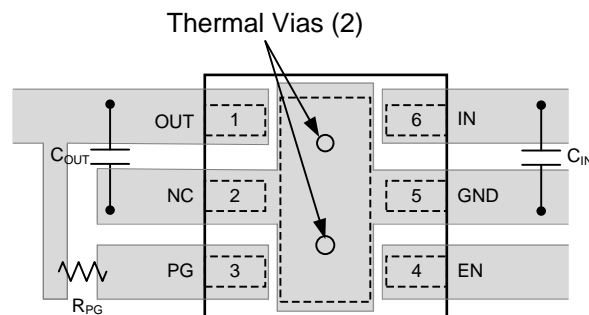
### 11.1 Layout Guidelines

The dynamic performance of the LP5912-Q1 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5912-Q1.

Best performance is achieved by placing  $C_{IN}$  and  $C_{OUT}$  on the same side of the PCB as the LP5912-Q1, and as close to the package as is practical. The ground connections for  $C_{IN}$  and  $C_{OUT}$  must be back to the LP5912-Q1 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. Such connections add parasitic inductances and resistance that result in inferior performance especially during transient conditions.

### 11.2 Layout Example



**Figure 57. LP5912-Q1 Typical Layout**



## 12 器件和文档支持

### 12.1 相关文档

更多信息，请参见以下文档：

- 《AN1187 无引线框架封装 (LLP)》
- 半导体和集成电路 (IC) 封装热度量
- 《使用新的热指标》
- 《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》

### 12.2 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](http://www.ti.com.cn) 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5912Q0.9DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QA	<a href="#">Samples</a>
LP5912Q0.9DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QA	<a href="#">Samples</a>
LP5912Q1.1DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QH	<a href="#">Samples</a>
LP5912Q1.1DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QH	<a href="#">Samples</a>
LP5912Q1.2DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QB	<a href="#">Samples</a>
LP5912Q1.2DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QB	<a href="#">Samples</a>
LP5912Q1.5DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QC	<a href="#">Samples</a>
LP5912Q1.5DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QC	<a href="#">Samples</a>
LP5912Q1.8DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QD	<a href="#">Samples</a>
LP5912Q1.8DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QD	<a href="#">Samples</a>
LP5912Q2.8DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QE	<a href="#">Samples</a>
LP5912Q2.8DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QE	<a href="#">Samples</a>
LP5912Q3.0DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QG	<a href="#">Samples</a>
LP5912Q3.0DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QG	<a href="#">Samples</a>
LP5912Q3.3DRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QF	<a href="#">Samples</a>
LP5912Q3.3DRVTQ1	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QF	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

---

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5912Q0.9DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q0.9DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.1DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.1DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.2DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.2DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.5DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.5DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.8DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.8DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q2.8DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q2.8DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.0DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.0DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.3DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.3DRVTQ1	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

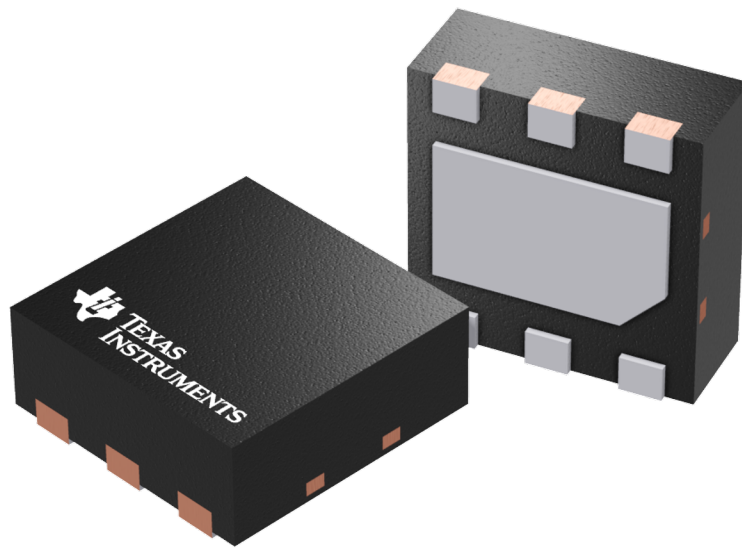
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5912Q0.9DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q0.9DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q1.1DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.1DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q1.2DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.2DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q1.5DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.5DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q1.8DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.8DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q2.8DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q2.8DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q3.0DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q3.0DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0
LP5912Q3.3DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q3.3DRVTQ1	WSON	DRV	6	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

DRV 6

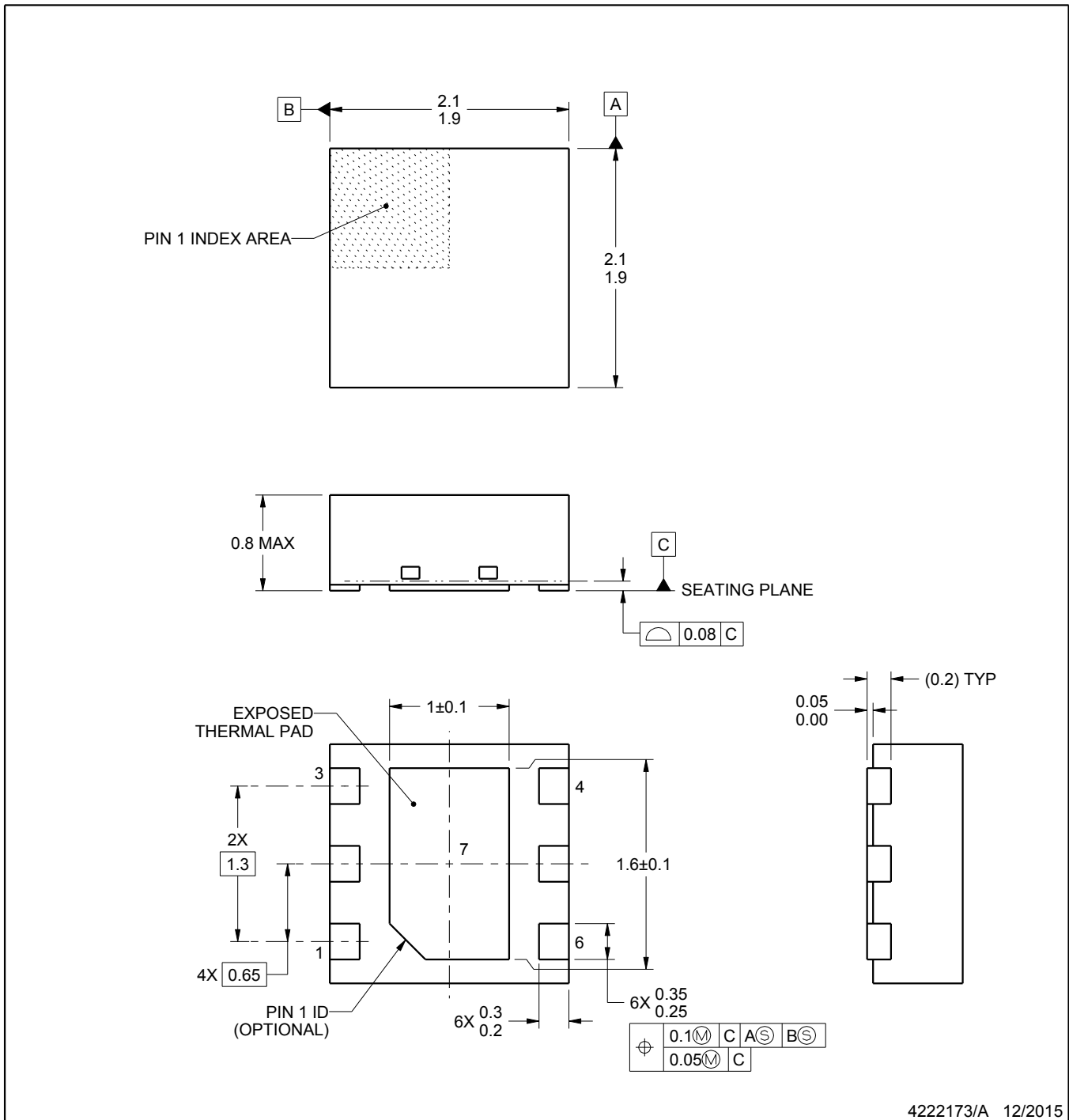
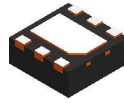
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



4222173/A 12/2015

NOTES:

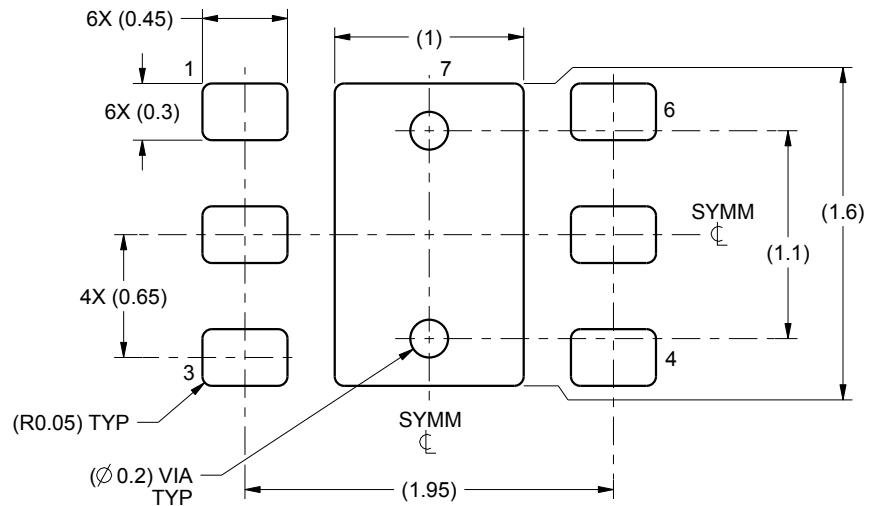
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

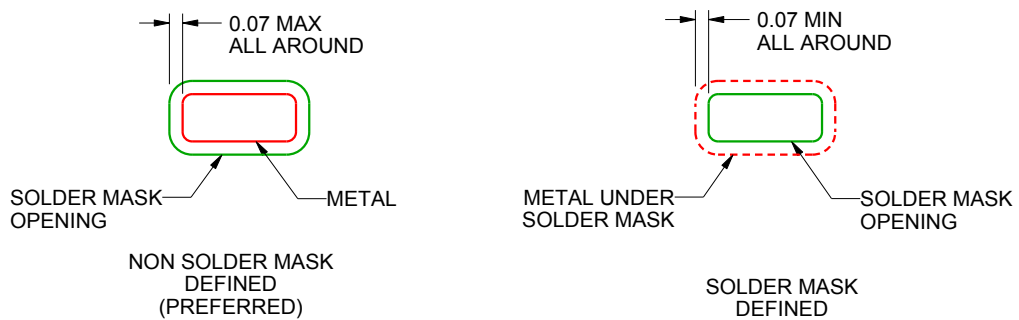
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

4222173/A 12/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

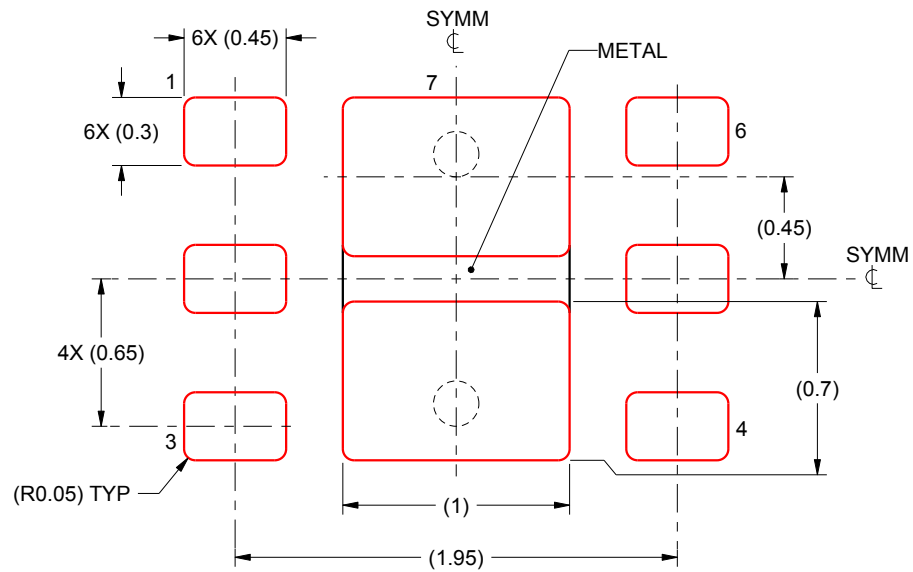


# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4222173/A 12/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和和该等应用所用 TI 产品的功能而设计。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与应用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准而设计。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2018 德州仪器半导体技术（上海）有限公司