bq294502, bq294504, bq294506
bq294512, bq294522, bq294524
bq294532, bq294533, bq294582, bq294592
ZHCS477H – SEPTEMBER 2011 – REVISED DECEMBER 2017

bq2945xx 适用于 2 节和 3 节锂离子电池的过压保护

1 特性

- 用于 2 节和 3 节电池二级保护的过压监控器
- 固定的可编程延迟计时器
- 固定的 OVP 阈值
  - 可用范围为 3.85V 至 4.6V
- 固定的 OVP 延迟选项：4 秒或 6.5 秒
- 高精度过压保护：
  ±10 mV
- 低功耗 I_{CC} ≈ 1 µA
  ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- 每节电池输入的泄漏电流低于 100nA
- 小封装尺寸
  - 6 引脚 SON

2 应用

- 用于下列产品的锂离子电池组中的二级保护：
  - 平板电脑
  - 手写板电脑
  - 电动工具
  - 笔记本电脑
  - 便携式设备和仪器

3 说明

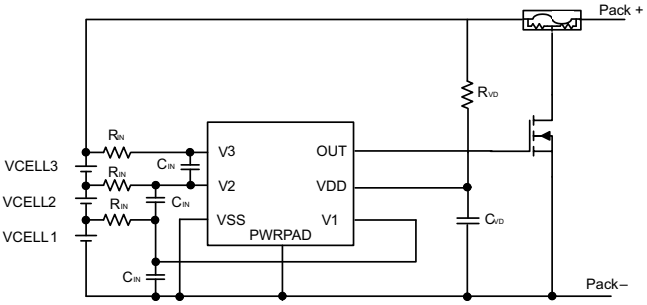
bq2945xx 系列产品是用于锂离子电池组系统的二级电压监控器和保护器。独立监控每节电池是否具有过压状态。根据配置，如果两节或三节电池中的任何电池存在过压，则在经过固定的延迟后会触发一个输出。在过压状态满足指定的延迟计时器条件后，该输出触发为高电平状态。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq2945xx	SON (6)	2.00mm × 2.00mm

(1) 要了解所有可用封装，请参见产品说明书末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (November 2017) to Revision H — **Page**

- Added the bq294506 device to the *Device Comparison Table* ... 4
- Added the bq294506 device to the *Electrical Characteristics* ... 6

Changes from Revision F (June 2017) to Revision G — **Page**

- Changed the *Device Comparison Table* ... 4
- Changed the *Electrical Characteristics* ... 6

Changes from Revision E (December 2016) to Revision F — **Page**

- Added bq294533 to the *Device Comparison Table* table ... 4
- Added the bq294592 device to Production Data ... 4
- Added the bq294533 VOV *Electrical Characteristics* ... 6

Changes from Revision D (July 2015) to Revision E — **Page**

- Changed RIN range values in *Design Requirements* section from: MIN: 900, MAX: 1100 to: MIN: 100, MAX: 4700 ... 11
- Changed CIN range values *Design Requirements* section from: MIN: 0.01, MAX: 0.1 to: MIN: 0.1, MAX: 1 ... 11
- 已添加 *接收文档更新通知*部分 ... 14

Changes from Revision C (May 2012) to Revision D — **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性 说明*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已添加 向说明部分添加了 过压 ... 1
- 已更改 更改了项目符号以整合特性项 ... 1

- 已添加 将固定的 OVP 延迟选项添加至 特性 1
- Changed *Absolute Maximum Ratings* 5
- Changed format of graphs 7

Changes from Revision B (February 2012) to Revision C **Page**

- Added the bq294524 device to Production Data 4
- Added the bq294532 device to Production Data 4
- Changed Overvoltage Detection Hysteresis 6
- Added Output Voltage Versus Output Current graphic 7
- Changed Timing for Customer Test Mode figure 10

Changes from Revision A (November 2011) to Revision B **Page**

- 已更改 将 bq294504 器件更改为产品数据 1
- 已添加 添加了 bq294512 器件 1
- 已添加 添加了 bq294592 器件 1
- Added a second I_{CC} Test Condition 6
- Changed Fault Detection Delay Time in bq2945x4 Test Mode Specifications 6

Changes from Original (September 2011) to Revision A **Page**

- Added the bq294582 device to Production Data 4

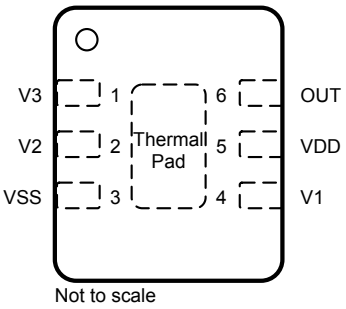
5 Device Comparison Table

T_A	PART NUMBER	OVP (V)	DELAY TIME (s)
–40°C to +110°C	bq294502	4.35	4
	bq294504	4.35	6.5
	bq294506(1)	4.38	4
	bq294512	4.4	4
	bq294522	4.45	4
	bq294524	4.45	6.5
	bq294532	4.5	4
	bq294533	4.5	6.5
	bq294582	4.225	4
	bq294592	4.3	4

(1) Advance Information. Contact TI for more information.

6 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



Not to scale

Pin Functions

NUMBER	NAME	I/O	DESCRIPTION
1	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack.
2	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack.
3	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack.
4	V1	IA	Sense input for positive voltage of the lowest cell in the stack.
5	VDD	P	Power supply
6	OUT	OA(1)	Output drive for external N-channel FET.
—	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed-circuit-board (PCB) for proper operation.

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	VDD–VSS	–0.3	30	V
Input voltage	V1–VSS or V2–VSS or V3–VSS+	–0.3	30	V
	V3–V2 or V2–V1	–0.3	8	V
Output voltage	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See *Thermal Information*		
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See Figure 8.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}(1)		3	25	V
Input voltage	V3–V2 or V2–V1 or V1–VSS	0	5	V
Operating ambient temperature, T_A		–40	110	°C

(1) See *Typical Application*.

7.4 Thermal Information

THERMAL METRIC(1)		bq2945xx DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	90.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	110.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	96.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 10.8 V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLD VCx						
V_{OV}	$V_{(PROTECT)}$ – Overvoltage Detection	bq294502, fixed delay 4 s		4.35		V
		bq294504, fixed delay 6.5 s		4.35		
		bq294506, fixed delay 4 s(1)		4.38		
		bq294512, fixed delay 4 s		4.4		
		bq294522, fixed delay 4 s		4.45		
		bq294524, fixed delay 6.5 s		4.45		
		bq294532, fixed delay 4 s		4.5		
		bq294533, fixed delay 6.5 s		4.5		
		bq294582, fixed delay 4 s		4.225		
		bq294592, fixed delay 4 s		4.3		
V_{HYS}	Overvoltage Detection Hysteresis	V_{HYS}	250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C, bq2945xx	–10		10	mV
		T_A = 25°C, bq294506 only(1)	–7		7	mV
$V_{OA\ –DRIFT}$	OV Detection Accuracy due to Temperature	T_A = –40°C T_A = 0°C T_A = 60°C T_A = 110°C	–40 –20 –24 –54		44 20 24 54	mV
		T_A = 10°C to 45°C, bq294506 only(1)	–15		15	mV
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	Supply Current	(V3–V2) = (V2–V1) = (V1–VSS) = 4 V (See Figure 8 for reference.)		1	2	µA
		(V3–V2) = (V2–V1) = (V1–VSS) = 2.8 V with T_A = –40°C to 60°C			1.25	
I_{IN}	Input Current at Vx Pins	Measured at V3, V2, and V1 = 4 V (V2–V1) = (V1–VSS) = 4 V T_A = 0°C to 60°C (See Figure 8 for reference.)	–0.1		0.1	µA
OUTPUT DRIVE OUT						
V_{OUT}	Output Drive Voltage	(V3–V2) or (V2–V1) or (V1–VSS) > V_{OV} V_{DD} = 7.2 V, I_{OH} = 100 µA, T_A = –40°C to +110°C	6			V
		Two of the three cells are short circuit and only one cell is powered (V3–V2) or (V2–V1) or (V1–VSS) > V_{OV} V_{DD} = Vx (Cell voltage), I_{OH} = 100 µA, T_A = –40°C to +110°C		VDD – 0.2		V
		(V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, I_{OL} = 100 µA, T_A = 25°C T_A = –40°C to +110°C		250	400	mV
$I_{OUT(Short)}$	OUT Short Circuit Current	OUT = 0 V (V3–V2) or (V2–V1) or (V1–VSS) > V_{OV}			4.5	mA
t_R	Output Rise Time	CL = 1 nF, $V_{OH(OUT)}$ = 0 V to 5 V(2)		5		µs
Z_O	Output Impedance			2	5	kΩ
FIXED DELAY TIMER						
t_{DELAY}	Fault Detection Delay Time	Fixed Delay, bq2945xx with delay set to 4s typ	3.2	4	4.8	s
		Fixed Delay, bq2945xx with delay set to 6.5s	5.2	6.5	7.8	
t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode	Fixed Delay (Internal settings)		15		ms

(1) Advance Information. Contact TI for more information.
(2) Specified by design. Not 100% tested in production.

7.6 Typical Characteristics

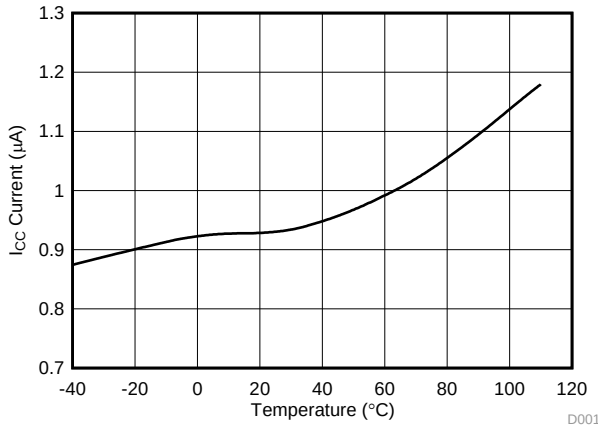


Figure 1. I_{CC} Current Consumption vs Temperature

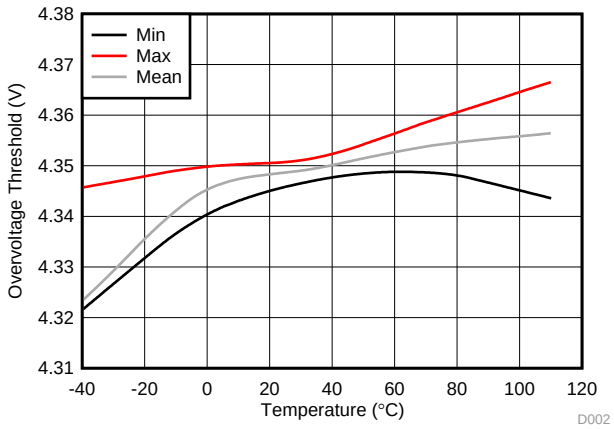


Figure 2. bq294502 Overvoltage Threshold (OVT) vs Temperature

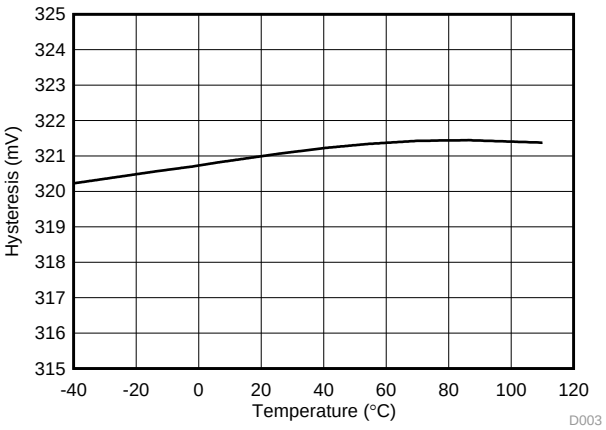


Figure 3. Hysteresis V_{HYS} vs Temperature

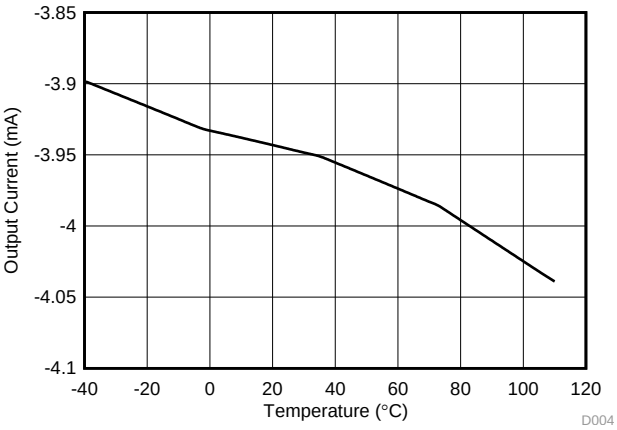


Figure 4. Output Current I_{OUT} vs Temperature

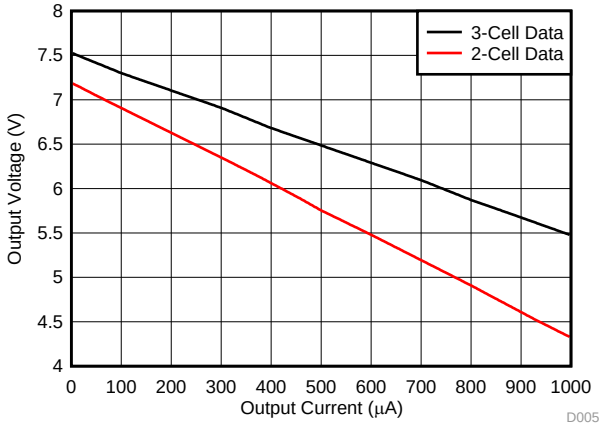


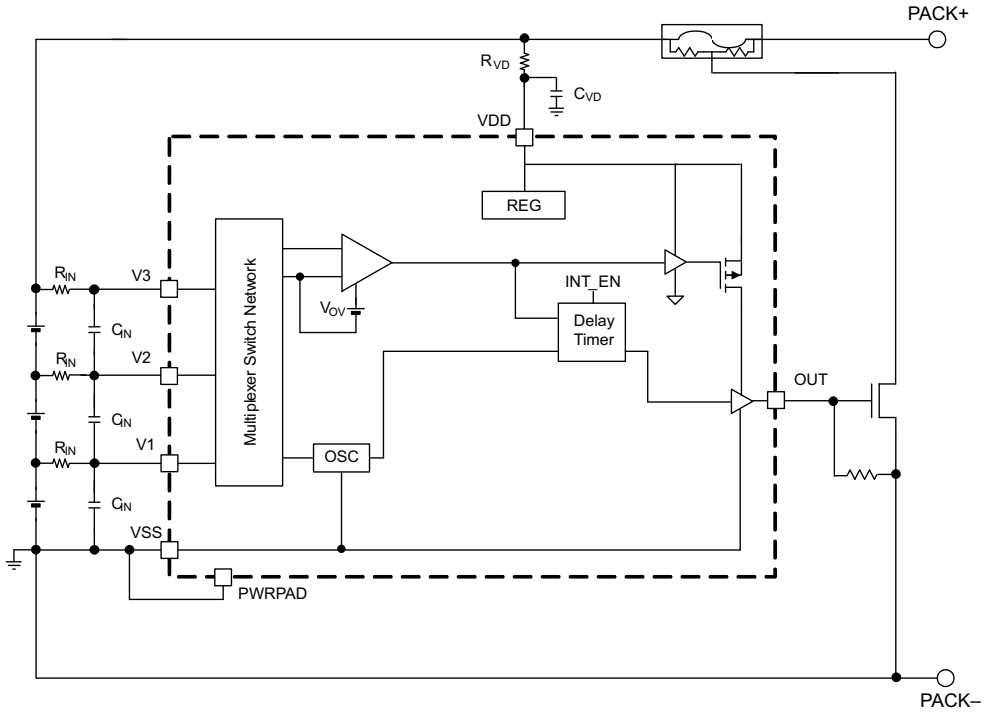
Figure 5. Output Voltage vs Output Current

8 Detailed Description

8.1 Overview

The bq2945xx is a second-level overvoltage (OV) protector. Each cell is monitored independently by comparing the actual cell voltage to a protection voltage threshold, V_{OV}. The protection threshold is preprogrammed at the factory with a range from 3.85 V to 4.65 V.

8.2 Functional Block Diagram



8.3 Feature Description

The voltage sensing for each cell is done independently using a multiplexer. The method of overvoltage detection is comparing the voltage to an overvoltage protection voltage V_{OV}. Once the voltage exceeds the programmed fixed value, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for either a 4-s or 6.5-s delay. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if *all* of the cell inputs (Vx) are below the OVP threshold minus the Vhys.

Feature Description (continued)

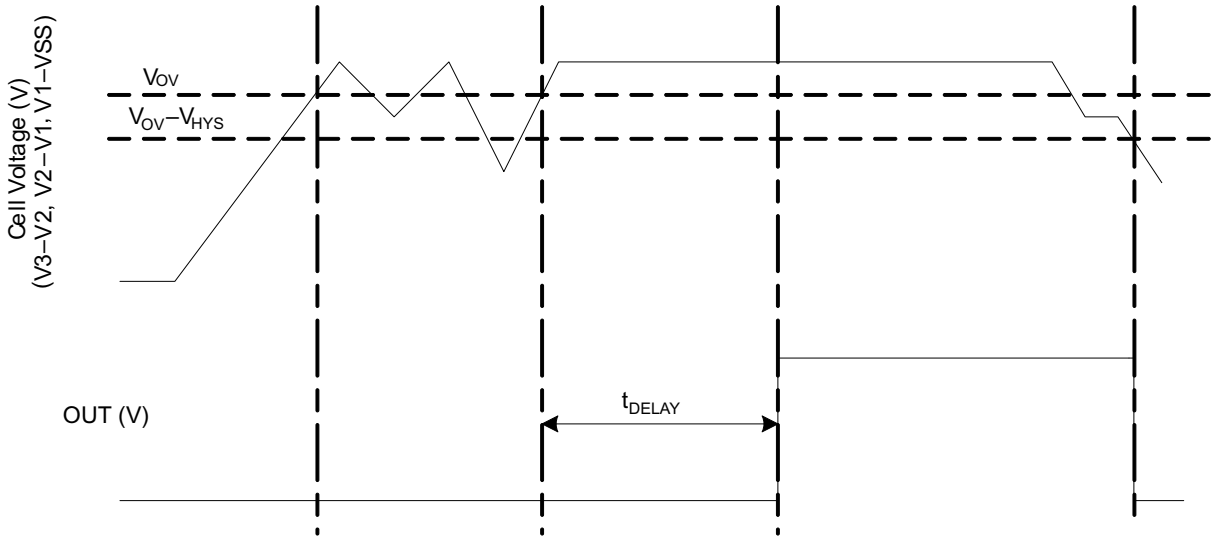


Figure 6. Timing for Overvoltage Sensing

8.3.1 Sense Positive Input for VX

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

The gate of an external N-channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. OUT will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.4 Thermal Pad, PWRPAD

For correct operation, the power pad (PWRPAD) is connected to the V_{SS} terminal on the PCB.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, VOV, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1) and (V3–V2). The OUT pin is inactive in this mode.

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, V_{OV} for the configured OV delay time, tDELAY. The OUT pin will pull high internally. An external FET ihen turns on, shorting the fuse to ground, which allows the battery or charger power to blow the fuse. When all of the cell voltages fall below (V_{OV}–V_{HYS}), the device returns to NORMAL mode.

Device Functional Modes (continued)

8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V3 (see Figure 7). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 7 shows the timing for CTM.

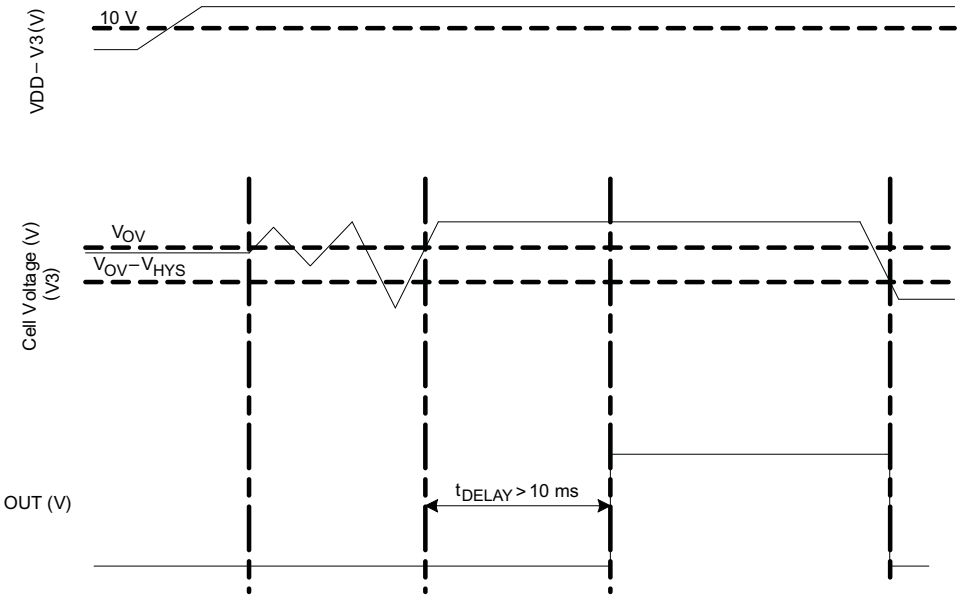


Figure 7. Timing for Customer Test Mode

Figure 8 shows the measurement for current consumption for the product for both VDD and Vx.

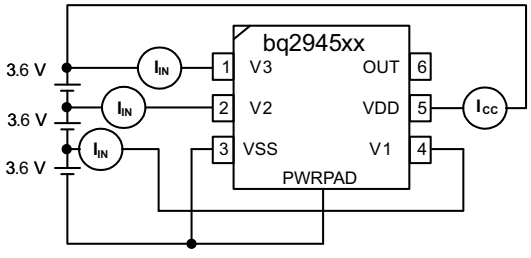


Figure 8. Configuration for IC Current Consumption Test

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2945xx devices are a family of second-level protectors used for overvoltage protection of the battery pack in the application. The device, when configuring the OUT pin with active high, drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery or charger power to blow the fuse and cut the power path.

9.2 Typical Application

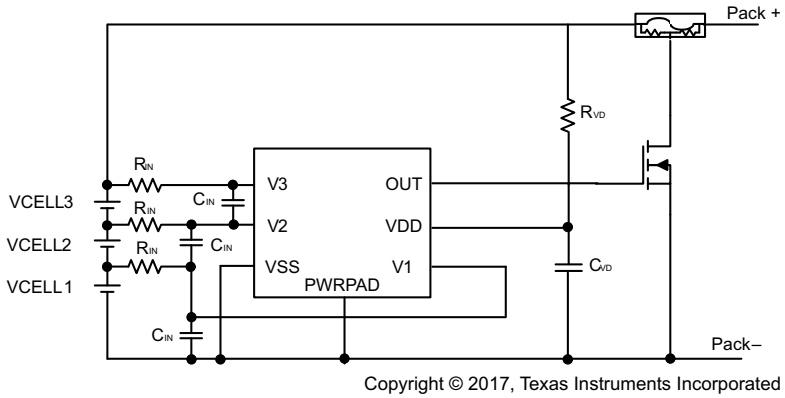


Figure 9. Application Configuration Schematic

9.2.1 Design Requirements

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 9 shows each external component.

Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	TYP	MAX	UNIT
Voltage monitor filter resistance	RIN	100	1000	4700	Ω
Voltage monitor filter capacitance	CIN	0.1		1	µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

9.2.2 Detailed Design Procedure

1. Determine the overvoltage threshold and delay time. Select the proper device from the table in *Device Comparison Table*, or contact TI for a different configuration.
2. Determine the number of cell in series. The device supports 2-S to 3-S cell configuration. For 2-S configuration, V3 pin should be shorted to V2.
3. Follow the application configuration schematic (see Figure 9) to connect the device.

9.2.3 Application Curves

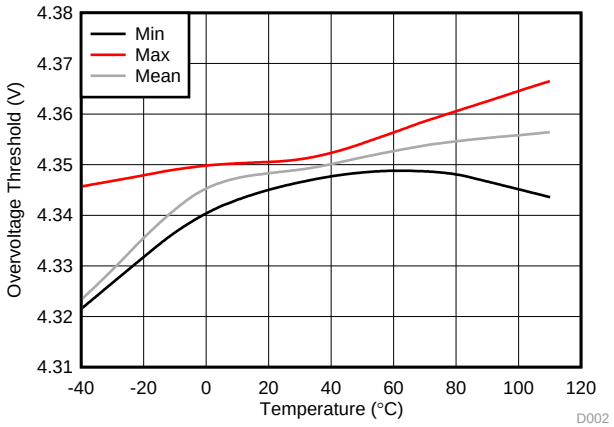


Figure 10. OVT vs Temperature

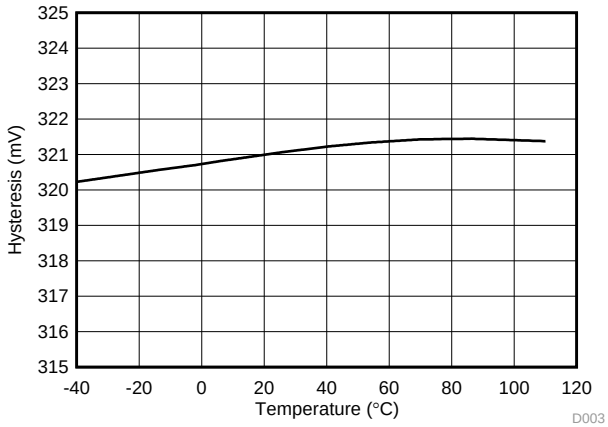


Figure 11. V_{HYS} vs Temperature

9.3 System Examples

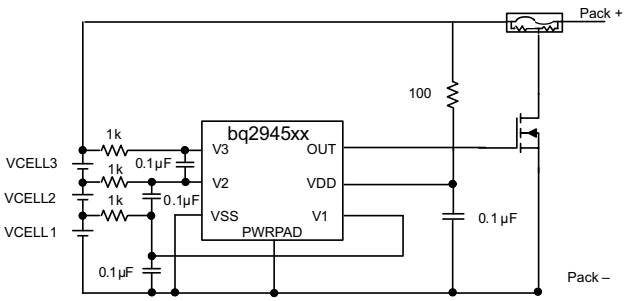


Figure 12. 3-Series Cell Configuration With Fixed Delay

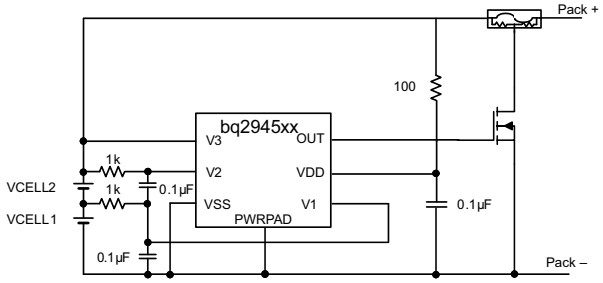


Figure 13. 2-Series Cell Configuration With Internal Fixed Delay

10 Power Supply Recommendations

The maximum power of this device is 25 V on VDD.

11 Layout

11.1 Layout Guidelines

- Ensure the RC filters for the V1 and VDD pins are placed as close as possible to the target terminal, reducing the tracing loop area.
- The VSS pin should be routed to the CELL– terminal.
- Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack– is sufficient to withstand the current during a fuse blown event.

11.2 Layout Example

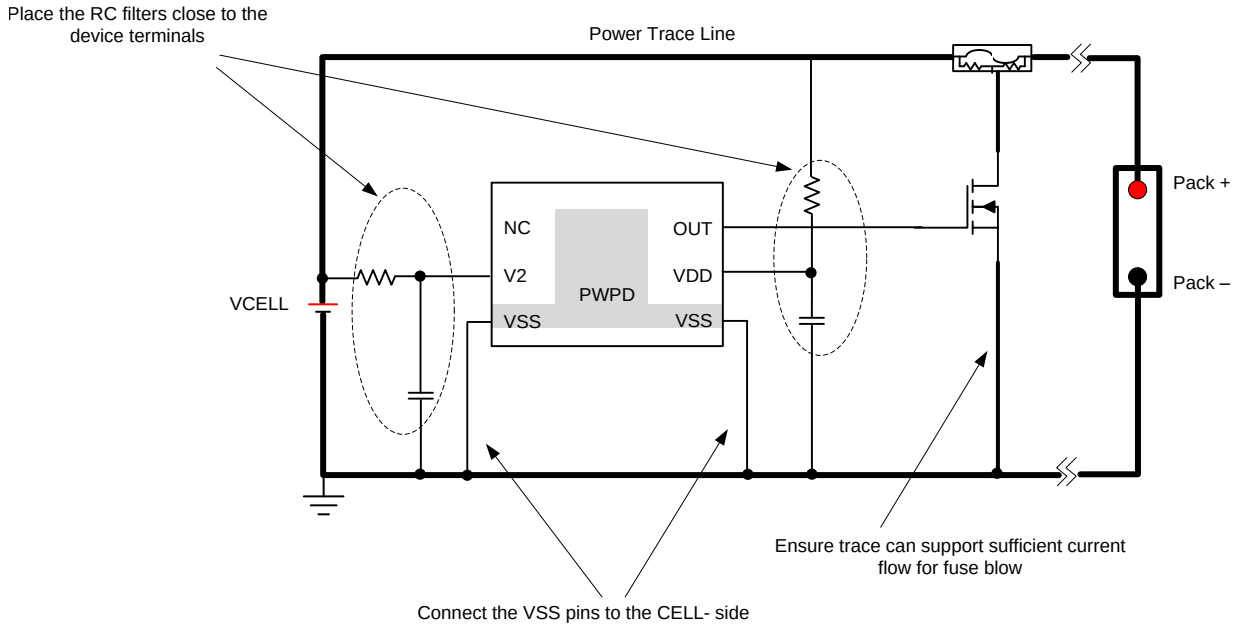


Figure 14. Layout Schematic

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **2.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
bq294502	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294504	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294512	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294522	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294524	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294532	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294533	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294582	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294592	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294502DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294502DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294504DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	Samples
BQ294504DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	Samples
BQ294512DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294512DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294522DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294522DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294524DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4524	Samples
BQ294524DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4524	Samples
BQ294532DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4532	Samples
BQ294532DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4532	Samples
BQ294533DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4533	Samples
BQ294533DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4533	Samples
BQ294582DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4582	Samples
BQ294582DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4582	Samples
BQ294592DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294592DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

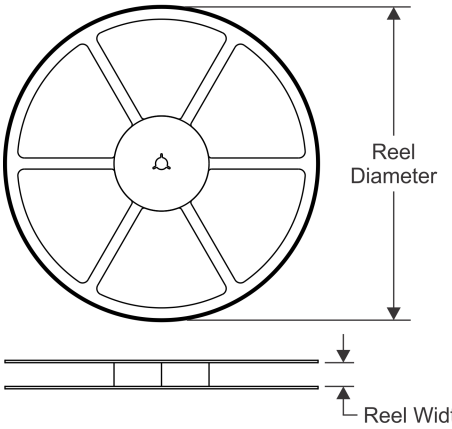
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

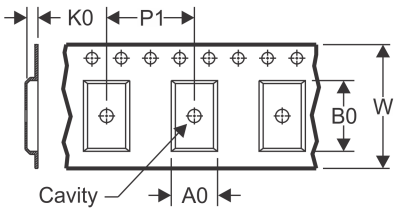
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

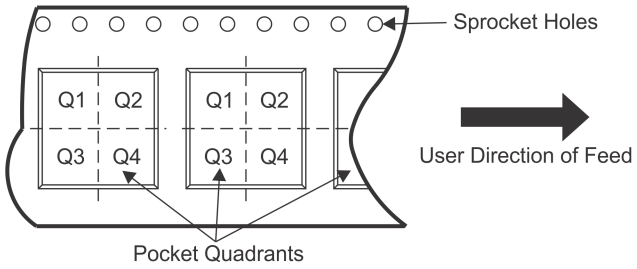


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

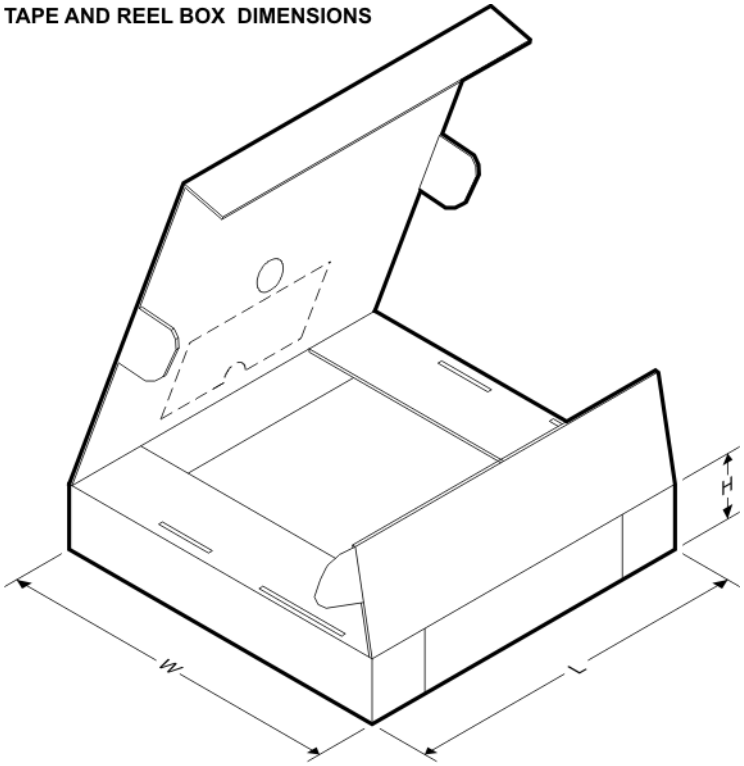


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294502DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294502DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294502DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294512DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294512DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294522DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294522DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294532DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294533DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294533DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



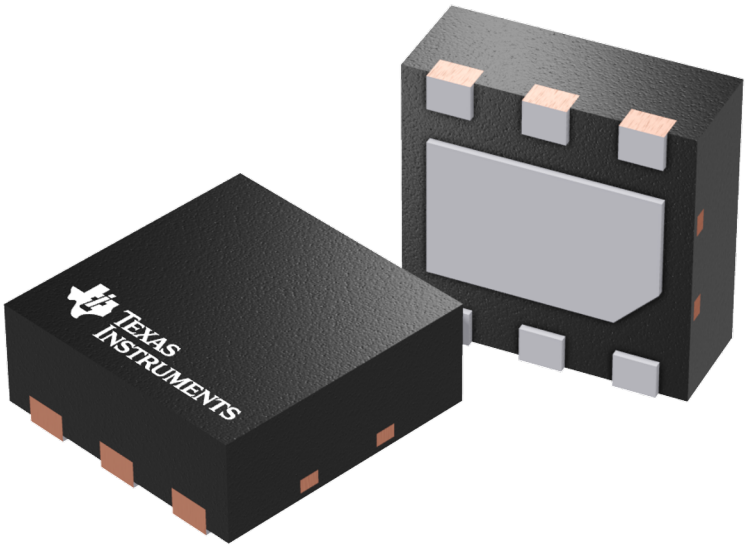
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294502DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294502DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294502DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294504DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294504DRVT	WSON	DRV	6	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294504DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294512DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294512DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294522DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294522DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294524DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294524DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294532DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294532DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294533DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294533DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294582DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294582DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294592DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294592DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



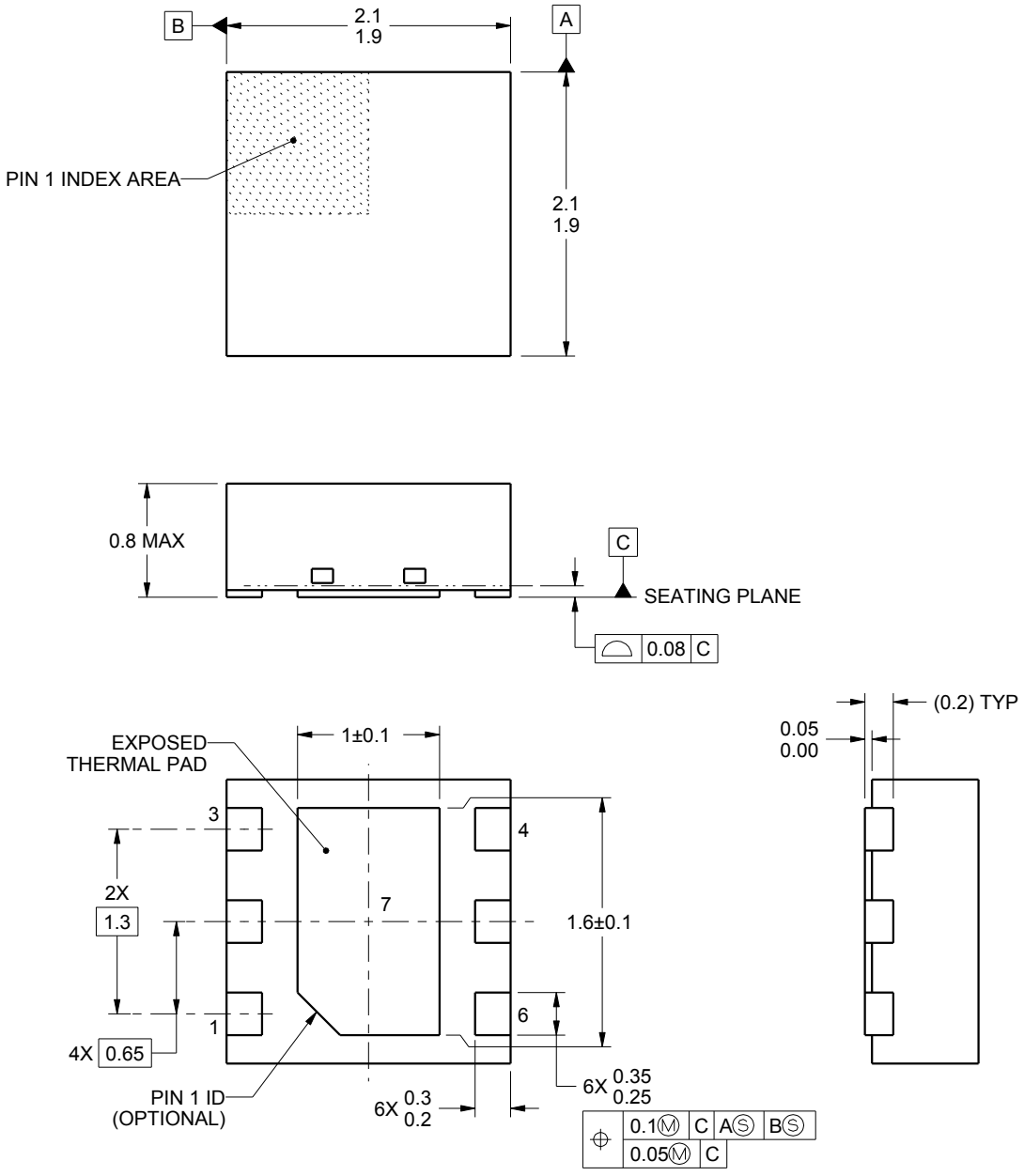
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

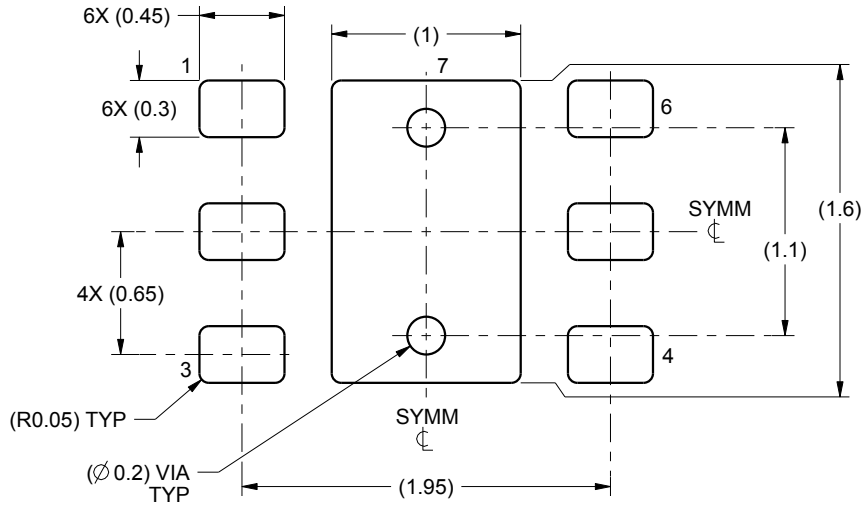
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

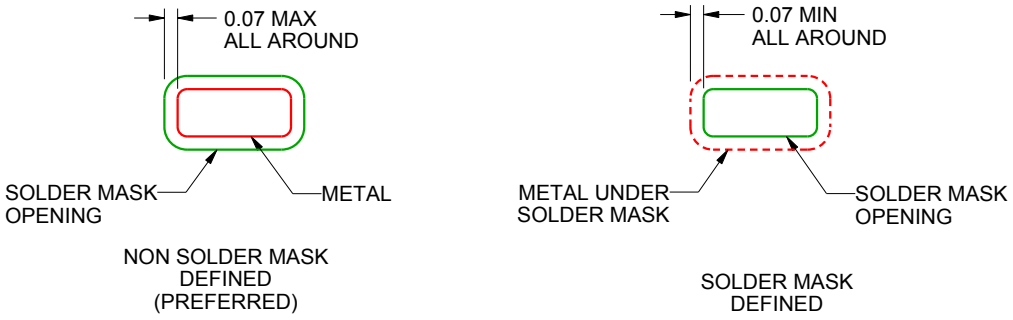


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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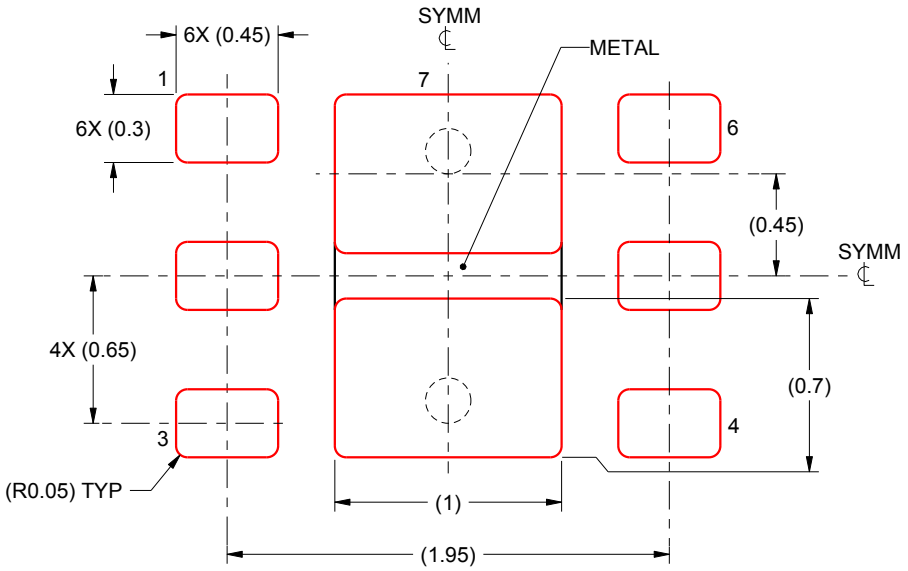
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/A 12/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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