具有内部延迟计时器的 2 节至 5 节串联锂离子电池 bq7718 过压保护器

1 特性

- 2、3、4 和 5 节串联电池过压保护
- 内部延迟定时器
- 固定的过压保护 (OVP) 阈值
- 高精度过压保护：
  ±10mV
- 低功耗 I_{CC}≈1μA
  （$V_{电池（全部）} < V_{保护}$）
- 每节电池输入的低泄漏电流 < 100nA
- 小型封装尺寸
  - 8 QFN (3.00mm x 4.00mm)

2 应用

- 为以下器件中的锂离子电池组提供保护：
  - 电动工具
  - 不间断电源 (UPS) 备用电池
  - 轻型电动车辆（电动自行车 (eBike)，电动踏板车 (eScooter)，踏板辅助自行车）

3 说明

bq7718xy 系列产品可提供适用于锂离子电池组系统的过压监视器和保护器。独立监控每节电池是否具有过压状态。为了实现更快速的产品线测试，bq7718xy 器件可提供延迟时间大幅减少的客户测试模式 (CTM)。

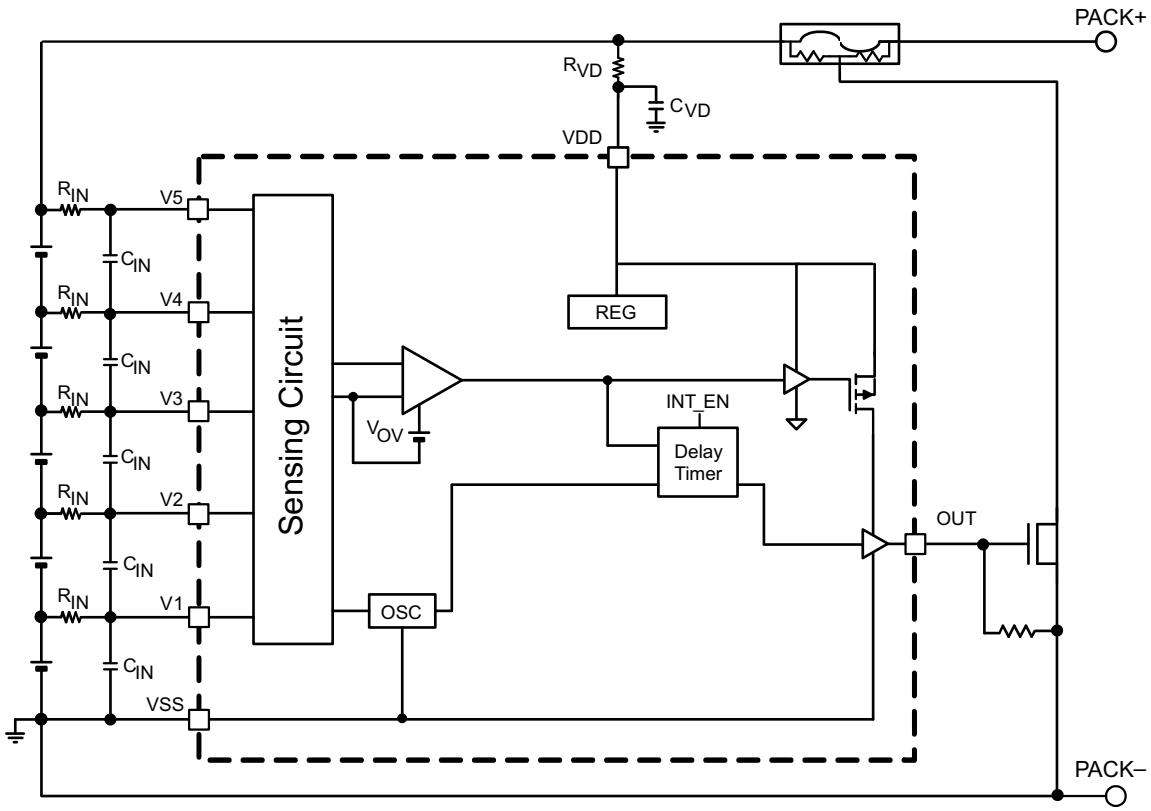
在 bq7718xy 器件中，一旦在任一节电池上检测到过压情况就会启动一个外部延迟定时器。在延迟定时器超时时，输出被触发进入其激活状态（根据配置的不同为高电平或低电平）。

器件信息表(1)

器件型号	封装	封装尺寸（标称值）
bq771800	WSON (8)	4.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅可订购产品附录（在数据表末尾）和器件比较表。

方框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (November 2014) to Revision E — **Page**

- 将数据表器件编号更改为 bq7718 1
- 增加了*方框图*图像 1
- Removed the Product Preview note from bq771806 in the *Device Comparison Table* 4
- Added bq771817 to Device Comparison Table 4
- Replaced the pinout image in the *Pin Configuration and Functions* section 5
- Deleted " Lead temperature (soldering, 10 s)" from the *Absolute Maximum Ratings* table 6
- Changed the *Handling Ratings* table to *ESD Ratings* table 6
- Removed the Product Preview note from bq771806 in the *DC Characteristics* table 7
- Added bq771817 to V_{HYS} DC Characteristics 7
- Added the *Timing Requirements* table 8
- Added the *Feature Description* section 11
- Added the *Device Functional Modes* section 12
- Added the *Power Supply Recommendations* section 16
- Added the *Layout* section 17

Changes from Revision C (August 2014) to Revision D — **Page**

- Added the bq771815 device to Production Data 4
- Changed the *Handling Ratings* table 6
- Added bq771817 to the V_{OV} DC Characteristics 7
- Added note to the *Application and Implementation* section 13

Changes from Revision B (October 2013) to Revision C — **Page**

- 已更改 数据表格式 1
- Added the bq771807 device to Production Data 4

Changes from Revision A (September 2013) to Revision B **Page**

- Added the bq771809 device to Production Data 4

Changes from Original (December 2012) to Revision A **Page**

- Added the bq771808 device to Production Data 4

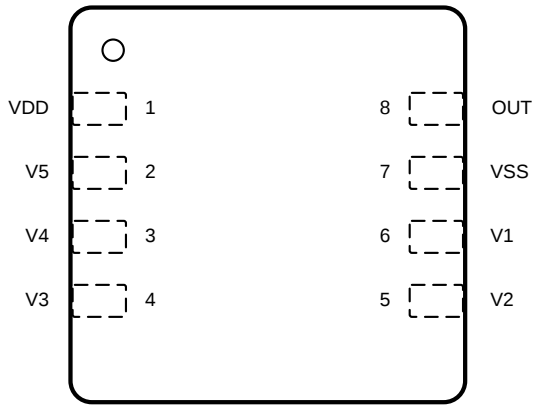
5 Device Comparison Table

T_A	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Delay	Output Drive	Tape and Reel (Large)	Tape and Reel (Small)
–40°C to 110°C	bq771800	8-Pin QFN	DPJ	4.300	0.300	4 s	CMOS Active High	bq771800DPJR	bq771800DPJT
	bq771801			4.275	0.050	3 s	NCH Active Low, Open Drain	bq771801DPJR	bq771801DPJT
	bq771802			4.225	0.300	1 s	NCH Active Low, Open Drain	bq771802DPJR	bq771802DPJT
	bq771803			4.275	0.050	1 s	NCH Active Low, Open Drain	bq771803DPJR	bq771803DPJT
	bq771804(1)			4.225	0.300	3 s	CMOS Active High	bq771804DPJR	bq771804DPJT
	bq771805(1)			4.325	0.300	3 s	CMOS Active High	bq771805DPJR	bq771805DPJT
	bq771806			4.350	0.300	3 s	CMOS Active High	bq771806DPJR	bq771806DPJT
	bq771807			4.450	0.300	3 s	CMOS Active High	bq771807DPJR	bq771807DPJT
	bq771808			4.200	0.050	1 s	NCH Active Low	bq771808DPJR	bq771808DPJT
	bq771809			4.200	0.050	1 s	CMOS Active High	bq771809DPJR	bq771809DPJT
	bq771810(1)			4.200	0.250	1 s	CMOS Active High	bq771810DPJR	bq771810DPJT
	bq771811(1)			4.225	0.050	1 s	CMOS Active High	bq771811DPJR	bq771811DPJT
	bq771812(1)			4.250	0.050	1 s	CMOS Active High	bq771812DPJR	bq771812DPJT
	bq771813(1)			4.250	0.050	1 s	CMOS Active High	bq771813DPJR	bq771813DPJT
	bq771814(1)			3.900	0.300	3 s	CMOS Active High	bq771814DPJR	bq771814DPJT
	bq771815			4.225	0.050	1 s	NCH Active Low	bq771815DPJR	bq771815DPJT
	bq771816(1)			4.250	0.050	1 s	NCH Active Low	bq771816DPJR	bq771816DPJT
	bq771817			4.275	0.050	1 s	CMOS Active High	bq771817DPJR	bq771817DPJRT
	bq7718xy(2)			3.850–4.650	0–0.300	1 s	NCH, Active Low, Open Drain	bq7718xyDPJR	bq7718xyDPJT

(1) Product Preview only.
(2) Future option, contact TI.

6 Pin Configuration and Functions

DPJ Package
8-Pin (WSON)
Top View



Pin Functions

NO.	NAME	TYPE I/O	DESCRIPTION
1	VDD	P	Power supply
2	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
3	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
4	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
5	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
6	V1	I	Sense input for positive voltage of the lowest cell in the stack
7	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
8	OUT	O	Output drive for overvoltage fault signal

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD–VSS	–0.3	30	V
Input voltage range	V5–VSS or V4–VSS or V3–VSS or V2–VSS or V1–VSS	–0.3	30	V
Output voltage range	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See *Thermal Information*		
Functional temperature		–40	110	°C
Storage temperature range, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Rating	Electrostatic discharge	Human body model (HBM) ESD stress voltage(1)	±2000	V
		Charged device model (CDM) ESD stress voltage(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}(1)		3	25	V
Input voltage range	V5–V4 or V4–V3 or V3–V2 or V2–V1 or V1–VSS	0	5	V
Operating ambient temperature range, T_A		–40	110	°C

(1) See Systems Examples.

7.4 Thermal Information

THERMAL METRIC(1)		bq7718xy DPJ (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.6	°C/W
$R_{\theta JCtop}$	Junction-to-case(top) thermal resistance	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JCbot}$	Junction-to-case(bottom) thermal resistance	11.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 DC Characteristics

Typical values stated where T_A = 25°C and V_{DD} = 18 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 25 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Protection Threshold VCx						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	bq771800		4.300		V
		bq771801		4.275		V
		bq771803		4.275		V
		bq771802		4.225		V
		bq771804(1)		4.225		V
		bq771805(1)		4.325		V
		bq771806		4.350		V
		bq771807		4.450		V
		bq771808		4.200		V
		bq771809		4.200		V
		bq771810(1)		4.200		V
		bq771811(1)		4.225		V
		bq771812(1)		4.250		V
		bq771813(1)		4.250		V
		bq771814(1)		3.900		V
		bq771815		4.225		V
		bq771816(1)		4.250		V
		bq771817		4.275		V
V_{HYS}	OV Detection Hysteresis	bq771800	250	300	400	mV
		bq771801	0	50	100	mV
		bq771802	250	300	400	mV
		bq771803	0	50	100	mV
		bq771804(1)	250	300	400	mV
		bq771805(1)	250	300	400	mV
		bq771806	250	300	400	mV
		bq771807	250	300	400	mV
		bq771808	0	50	100	mV
		bq771809	0	50	100	mV
		bq771810(1)	200	250	250	mV
		bq771811(1)	0	50	100	mV
		bq771812(1)	0	50	100	mV
		bq771813(1)	0	50	100	mV
		bq771814(1)	250	300	400	mV
		bq771815	0	50	100	mV
		bq771816(1)	0	50	100	mV
		bq771817	0	50	100	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		44	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV

(1) Product Preview only.

DC Characteristics (continued)

Typical values stated where T_A = 25°C and V_{DD} = 18 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 25 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply and Leakage Current						
I_{CC}	Supply Current	(V5–V4) = (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4 V (See Figure 8.)		1	2	µA
I_{IN}	Input Current at Vx Pins	(V5–V4) = (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4 V (See Figure 8.)	–0.1		0.1	µA
Output Drive OUT, CMOS Active HIGH Versions Only						
V_{OUT1}	Output Drive Voltage, Active High	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V, I_{OH} = 100 µA	6			V
		If three of four cells are short circuited and only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 µA		VDD – 0.3		V
		(V5–V4), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 18 V, I_{OL} = 100 µA measured into pin		250	400	mV
I_{OUTH1}	OUT Source Current (during OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V. OUT = 0 V. Measured out of OUT pin			4.5	mA
I_{OUTL1}	OUT Sink Current (no OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 18 V, OUT = VDD. Measured into OUT pin	0.5		14	mA
Output Drive OUT, NCH Open Drain Active LOW Versions Only						
V_{OUT2}	Output Drive Voltage, Active Low	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH2}	OUT Sink Current (during OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V. OUT = VDD. Measured into OUT pin	0.5		14	mA
I_{OUTL2}	OUT Source Current (no OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 18 V. OUT = VDD. Measured out of OUT pin			100	nA

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
Delay Timer						
t_{DELAY}	OV Delay Time	bq771800	3.2	4	4.8	s
		bq771801, bq771807	2.4	3	3.6	s
		bq771802, bq771803, bq771815	0.8	1	1.2	s
		Preview option only. Contact TI.	4.4	5.5	6.6	s
$X_{CTMDELAY}$	Fault Detection Delay Time during Customer Test Mode	See Customer Test Mode.		15		ms

7.7 Typical Characteristics

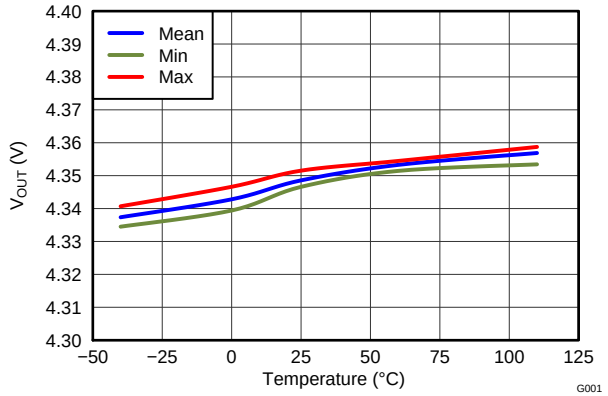


Figure 1. Overvoltage Threshold (OVT) vs. Temperature

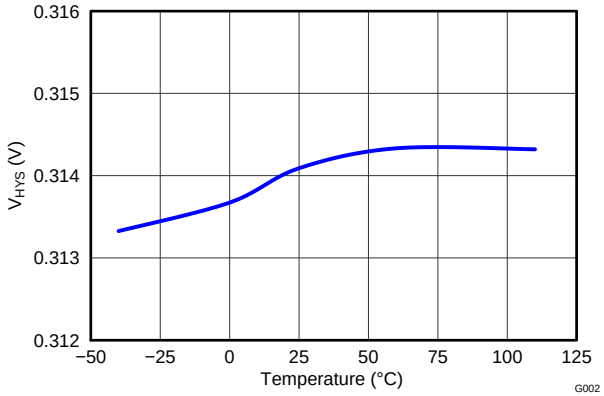


Figure 2. Hysteresis V_{HYS} vs. Temperature

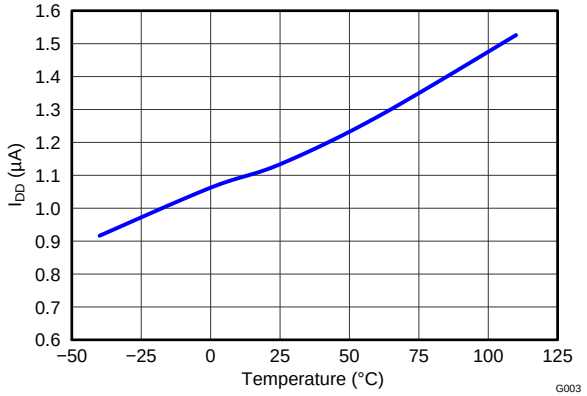


Figure 3. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

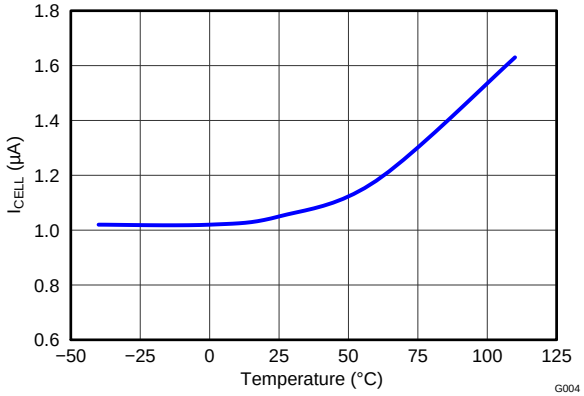


Figure 4. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

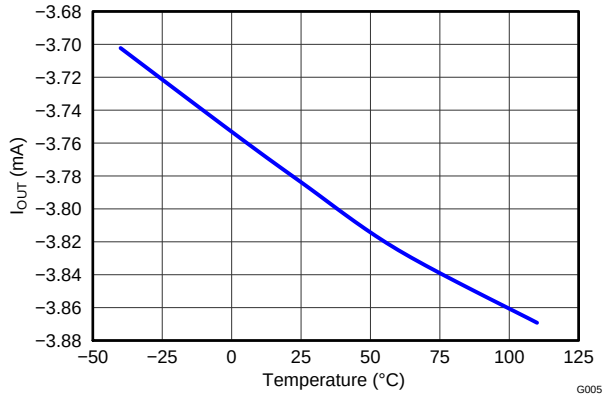


Figure 5. Output Current I_{OUT} vs. Temperature

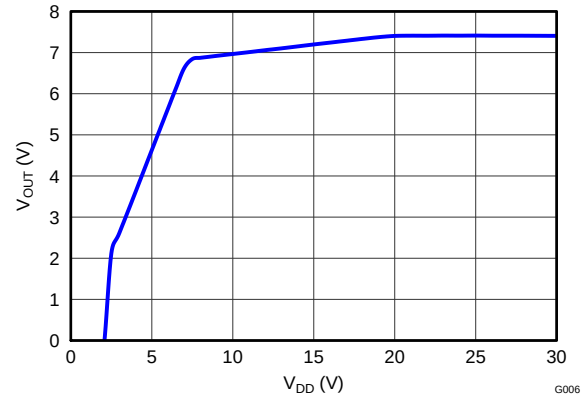


Figure 6. V_{OUT} vs. V_{DD}

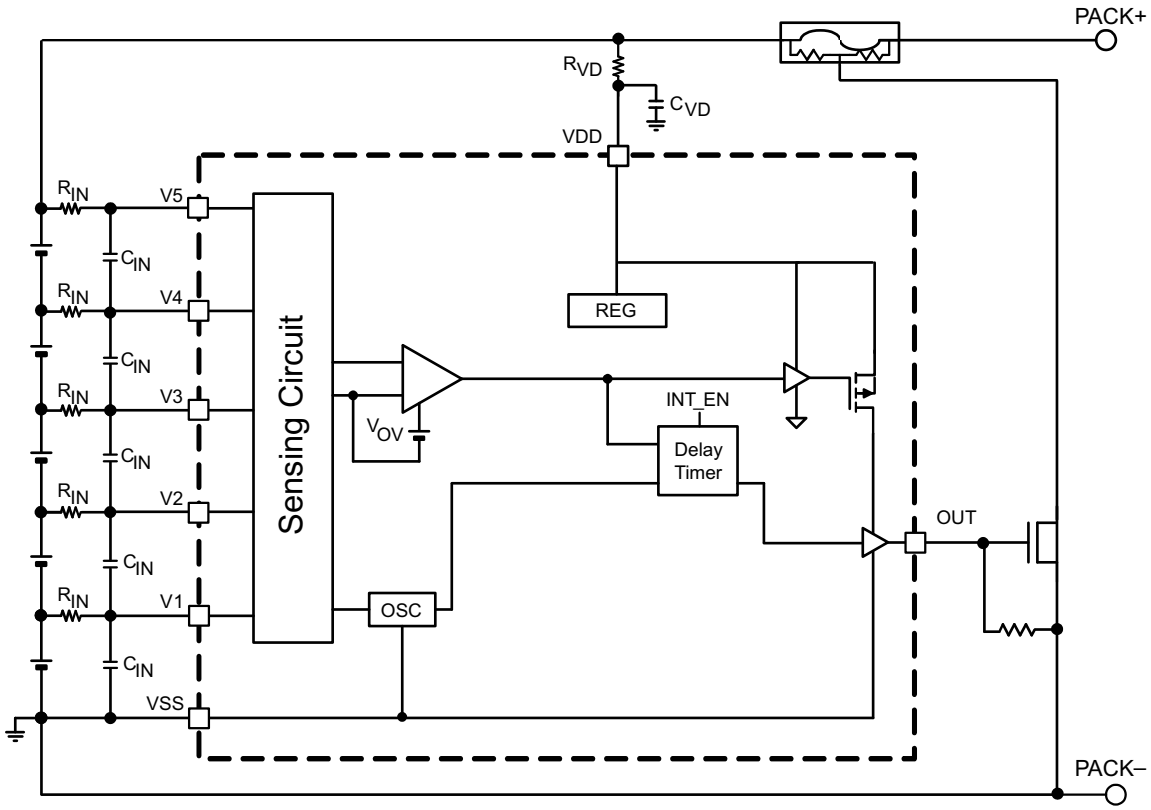
8 Detailed Description

8.1 Overview

In the bq7718xy family of devices, each cell is monitored independently and an external delay timer is initiated if an overvoltage condition is detected on any cell.

For quicker production-line testing, the device provides a Customer Test Mode with greatly reduced delay time.

8.2 Functional Block Diagram



8.3 Feature Description

In the bq7718xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the OUT pin goes from inactive to active state.

For NCH Open Drain Active Low configurations, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).

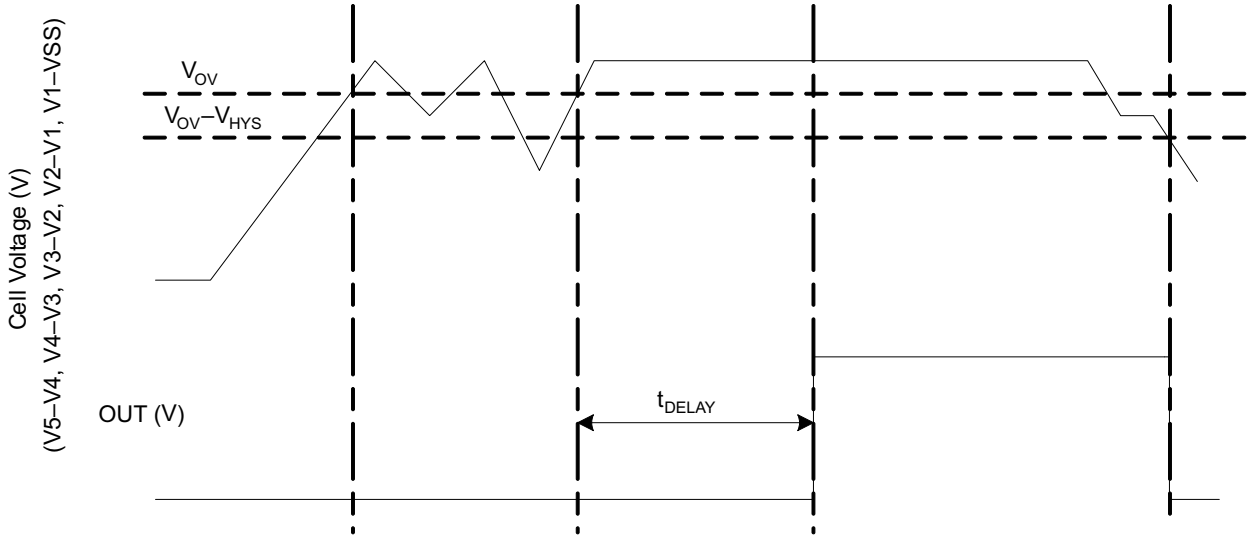


Figure 7. Timing for Overvoltage Sensing

8.3.1 Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

This pin serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

8.3.3 Supply Input, VDD

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.4 Device Functional Modes

8.4.1 Normal Mode

When all of the cell voltages are below the overvoltage threshold, V_{OV}, the device operates in Normal mode. The device monitors the differential cell voltages connected across (V1 – VSS), (V2 – V1), (V3 – V2), (V4 – V3), and (VC4 – VC5). The OUT pin is inactive and if configured:

The OUT pin is inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

8.4.2 Overvoltage Mode

Overvoltage mode is detected if any of the cell voltages exceeds the overvoltage threshold, V_{OV} for configured OV delay time. The OUT pin is activated after a delay time set by the capacitance in the CD pin. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When all of the cell voltages fall below the (V_{OV} – V_{HYS}), the device returns to NORMAL mode

8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V5 (see Figure 8). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V5 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V5–V4), (V4–V3), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 8 shows the timing for the Customer Test Mode.

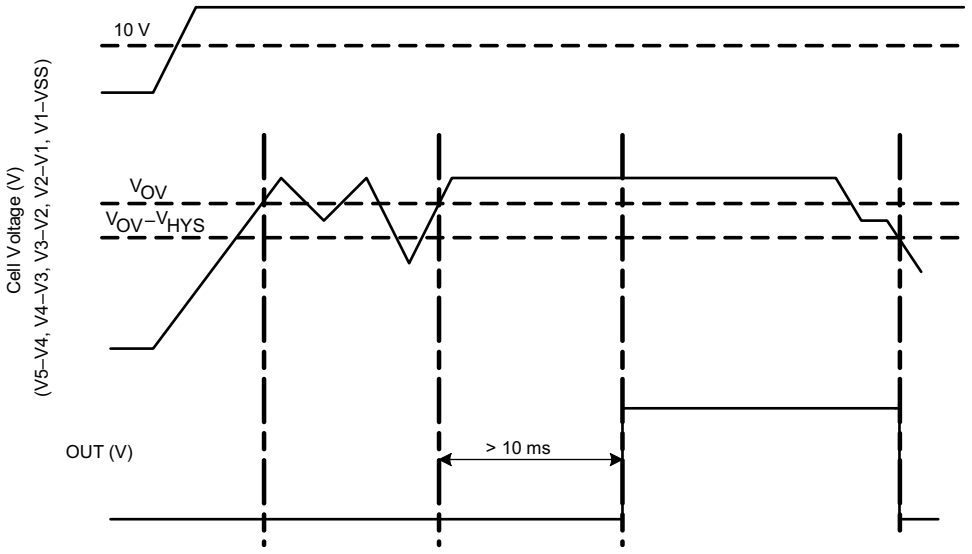


Figure 8. Timing for Customer Test Mode

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT pin. Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

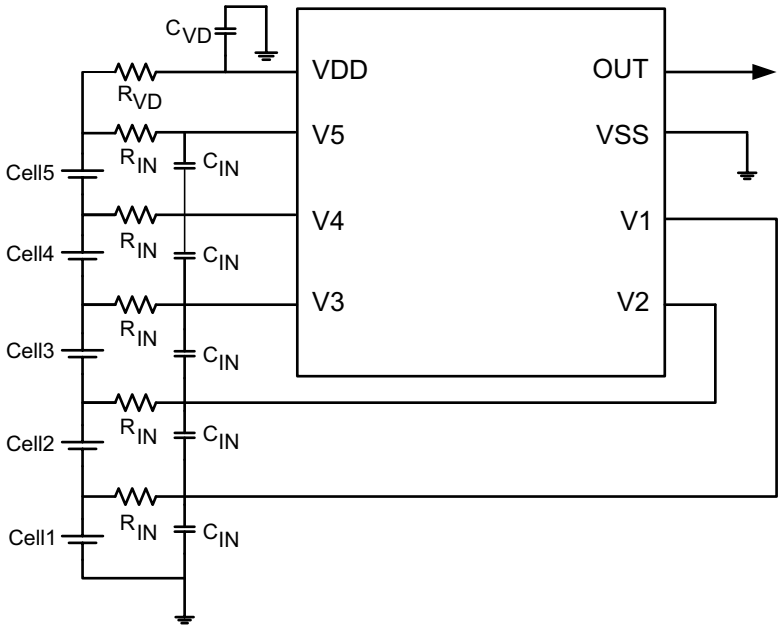


Figure 9. Application Configuration

9.1.1 Design Requirements

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 9 shows each external component.

Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	1100	Ω
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	µF
Supply voltage filter resistance	R_{VD}	100		1K	Ω
Supply voltage filter capacitance	C_{VD}		0.1		µF
CD external delay capacitance			0.1	1	µF
OUT Open drain version pull-up resistance to PACK+			100		kΩ

NOTE

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

9.1.2 Detailed Design Procedure

Figure 10 shows the measurement for current consumption for the product for both VDD and Vx.

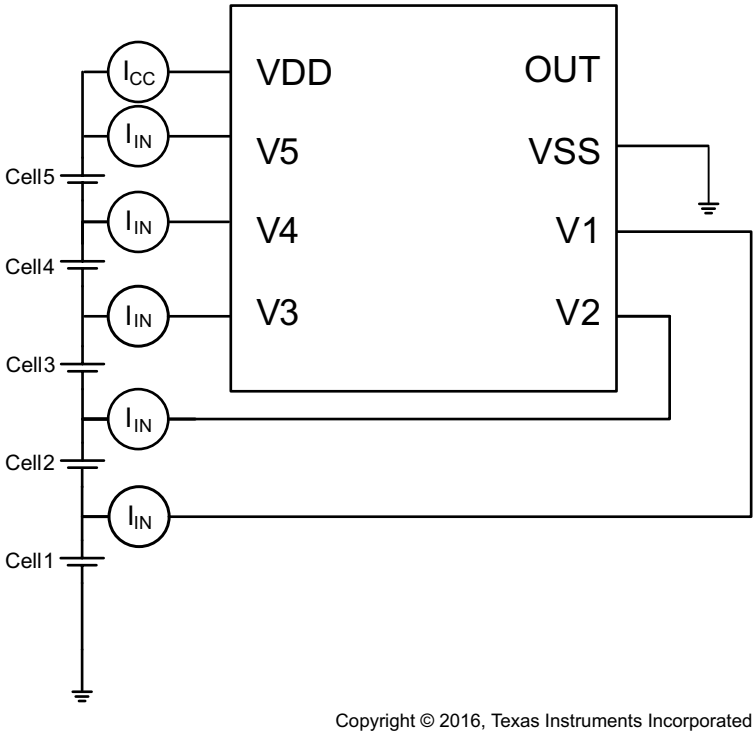


Figure 10. Configuration for IC Current Consumption Test

9.1.2.1 Application Curves

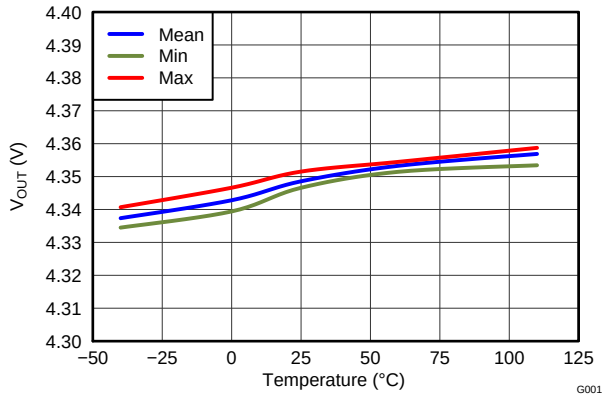


Figure 11. Overvoltage Threshold (OVT) vs. Temperature

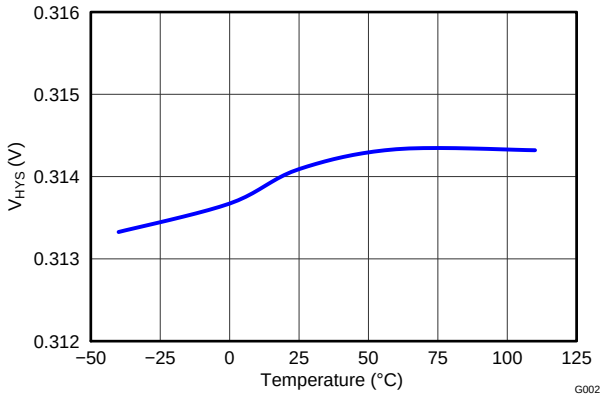


Figure 12. Hysteresis V_{HYS} vs. Temperature

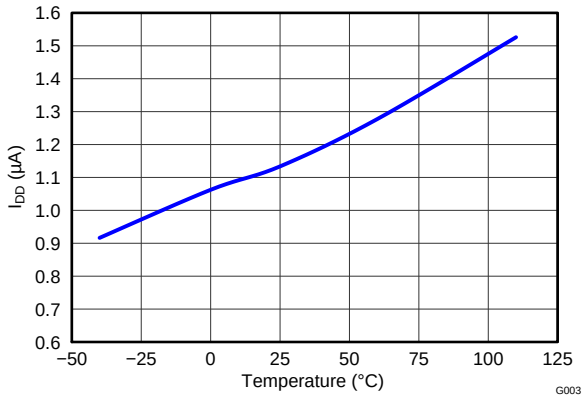


Figure 13. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

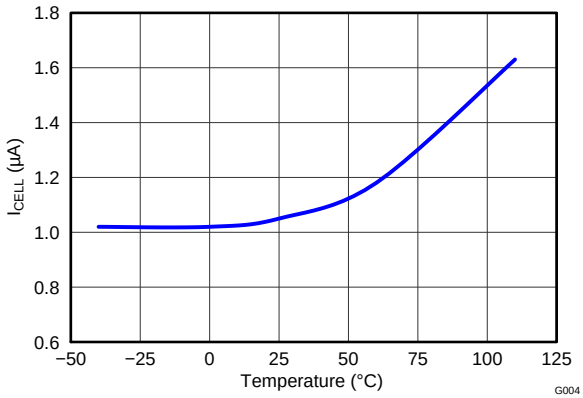


Figure 14. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

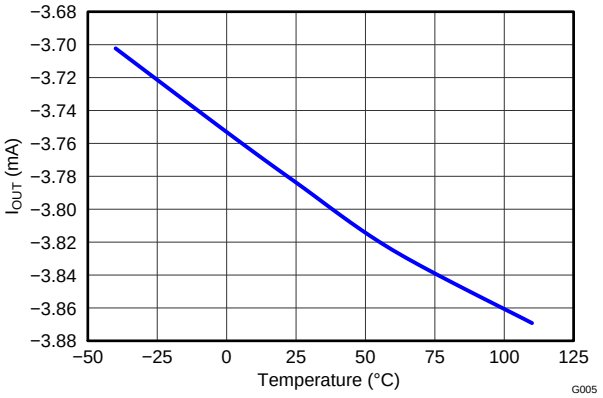


Figure 15. Output Current I_{OUT} vs. Temperature

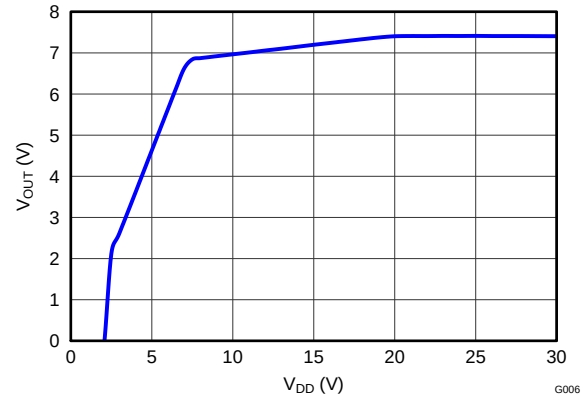


Figure 16. V_{OUT} vs. V_{DD}

9.2 Systems Examples

In these application examples, an external pull-up resistor is required on the OUT pin to configure for an Open Drain Active Low operation.

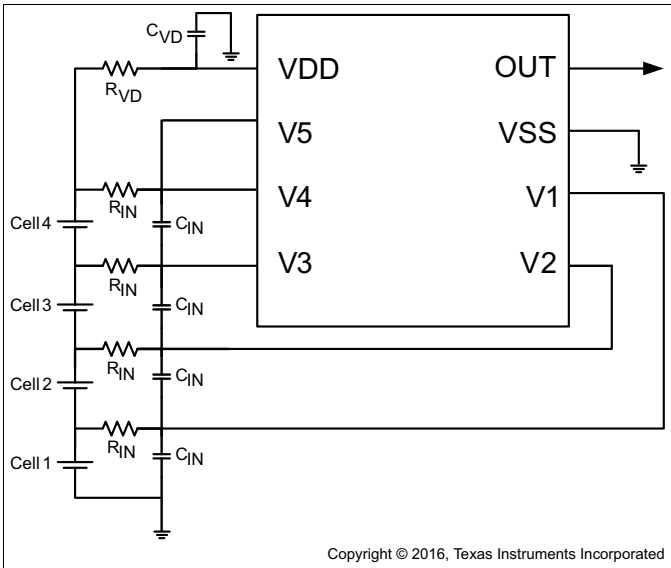


Figure 17. 4-Series Cell Configuration

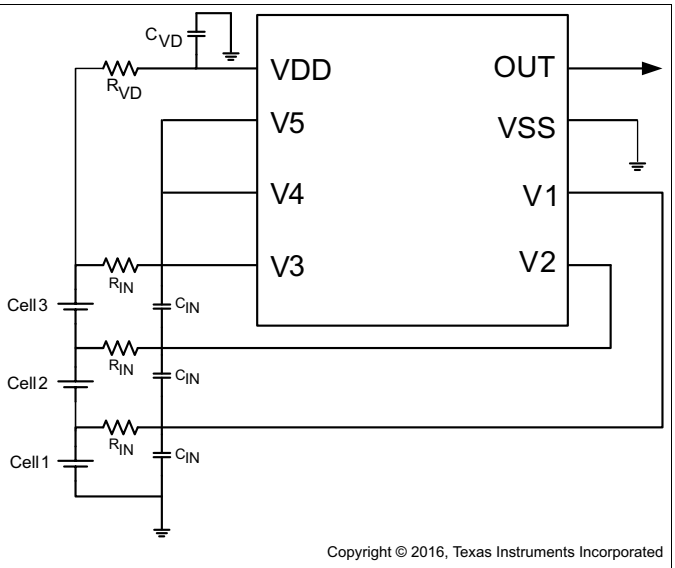


Figure 18. 3-Series Cell Configuration with Fixed Delay

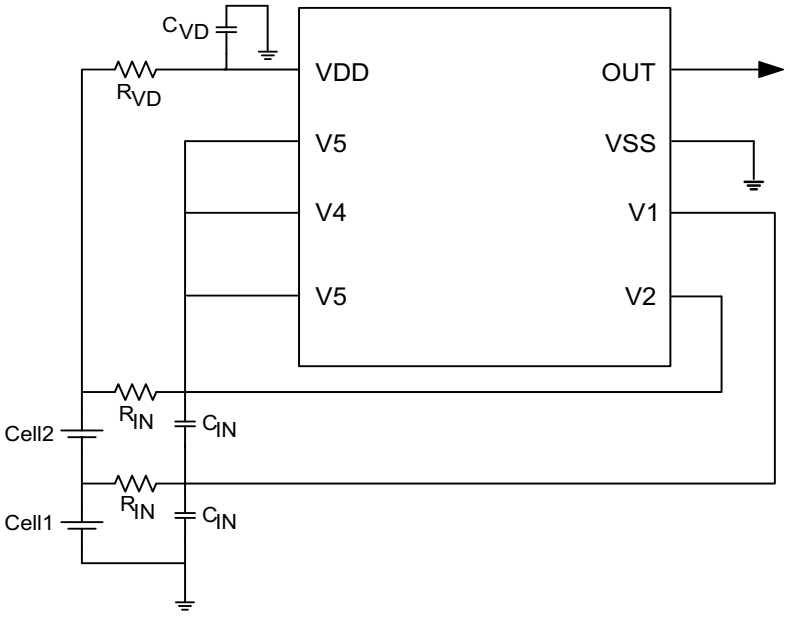


Figure 19. 2-Series Cell Configuration with Internal Fixed Delay

10 Power Supply Recommendations

The maximum power of this device is 25 V on VDD.

11 Layout

11.1 Layout Guidelines

- Ensure the RC filters for the V1 and VDD pins are placed as close as possible to the target terminal.
- The VSS pin should be routed to the CELL– terminal.

11.2 Layout Example

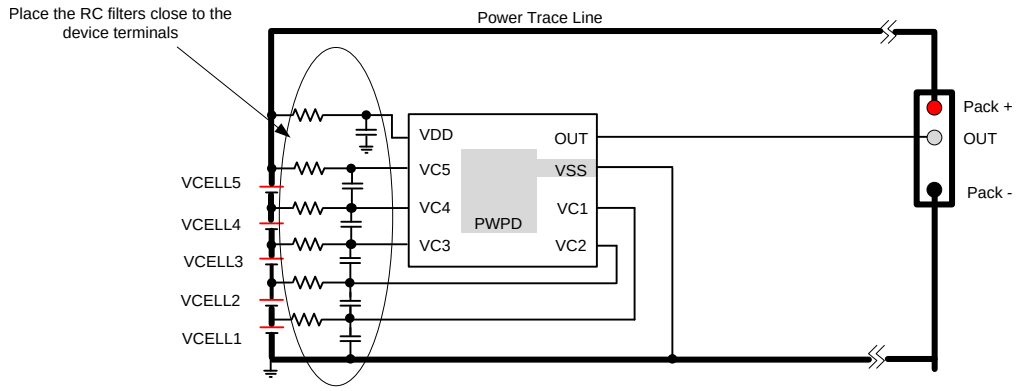


Figure 20. Example Layout

12 器件和文档支持

12.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可通过快速访问立刻订购。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持与社区
bq7718	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771800	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771801	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771802	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771803	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771806	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771807	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771808	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771809	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771815	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq771817	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771800DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771800	Samples
BQ771800DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771800	Samples
BQ771801DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771801	Samples
BQ771801DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771801	Samples
BQ771802DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771802	Samples
BQ771802DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771802	Samples
BQ771803DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771803	Samples
BQ771803DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771803	Samples
BQ771806DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771806	Samples
BQ771806DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771806	Samples
BQ771807DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771807	Samples
BQ771807DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771807	Samples
BQ771808DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771808	Samples
BQ771808DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771808	Samples
BQ771809DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771809	Samples
BQ771809DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771809	Samples
BQ771815DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771815	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771815DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771815	Samples
BQ771817DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771817	Samples
BQ771817DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771817	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

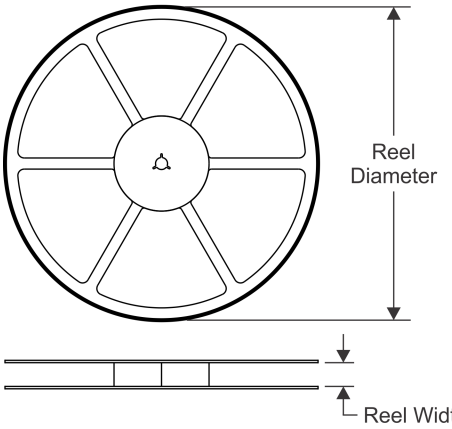
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

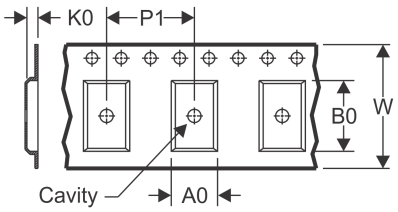
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

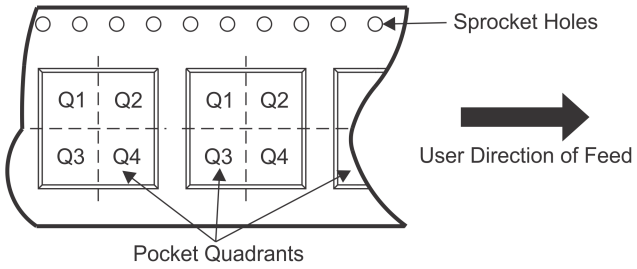


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

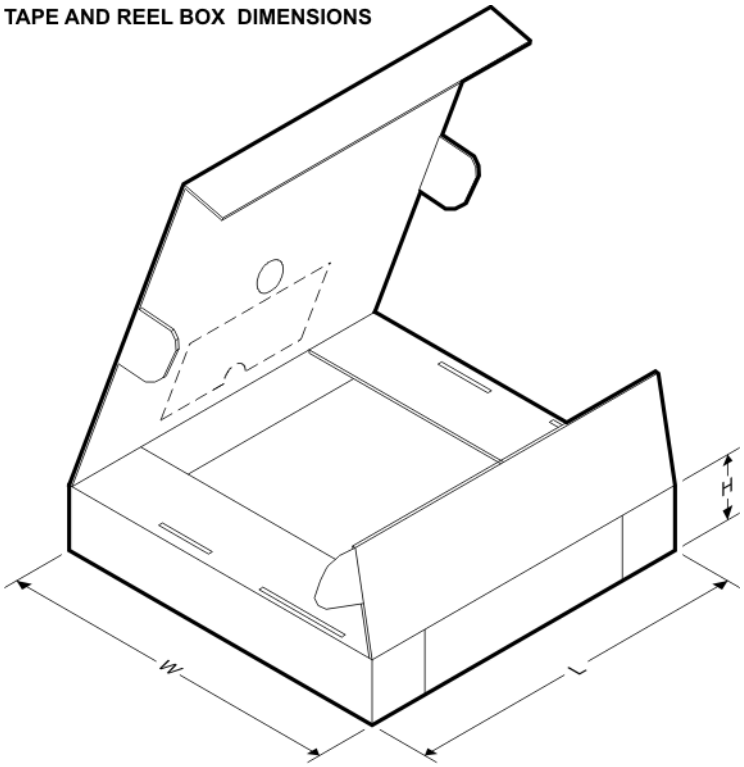


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771800DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771800DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771801DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771801DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771802DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771802DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771803DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771803DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771806DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771806DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771807DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771807DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771808DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771808DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771809DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771809DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771815DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771815DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771817DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771817DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

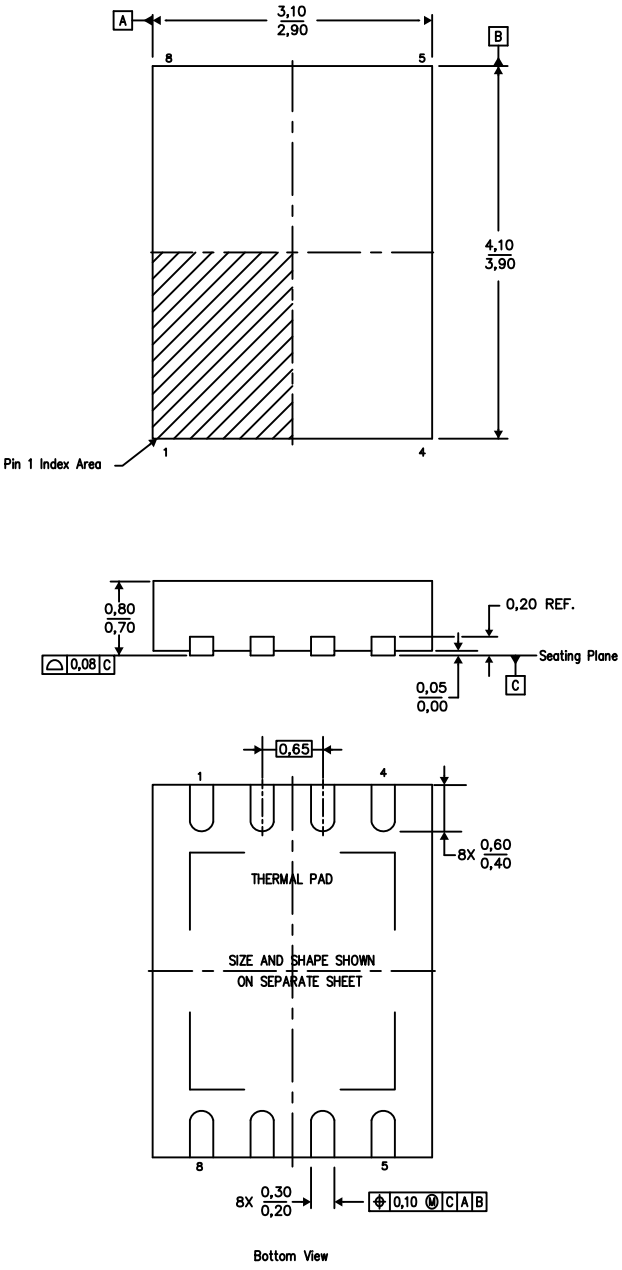


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771800DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771800DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771801DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771801DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771802DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771802DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771803DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771803DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771806DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771806DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771807DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771807DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771808DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771808DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771809DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771809DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771815DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771815DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771817DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771817DPJT	WSON	DPJ	8	250	210.0	185.0	35.0

DPJ (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4212590/B 04/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

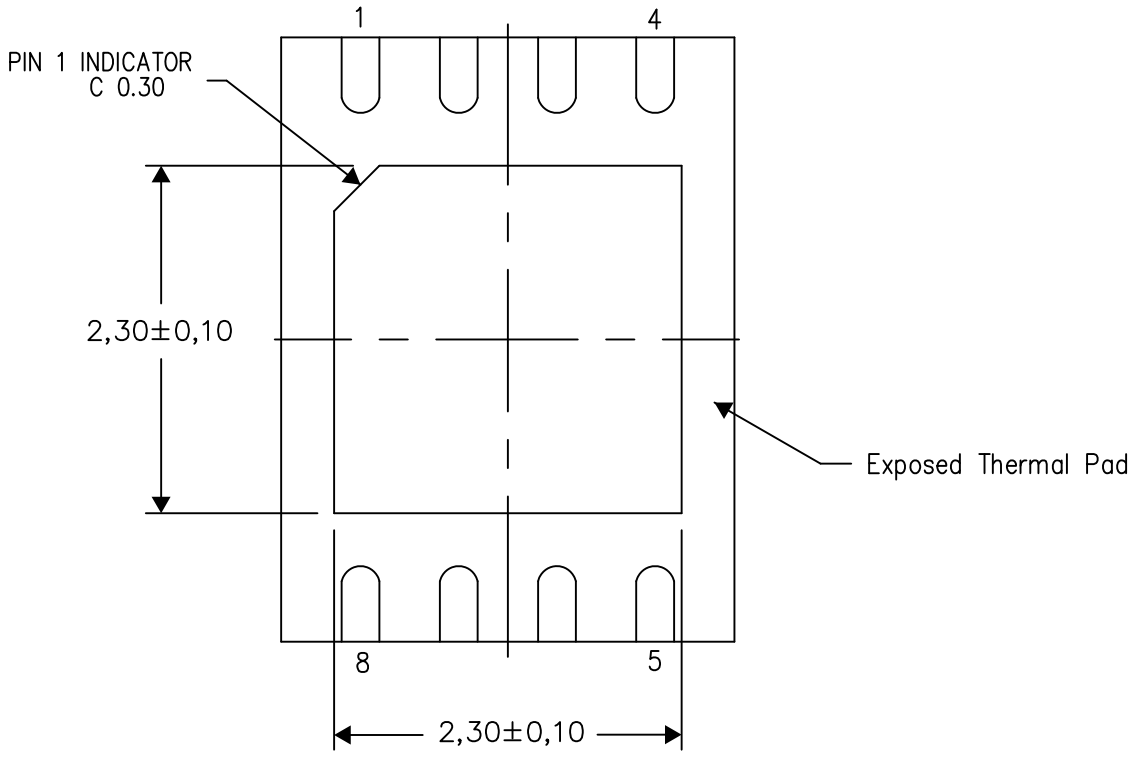
DPJ (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212605/A 04/12

NOTE: All linear dimensions are in millimeters

重要声明

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